



DS21Q59 Quad E1 Transceiver

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REVISION A1 ERRATA

The errata listed below describe situations where DS21Q59 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS21Q59 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. The die revision can also be determined through the IDR register at location 0Fh. The four MSBs are fixed to "1001," indicating the DS21Q59 device. The four LSB's contain the revision code "0000" on A1 revision devices. To obtain an errata sheet on another DS21Q59 die revision, visit our website at www.maxim-ic.com/errata or contact technical support at technical.support@dalsemi.com.

1. LINE BUILD-OUT SETTING 5, "120Ω WITH HIGH RETURN LOSS" DOES NOT MEET TEMPLATE

Description:

The output waveform of the line build-out selected by LICR bit settings L2 = 1, L1 = 0, and L0 = 1 does not meet specifications and should not be used.

Work Around:

There is no known work-around for this erratum.