Rev: 030603

ERRATA SHEET
DS1501/DS1511

Revision A6 Errata

The errata listed below describe situations where DS1501/DS1511 revision A6 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

*This errata sheet only applies to DS1501/DS1511 revision A6 components. Revision A6 components are branded on the topside of the package with a six-digit code in the form yywwA6, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS1501/DS1511 die revision, visit our website at **www.maxim-ic.com/errata**.*

1) ALARMS RETRIGGER AFTER CLEAR

Description:
The alarm retriggers after clear. Under normal operation, after an alarm a service routine clears the interrupt. Writing to any register in the device causes the alarm to retrigger if done within the first second after the initial alarm.

Workaround:
The recommended workaround is to delay clearing the alarm until all writes to the device are done. The alarm can then be cleared after a delay of at least 488µs after the last write.

2) WATCHDOG HAS A +5ms OFFSET BETWEEN PROGRAMMED AND ACTUAL TIMEOUT

Description:
The watchdog has a +5ms offset between the programmed and the actual timeout.

Workaround:
None.

3) TE MUST BE ACTIVE FOR AT LEAST 488µs TO ENSURE A TRANSFER

Description:
TE must be active for at least 488µs to ensure a transfer, but this is not indicated in the data sheet.

Workaround:
See errata #5. This requirement is expected to change on the new revision.

4) $\overline{RST}$ DOES NOT GO INACTIVE IF V_{CC} GOES INACTIVE WHILE $\overline{RST}$ IS LOW FROM A WATCHDOG EVENT

Description:
If the watchdog is steered to the $\overline{RST}$ output and V_{CC} goes inactive during a watchdog event, $\overline{RST}$ never deactivates.

Workaround:
Do not steer the watchdog output to the $\overline{RST}$ output.

5) INCORRECT DATA IS SOMETIMES TRANSFERRED FROM THE INTERNAL REGISTERS TO THE BUFFERS

Description:
Incorrect data is sometimes transferred from the internal time and date registers to the user registers when the TE bit is set to 0, or when any register is written before reading any time or date register.

Workaround:
To read the time and date correctly, the TE bit should not be used and the following sequence should be performed:

1) Delay at least 488µs after the last write to the RTC.
2) Read the time and date registers sequentially twice, saving the data.
3) Compare each value from the first read with the second. If the data does not match, repeat steps 2 and 3.