General Description

The MAX8792 pulse-width modulation (PWM) controller provides high efficiency, excellent transient response, and high DC-output accuracy needed for stepping down high-voltage batteries to generate low-voltage core or chipset/RAM bias supplies in notebook computers. The output voltage can be dynamically controlled using the dynamic REFIN, which supports input voltages between 0 to 2V. The REFIN adjustability combined with a resistive voltage-divider on the feedback input allows the MAX8792 to be configured for any output voltage between 0 to 0.9VIN.

Maxim’s proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios (low-duty-cycle applications) with ease and provides 100ns “instant-on” response to load transients while maintaining a relatively constant switching frequency. Strong drivers allow the MAX8792 to efficiently drive large synchronous-rectifier MOSFETs.

The controller senses the current across the synchronous rectifier to achieve a low-cost and highly efficient valley current-limit protection. The adjustable current-limit threshold provides a high degree of flexibility, allowing thermally compensated protection using an NTC or foldback current-limit protection using a voltage-divider derived from the output.

The MAX8792 includes a voltage-controlled soft-start and soft-shutdown in order to limit the input surge current, provide a monotonic power-up (even into a precharged output), and provide a predictable power-up time. The controller also includes output protection—undervoltage and overvoltage protection—as well as thermal-fault protection.

The MAX8792 is available in a tiny 14-pin, 3mm x 3mm TDFN package. For space-constrained applications, refer to the MAX17016 single step-down with 10A, 26V internal MOSFETs available in a small 40-pin, 6mm x 6mm TQFN package.

Features

- Quick-PWM with Fast Transient Response
- Supports Any Output Capacitor
- No Compensation Required with Polymers/Tantalum
- Stable with Ceramic Output Capacitors Using External Compensation
- Precision 2V ±10mV Reference
- Dynamically Adjustable Output Voltage (0 to 0.9VIN Range)
  Feedback Input Regulates to 0 to 2V REFIN Voltage
- 0.5% VOUT Accuracy Over Line and Load
- 26V Maximum Input Voltage Rating
- Adjustable Valley Current-Limit Protection
- Thermal Compensation with NTC
- Supports Foldback Current Limit
- Resistively Programmable Switching Frequency
- Overvoltage Protection
- Undervoltage/Thermal Protection
- Voltage Soft-Start and Soft-Shutdown
- Monotonic Power-Up with Precharged Output
- Power-Good Window Comparator

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>PIN-PACKAGE</th>
<th>PKG CODE</th>
<th>TOP MARK</th>
</tr>
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<tbody>
<tr>
<td>MAX8792ETD+T</td>
<td>14 TDFN - E P* 3mm x 3mm T1433-1 ADC</td>
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Note: This device is specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Applications

- Notebook Computers
- I/O and Chipset Supplies
- GPU Core Supply
- DDR Memory—VDDQ or VTT
- Point-of-Load Applications
- Step-Down Power Supply

Quick-PWM is a trademark of Maxim Integrated Products, Inc.
**Single Quick-PWM Step-Down Controller with Dynamic REFIN**

**ABSOLUTE MAXIMUM RATINGS**

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<thead>
<tr>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TON to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+28V</td>
<td></td>
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<tr>
<td>Vpp to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
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<tr>
<td>VCC to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
</tr>
<tr>
<td>EN, SKIP, PGOOD to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
</tr>
<tr>
<td>REF, REFIN to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
</tr>
<tr>
<td>ILIM, FB to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
</tr>
<tr>
<td>DL to GND</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
</tr>
<tr>
<td>BST to GND</td>
<td>(VDD - 0.3V)</td>
<td>(VDD - 0.3V)</td>
<td>+34V</td>
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</tr>
<tr>
<td>BST to LX</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+6V</td>
<td></td>
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<tr>
<td>BST to VDD</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>+28V</td>
<td></td>
</tr>
<tr>
<td>DH to LX</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>(VBST + 0.3V)</td>
<td></td>
</tr>
<tr>
<td>DH to LX</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>(VBST + 0.3V)</td>
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</tr>
<tr>
<td>DH to LX</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>(VBST + 0.3V)</td>
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</tr>
<tr>
<td>DH to LX</td>
<td>-0.3V</td>
<td>-0.3V</td>
<td>(VBST + 0.3V)</td>
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**ELECTRICAL CHARACTERISTICS**

(Circuit of Figure 1, VIN = 12V, VDD = VCC = VEN = 5V, REFIN = ILIM = REF, SKIP = GND, TA = 0°C to +85°C, unless otherwise specified. Typical values are at TA = +25°C.) (Note 1)

### PWM CONTROLLER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>VIN</td>
<td>VIN = 12V, VFB = 1.0V (Note 3)</td>
<td>RTON = 97.5kΩ (600kHz)</td>
<td>118</td>
<td>139</td>
<td>160</td>
</tr>
<tr>
<td>Quiescent Supply Current (VDD)</td>
<td>IDD + ICC</td>
<td>FB forced above REFIN</td>
<td>0.7</td>
<td>1.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current (VDD)</td>
<td>ISHDN</td>
<td>EN = GND, TA = +25°C</td>
<td>0.1</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VDD-to-VCC Resistance</td>
<td>RCC</td>
<td>20</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>On-Time</td>
<td>TON</td>
<td>VIN = 12V, VFB = 1.0V (Note 3)</td>
<td>RTON = 200kΩ (300kHz)</td>
<td>250</td>
<td>278</td>
<td>306</td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td>TOFF(MIN)</td>
<td>EN = GND, VTON = 26V, VCC = 0V or 5V, TA = +25°C</td>
<td>200</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TON Shutdown Supply Current</td>
<td>ITON</td>
<td>EN = GND, VTON = 26V, VCC = 0V or 5V, TA = +25°C</td>
<td>0.01</td>
<td>1</td>
<td>μA</td>
<td></td>
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<tr>
<td>REFIN Voltage Range</td>
<td>VREFIN</td>
<td>(Note 2)</td>
<td>0</td>
<td>VREF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB Voltage Range</td>
<td>VFB</td>
<td>(Note 2)</td>
<td>0</td>
<td>VREF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB Voltage Accuracy</td>
<td>VFB</td>
<td>VREFIN = 0.5V, measured at FB, VIN = 2V to 26V, SKIP = VDD</td>
<td>TA = +25°C</td>
<td>0.495</td>
<td>0.5</td>
<td>0.505</td>
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<tr>
<td></td>
<td></td>
<td>VREFIN = 1.0V</td>
<td>TA = 0°C to +85°C</td>
<td>0.995</td>
<td>1.0</td>
<td>1.005</td>
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<tr>
<td></td>
<td></td>
<td>VREFIN = 2.0V</td>
<td>TA = 0°C to +85°C</td>
<td>1.990</td>
<td>2.0</td>
<td>2.010</td>
</tr>
<tr>
<td>FB Input Bias Current</td>
<td>IFB</td>
<td>VFB = 0.5V to 2.0V, TA = +25°C</td>
<td>-0.1</td>
<td>+0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Load-Regulation Error</td>
<td>ILoad</td>
<td>ILOAD = 0 to 3A, SKIP = VDD</td>
<td>0.1</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Line-Regulation Error</td>
<td>ICC</td>
<td>VCC = 4.5V to 5.5V, VIN = 4.5V to 26V</td>
<td>0.25</td>
<td></td>
<td>%</td>
<td></td>
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<tr>
<td>Soft-Start/Stop Slew Rate</td>
<td>tSS</td>
<td>Rising/falling edge on EN</td>
<td>1</td>
<td></td>
<td>mV/μs</td>
<td></td>
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<tr>
<td>Dynamic REFIN Slew Rate</td>
<td>tDYN</td>
<td>Rising edge on REFIN</td>
<td>8</td>
<td></td>
<td>mV/μs</td>
<td></td>
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**REFERENCE**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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</thead>
<tbody>
<tr>
<td>Reference Voltage</td>
<td>VREF</td>
<td>VCC = 4.5V to 5.5V</td>
<td>1.990</td>
<td>2.00</td>
<td>2.010</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IREF = -10μA to +50μA</td>
<td>1.98</td>
<td></td>
<td>2.02</td>
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</table>
### ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. \(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, \text{REFIN} = \text{ILIM} = \text{REF}, \text{SKIP} = \text{GND}. T_A = 0°C \text{ to } +85°C, \) unless otherwise specified. Typical values are at \(T_A = +25°C\).) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td><strong>FAULT DETECTION</strong></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Output Overvoltage-Protection Trip Threshold</td>
<td>OVP</td>
<td>With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV</td>
<td>250</td>
<td>300</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dynamic transition</td>
<td>(V_{REF} + 0.30)</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Minimum OVP threshold</td>
<td>0.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Overvoltage Fault-Propagation Delay</td>
<td>(t_{OVP})</td>
<td>FB forced 25mV above trip threshold</td>
<td>5</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td>Output Undervoltage-Protection Trip Threshold</td>
<td>UVP</td>
<td>With respect to the internal target voltage (error comparator threshold); falling edge; hysteresis = 50mV</td>
<td>-240</td>
<td>-200</td>
<td>-160</td>
<td>mV</td>
</tr>
<tr>
<td>Output Undervoltage Fault-Propagation Delay</td>
<td>(t_{UVP})</td>
<td>FB forced 25mV below trip threshold</td>
<td>100</td>
<td>200</td>
<td>350</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>PGOOD Propagation Delay</td>
<td>(t_{PGOOD})</td>
<td>UVP falling edge, 25mV overdrive</td>
<td>5</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OVP rising edge, 25mV overdrive</td>
<td>5</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Startup delay</td>
<td>100</td>
<td>200</td>
<td>350</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>PGOOD Output-Low Voltage</td>
<td>(I_{SINK})</td>
<td>(3mA)</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>PGOOD Leakage Current</td>
<td>(I_{PGOOD})</td>
<td>FB = \text{REFIN} (PGOOD high impedance), PGOOD forced to 5V, (T_A = +25°C)</td>
<td>1</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Dynamic REFIN Transition Fault Blanking Threshold</td>
<td></td>
<td>Fault blanking initiated; REFIN deviation from the internal target voltage (error comparator threshold); hysteresis = 10mV</td>
<td>±50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Thermal-Shutdown Threshold</td>
<td>(T_{SHDN})</td>
<td>Hysteresis = 15°C</td>
<td>160</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>(V_{CC}) Undervoltage Lockout Threshold</td>
<td>(V_{U(VLO(VCC))})</td>
<td>Rising edge, PWM disabled below this level; hysteresis = 100mV</td>
<td>3.95</td>
<td>4.2</td>
<td>4.45</td>
<td>V</td>
</tr>
<tr>
<td><strong>CURRENT LIMIT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIM Input Range</td>
<td>(V_{ILIMIT})</td>
<td>(0.4V)</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Current-Limit Threshold</td>
<td>(V_{ILIMIT})</td>
<td>(0.4V)</td>
<td>18</td>
<td>20</td>
<td>22</td>
<td>mV</td>
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<tr>
<td>Current-Limit Threshold (Negative)</td>
<td>(V_{INEG})</td>
<td>(0.4V)</td>
<td>92</td>
<td>100</td>
<td>108</td>
<td>mV</td>
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<tr>
<td>Current-Limit Threshold (Zero Crossing)</td>
<td>(V_{ZX})</td>
<td>(0.4V); (V_{GND} - V_{LX}, \text{SKIP} = \text{GND or open})</td>
<td>-24</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Ultrasonic Frequency</td>
<td></td>
<td>(3.3V); (V_{FB} = V_{REFIN} + 50mV)</td>
<td>18</td>
<td>30</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Ultrasonic Current-Limit Threshold</td>
<td>(\text{SKIP} = \text{open (3.3V)}); (V_{FB} = V_{REFIN} + 50mV)</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>
Single Quick-PWM Step-Down Controller with Dynamic REFIN

ELECTRICAL CHARACTERISTICS (continued)
(Circuit of Figure 1, \( V_{IN} = 12V, \ V_{DD} = \ V_{CC} = \ V_{EN} = 5V, \ \text{REFIN} = \ \text{ILIM} = \ \text{REF}, \ \text{SKIP} = \ \text{GND}, \ \text{T}_{A} = 0^\circ \text{C} \text{ to } +85^\circ \text{C}, \) unless otherwise specified. Typical values are at \( \text{T}_{A} = +25^\circ \text{C}. \) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>GATE DRIVERS</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>DH Gate Driver On-Resistance</td>
<td>( R_{ON(DH)} )</td>
<td>Low state (pulldown)</td>
<td>1.2</td>
<td>3.5</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High state (pullup)</td>
<td>1.2</td>
<td>3.5</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>DL Gate Driver On-Resistance</td>
<td>( R_{ON(DL)} )</td>
<td>High state (pullup)</td>
<td>1.7</td>
<td>4</td>
<td></td>
<td>( \Omega )</td>
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<tr>
<td></td>
<td></td>
<td>Low state (pulldown)</td>
<td>0.9</td>
<td>2</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>DH Gate Driver Source/Sink Current</td>
<td>( I_{DH} )</td>
<td>DH forced to 2.5V, BST - LX forced to 5V</td>
<td>1.5</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>DL Gate Driver Source Current</td>
<td>( I_{DL(SOURCE)} )</td>
<td>DL forced to 2.5V</td>
<td>1</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>DL Gate Driver Sink Current</td>
<td>( I_{DL(SINK)} )</td>
<td>DL forced to 2.5V</td>
<td>2.4</td>
<td></td>
<td></td>
<td>A</td>
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<tr>
<td>Driver Propagation Delay</td>
<td></td>
<td>DL low to DH high</td>
<td>10</td>
<td>25</td>
<td></td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>DL low to DH high</td>
<td>15</td>
<td>35</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DL Transition Time</td>
<td></td>
<td>DL falling, ( C_{DL} = 3nF )</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DL rising, ( C_{DL} = 3nF )</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DH Transition Time</td>
<td></td>
<td>DH falling, ( C_{DH} = 3nF )</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DH rising, ( C_{DH} = 3nF )</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Internal BST Switch On-Resistance</td>
<td>( R_{BST} )</td>
<td>( I_{BST} = 10mA, \ V_{DD} = 5V )</td>
<td>4</td>
<td>7</td>
<td></td>
<td>( \Omega )</td>
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</tbody>
</table>

INPUTS AND OUTPUTS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>EN Logic-Input Threshold</td>
<td>( V_{EN} )</td>
<td>EN rising edge, hysteresis = 450mV (typ)</td>
<td>1.20</td>
<td>1.7</td>
<td>2.20</td>
<td>V</td>
</tr>
<tr>
<td>EN Logic-Input Current</td>
<td>( I_{EN} )</td>
<td>EN forced to GND or ( V_{DD}, \ T_{A} = +25^\circ \text{C} )</td>
<td>-0.5</td>
<td>+0.5</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>SKIP Quad-Level Input Logic Levels</td>
<td>( V_{\text{SKIP}} )</td>
<td>High (5V ( V_{DD} ))</td>
<td>( V_{CC} - 0.4 )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mid (3.3V)</td>
<td>3.0</td>
<td>3.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ref (2.0V)</td>
<td>1.7</td>
<td>2.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low (GND)</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SKIP Logic-Input Current</td>
<td>( I_{\text{SKIP}} )</td>
<td>SKIP forced to GND or ( V_{DD} )</td>
<td>-2</td>
<td>+2</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS
(Circuit of Figure 1, \( V_{IN} = 12V, \ V_{DD} = \ V_{CC} = \ V_{EN} = 5V, \ \text{REFIN} = \ \text{ILIM} = \ \text{REF}, \ \text{SKIP} = \ \text{GND}, \ \text{T}_{A} = -40^\circ \text{C} \text{ to } +85^\circ \text{C}, \) unless otherwise specified.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>PWM CONTROLLER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>( V_{IN} )</td>
<td></td>
<td>2</td>
<td>26</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Supply Current (( V_{DD} ))</td>
<td>( IDD + ICC )</td>
<td>FB forced above ( \text{REFIN} )</td>
<td>1.2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>On-Time</td>
<td>( I_{ON} )</td>
<td>( V_{IN} = 12V, \ V_{FB} = 1.0V ) (Note 3)</td>
<td>( R_{TON} = 97.5k\Omega ) (600kHz)</td>
<td>115</td>
<td>163</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( R_{TON} = 200k\Omega ) (300kHz)</td>
<td>250</td>
<td>306</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( R_{TON} = 302.5k\Omega ) (200kHz)</td>
<td>348</td>
<td>486</td>
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</table>
### ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, \( V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, \) \( REF = ILIM, SKIP = GND, T_A = -40^\circ C \) to \(+85^\circ C, \) unless otherwise specified.) \( \text{Note 1} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Off-Time</td>
<td>( t_{OFF(MIN)} )</td>
<td>(Note 3)</td>
<td>350</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>REF(\text{FIN Voltage Range} )</td>
<td>( V_{REFIN} )</td>
<td>(Note 2)</td>
<td>0</td>
<td>( V_{REF} )</td>
<td></td>
</tr>
<tr>
<td>FB Voltage Range</td>
<td>( V_{FB} )</td>
<td>(Note 2)</td>
<td>0</td>
<td>( V_{REF} )</td>
<td></td>
</tr>
<tr>
<td>FB Voltage Accuracy</td>
<td>( V_{FB} )</td>
<td>Measured at FB, ( V_{IN} = 2V ) to 26V, ( SKIP = V_{DD} )</td>
<td>( V_{REFIN} = 0.5V )</td>
<td>0.49</td>
<td>0.51</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{REFIN} = 1.0V )</td>
<td>0.99</td>
<td>1.01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V_{REFIN} = 2.0V )</td>
<td>1.985</td>
<td>2.015</td>
</tr>
</tbody>
</table>

| REFERENCE | Reference Voltage | \( V_{REF} \) | \( V_{CC} = 4.5V \) to 5.5V | 1.985 | 2.015 | V |

### FAULT DETECTION

| Output Overvoltage-Protection | Trip Threshold | OVP | With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV | 250 | 350 | mV |
| Output Undervoltage-Protection | Trip Threshold | UVP | With respect to the internal target voltage (error comparator threshold); falling edge; hysteresis = 50mV | -240 | -160 | mV |
| Output Undervoltage | Fault-Propagation Delay | \( t_{UVP} \) | FB forced 25mV below trip threshold | 80 | 400 | \( \mu \)s |
| PGOOD Output Low Voltage | | \( I_{SINK} = 3mA \) | | 0.4 | V |

### CURRENT LIMIT

| ILIM Input Range | \( V_{ILIMIT} \) | \( V_{ILIMIT} = 0.4V \) | 17 | 23 | mV |
| Current-Limit Threshold | | \( ILIM = REF (2.0V) \) | 90 | 110 |
| Ultrasonic Frequency | \( SKIP = \) open (3.3V); \( V_{FB} = V_{REFIN} + 50mV \) | 17 | kHz |

### GATE DRIVERS

| DH Gate Driver On-Resistance | \( R_{ON(DH)} \) | BST - LX forced to 5V | Low state (pulldown) | 3.5 | \( \Omega \) |
| | | | High state (pullup) | 3.5 |
| DL Gate Driver On-Resistance | \( R_{ON(DL)} \) | High state (pullup) | | 4 | \( \Omega \) |
| | | Low state (pulldown) | | 2 |
| Internal BST Switch On-Resistance | \( R_{BST} \) | \( IBST = 10mA, V_{DD} = 5V \) | | 7 | \( \Omega \) |
Single Quick-PWM Step-Down Controller with Dynamic REFIN

ELECTRICAL CHARACTERISTICS (continued)
(Circuit of Figure 1, \( V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, \) REFIN = ILIM = REF, \( V_{SKIP} = GND, \) \( T_A = -40^\circ C \) to \( +85^\circ C, \) unless otherwise specified.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN Logic-Input Threshold</td>
<td>( V_{EN} )</td>
<td>EN rising edge; hysteresis = 450mV (typ)</td>
<td>1.20</td>
<td>2.20</td>
<td>V</td>
</tr>
<tr>
<td>( V_{skip} ) Quad-Level Input Logic Levels</td>
<td></td>
<td>High (5V ( V_{DD} ))</td>
<td>( V_{CC} - 0.4 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mid (3.3V)</td>
<td>3.0</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ref (2.0V)</td>
<td>1.7</td>
<td>2.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low (GND)</td>
<td>1.0</td>
<td>0.4</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Limits are 100% production tested at \( T_A = +25^\circ C. \) Maximum and minimum limits over temperature are guaranteed by design and characterization.

Note 2: The 0 to 0.5V range is guaranteed by design, not production tested.

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, \( V_{BST} = 5V, \) and a 250pF capacitor connected from DH to LX. Actual in-circuit times can differ due to MOSFET switching speeds.

Typical Operating Characteristics
(MAX8792 Circuit of Figure 1, \( V_{IN} = 12V, V_{DD} = 5V, V_{SKIP} = GND, R_{TON} = 200k\Omega, T_A = +25^\circ C, \) unless otherwise noted.)

**1.5V OUTPUT EFFICIENCY vs. LOAD CURRENT**

**1.5V OUTPUT EFFICIENCY vs. LOAD CURRENT**

**1.5V OUTPUT VOLTAGE vs. LOAD CURRENT**
**Single Quick-PWM Step-Down Controller with Dynamic REFIN**

**Typical Operating Characteristics (continued)**

(MAX8792 Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = 5V$, $\text{SKIP} = \text{GND}$, $R_{TON} = 200\, \Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

1. **0.5V Output Efficiency vs. Load Current**
2. **0.5V Output Efficiency vs. Load Current**
3. **0.5V Output Voltage vs. Load Current**
4. **Switching Frequency vs. Load Current**
5. **PWM Mode Switching Frequency vs. Input Voltage**
6. **Switching Frequency vs. Temperature**
7. **Maximum Output Current vs. Input Voltage**
8. **Maximum Output Current vs. Temperature**
9. **No-Load Supply Current $I_{BIAS}$ vs. Input Voltage**
Single Quick-PWM Step-Down Controller with Dynamic REFIN

Typical Operating Characteristics (continued)
(MAX8792 Circuit of Figure 1, VIN = 12V, VDD = 5V, SKIP = GND, RTON = 200kΩ, TA = +25°C, unless otherwise noted.)

NO-LOAD SUPPLY CURRENT IIN vs. INPUT VOLTAGE

REF OUTPUT VOLTAGE vs. LOAD CURRENT

REFIN-TO-FB OFFSET VOLTAGE DISTRIBUTION

SAMPLE SIZE = 100

20V ILIM THRESHOLD VOLTAGE DISTRIBUTION

SAMPLE SIZE = 100

SOFT-START WAVEFORM (HEAVY LOAD)

LOAD-TRANSIENT RESPONSE (PWM MODE)

200μs/div

LOAD-TRANSIENT RESPONSE (SKIP MODE)

200μs/div
**Single Quick-PWM Step-Down Controller with Dynamic REFIN**

Typical Operating Characteristics (continued)

(MAX8792 Circuit of Figure 1, VIN = 12V, VDD = 5V, SKIP = GND, RTON = 200kΩ, TA = +25°C, unless otherwise noted.)
### Single Quick-PWM Step-Down Controller with Dynamic REFIN

#### Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EN</td>
<td>Shutdown Control Input. Connect to VDD for normal operation. Pull EN low to place the controller into its 2μA shutdown state. When disabled, the MAX8792 slowly ramps down the target/output voltage to ground and after the target voltage reaches 0.1V, the controller forces both DH and DL low and enters the low-power shutdown state. Toggle EN to clear the fault-protection latch.</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass VDD to power ground with a 1μF or greater ceramic capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>DL</td>
<td>Low-Side Gate Driver. DL swings from GND to VDD. The controller pulls DL high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. The MAX8792 forces DL low during VCC UVLO and REFOK lockout conditions.</td>
</tr>
<tr>
<td>4</td>
<td>LX</td>
<td>Inductor Connection. Connect LX to the switched side of the inductor as shown in Figure 1.</td>
</tr>
<tr>
<td>5</td>
<td>DH</td>
<td>High-Side Gate Driver. DH swings from LX to BST. The MAX8792 pulls DH low whenever the controller is disabled.</td>
</tr>
<tr>
<td>6</td>
<td>BST</td>
<td>Boost Flying-Capacitor Connection. Connect to an external 0.1μF 6V capacitor as shown in Figure 1. The MAX8792 contains an internal boost switch/diode (see Figure 2).</td>
</tr>
</tbody>
</table>
| 7   | TON  | Switching Frequency-Setting Input. An external resistor between the input power source and TON sets the switching period (TSW = 1/fSW) according to the following equation:

\[
T_{SW} = C_{TON} \left( R_{TON} + 6.5kΩ \right) \left( \frac{V_{FB}}{V_{OUT}} \right)
\]

where \( C_{TON} = 16.26pF \) and \( V_{FB} = V_{REFIN} \) under normal operating conditions. If the TON current drops below 10μA, the MAX8792 shuts down, and enters a high-impedance state. TON is high impedance in shutdown. |
| 8   | FB   | Feedback Voltage-Sense Connection. Connect directly to the positive terminal of the output capacitors for output voltages less than 2V as shown in Figure 1. For fixed-output voltages greater than 2V, connect REFIN to REF and use a resistive divider to set the output voltage (Figure 4). FB senses the output voltage to determine the on-time for the high-side switching MOSFET. |
| 9   | ILIM | Current-Limit Threshold Adjustment. The current-limit threshold is 0.05 times (1/20) the voltage at ILIM. Connect ILIM to a resistive divider (from REF) to set the current-limit threshold between 20mV and 100mV (with 0.4V to 2V at ILIM). |
| 10  | REFIN| External Reference Input. REFIN sets the feedback regulation voltage (\( V_{FB} = V_{REFIN} \)) of the MAX8792 using the resistor-divider connected between REF and GND. The MAX8792 includes an internal window comparator to detect REFIN voltage transitions, allowing the controller to blank PGOOD and the fault protection. |
| 11  | REF  | 2V Reference Voltage. Bypass to analog ground using a 470pF to 10nF ceramic capacitor. The reference can source up to 50μA for external loads. |
| 12  | SKIP | Pulse-Skipping Control Input. This four-level input determines the mode of operation under normal steady-state conditions and dynamic output-voltage transitions:

- VDD (5V) = forced-PWM operation.
- REF (2V) = pulse-skipping mode with forced-PWM during transitions.
- Open (3.3V) = ultrasonic mode (without forced-PWM during transitions).
- GND = pulse-skipping mode (without forced-PWM during transitions). |
| 13  | VCC  | 5V Analog Supply Voltage. Internally connected to VDD through an internal 20Ω resistor. Bypass VCC to analog ground using a 1μF ceramic capacitor. |
Standard Application Circuits
The MAX8792 standard application circuit (Figure 1) generates a 1.5V or 1.05V output rail for general-purpose use in a notebook computer. See Table 1 for component selections. Table 2 lists the component manufacturers.
Single Quick-PWM Step-Down Controller with Dynamic REFIN

Detailed Description

The MAX8792 step-down controller is ideal for the low-duty-cycle (high-input voltage to low-output voltage) applications required by notebook computers. Maxim’s proprietary Quick-PWM pulse-width modulator in the MAX8792 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency, current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time (regardless of input voltage) PFM control schemes.

+5V Bias Supply (VCC/VDD)

The MAX8792 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook’s main 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615. The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is determined by:

\[ I_{BIAS} = I_Q + f_{SWQG} = 2mA \text{ to } 20mA \text{ (typ)} \]

Table 1. Component Selection for Standard Applications

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>VOUT = 1.5V/1.05V AT 10A (Figure 1)</th>
<th>VOUT = 3.3V AT 5A (Figure 4)</th>
<th>VOUT = 1.5V AT 10A/1.05V AT 7A (Figure 7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN = 7V to 20V</td>
<td>RTON = 200kΩ (300kHz)</td>
<td>VIN = 7V to 20V</td>
<td>RTON = 100kΩ (600kHz)</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>(2x) 330μF, 6mΩ Panasonic EEFX0D331XR</td>
<td>(1x) 330μF, 18mΩ SANYO 4TPE330MI</td>
<td>(2x) 330μF, 7mΩ NEC-TOKIN PSGD0E337M7</td>
</tr>
<tr>
<td>Inductor</td>
<td>1.0μH, 3.25mΩ Würth 744 3552 100</td>
<td>3.3μH, 14mΩ NEC-TOKIN MPLC1040L3R3</td>
<td>0.68μH, 4.6mΩ Coiltronics FP3-R68</td>
</tr>
<tr>
<td>High-Side MOSFET</td>
<td>Fairchild (1x) FDS8690 8.6mΩ/11.4mΩ (typ/max)</td>
<td>Siliconix (1x) Si4916DY N\text{H} = 18mΩ/22mΩ (typ/max)</td>
<td>Fairchild (1x) FDS8690 8.6mΩ/11.4mΩ (typ/max)</td>
</tr>
<tr>
<td>Low-Side MOSFET</td>
<td>Fairchild (1x) FDS8670 4.2mΩ/5.0mΩ (typ/max)</td>
<td>N\text{L} = 15mΩ/18mΩ (typ/max)</td>
<td>Fairchild (1x) FDS8670 4.2mΩ/5.0mΩ (typ/max)</td>
</tr>
</tbody>
</table>

Table 2. Component Suppliers

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>WEBSITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVX Corp.</td>
<td><a href="http://www.avxcorp.com">www.avxcorp.com</a></td>
</tr>
<tr>
<td>BI Technologies</td>
<td><a href="http://www.bitechnologies.com">www.bitechnologies.com</a></td>
</tr>
<tr>
<td>Central Semiconductor Corp.</td>
<td><a href="http://www.centralsemi.com">www.centralsemi.com</a></td>
</tr>
<tr>
<td>Coiltronics</td>
<td><a href="http://www.cooperet.com">www.cooperet.com</a></td>
</tr>
<tr>
<td>Fairchild Semiconductor</td>
<td><a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a></td>
</tr>
<tr>
<td>International Rectifier</td>
<td><a href="http://www.irf.com">www.irf.com</a></td>
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<td>KEMET Corp.</td>
<td><a href="http://www.kemet.com">www.kemet.com</a></td>
</tr>
<tr>
<td>NEC TOKIN America, Inc.</td>
<td><a href="http://www.nec-tokin.com">www.nec-tokin.com</a></td>
</tr>
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<td>Panasonic Corp.</td>
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<td>Pulse Engineering</td>
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<td>Renesas Technology Corp.</td>
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<tr>
<td>SANYO Electric Co., Ltd.</td>
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</tr>
<tr>
<td>Siliconix (Vishay)</td>
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</tr>
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<td>Sumida Corp.</td>
<td><a href="http://www.sumida.com">www.sumida.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
<tr>
<td>TDK Corp.</td>
<td><a href="http://www.component.tdk.com">www.component.tdk.com</a></td>
</tr>
<tr>
<td>TOKO America, Inc.</td>
<td><a href="http://www.tokoam.com">www.tokoam.com</a></td>
</tr>
<tr>
<td>Würth Electronik GmbH &amp; Co. KG</td>
<td><a href="http://www.we-online.com">www.we-online.com</a></td>
</tr>
</tbody>
</table>

+5V Bias Supply (VCC/VDD)

The MAX8792 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook’s main 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615. The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is determined by:

\[ I_{BIAS} = I_Q + f_{SWQG} = 2mA \text{ to } 20mA \text{ (typ)} \]
Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor’s ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to

Figure 2. MAX8792 Functional Diagram
**Single Quick-PWM Step-Down Controller with Dynamic REFIN**

input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (200ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

**On-Time One-Shot**

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to input and output voltage. The high-side switch on-time is inversely proportional to the input voltage as sensed by the TON input, and proportional to the feedback voltage as sensed by the FB input:

\[
\text{On-Time (tON)} = \frac{\text{TON}(\text{FB}/\text{VIN})}{\text{VSW}}
\]

where \(T_{SW}\) (switching period) is set by the resistance \((R_{TON})\) between TON and VIN. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. Connect a resistor \((R_{TON})\) between TON and VIN to set the switching period \(T_{SW} = 1/f_{SW}\):

\[
T_{SW} = C_{TON}(R_{TON} + 6.5k\Omega)
\left(\frac{V_{FB}}{V_{OUT}}\right)
\]

where \(C_{TON} = 16.26\mu\text{F}\). When used with unity-gain feedback \((V_{OUT} = V_{FB})\), a 96.75k\Omega to 303.25k\Omega corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

\[
t_{SW} = \frac{(V_{OUT} + V_{DIS})}{V_{TON}(V_{IN} + V_{DIS} - V_{CHG})}
\]

where \(V_{DIS}\) is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; \(V_{CHG}\) is the sum of the parasitic voltage drops in the charging path, including the high-side switch, inductor, and PCB resistances; and \(V_{TON}\) is the on-time calculated by the MAX8792.

**Power-Up Sequence (POR, UVLO)**

The MAX8792 is enabled when EN is driven high and the 5V bias supply \((V_{DD})\) is present. The reference powers up first. Once the reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 50\mu s one-shot delay in order to allow the bias circuitry and analog blocks enough time to settle to their proper states. With the control circuitry reliably powered up, the PWM controller may begin switching.

Power-on reset (POR) occurs when \(V_{CC}\) rises above approximately 3V, resetting the fault latch and preparing the controller for operation. The \(V_{CC}\) UVLO circuitry inhibits switching until \(V_{CC}\) rises above 4.25V. The controller powers up the reference once the system enables the controller, \(V_{CC}\) exceeds 4.25V, and EN is driven high. With the reference in regulation, the controller ramps the output voltage to the target REFIN voltage with a 1mV/\mu s slew rate:

\[
t_{START} = \frac{V_{FB}}{1mV/\mu s} = \frac{V_{FB}}{1V/ms}
\]

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PGOOD becomes high impedance immediately. PGOOD becomes high impedance approximately 200\mu s after the target REFIN voltage has been reached. The MAX8792 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown, regardless of the \(\text{SKIP}\) configuration.

For automatic startup, the battery voltage should be present before \(V_{CC}\). If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling EN or cycling the \(V_{CC}\) power supply below 0.5V.

If the \(V_{CC}\) voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from over-voltage faults, the controller shuts down immediately and forces a high-impedance output (DL and DH pulled low).

**Shutdown**

When the system pulls EN low, the MAX8792 enters low-power shutdown mode. PGOOD is pulled low immediately, and the output voltage ramps down with a 1mV/\mu s slew rate:

\[
t_{SHDN} = \frac{V_{FB}}{1mV/\mu s} = \frac{V_{FB}}{1V/ms}
\]
Slowly discharging the output capacitors by slewing the output over a long period of time (typically 0.5ms to 2ms) keeps the average negative inductor current low (damped response), thereby preventing the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX8792 shuts down completely—the drivers are disabled (DL and DH pulled low)—the reference turns off, and the supply currents drop to about 0.1μA (typ).

When a fault condition—output UVP or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle EN or cycle VCC power below 0.5V.

The MAX8792 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown, regardless of the SKIP configuration.

**Modes of Operation**

**Forced-PWM Mode** \((\text{SKIP} = \text{VDD})\)

The low-noise, forced-PWM mode \((\text{SKIP} = \text{VDD})\) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of \(V_{OUT}/V_{IN}\). The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 10mA to 50mA, depending on the switching frequency.

The MAX8792 automatically always uses forced-PWM operation during shutdown, regardless of the SKIP configuration.

**Automatic Pulse-Skipping Mode** \((\text{SKIP} = \text{GND or 2V})\)

In skip mode \((\text{SKIP} = \text{GND or 2V})\), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current’s zero crossing. The zero-crossing comparator threshold is set by the differential across \(L_X\) to GND.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX8792 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction \((\text{SKIP} = \text{GND} \text{ and } I_{OUT} < I_{LOAD} (\text{SKIP}))\), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

When SKIP is pulled to GND, the MAX8792 remains in pulse-skipping mode. Since the output is not able to sink current, the timing for negative dynamic output-voltage transitions depends on the load current and output capacitance. Letting the output voltage drift down is typically recommended in order to reduce the potential for audible noise since this eliminates the input current surge during negative output-voltage transitions.

**Ultrasonic Mode** \((\text{SKIP} = \text{Open} = 3.3\text{V})\)

Leaving SKIP unconnected activates a unique pulse-skipping mode with a minimum switching frequency of 18kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point \((I_{LOAD} (\text{SKIP}))\) that occurs when normally pulse skipping.

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 33μs. Once triggered, the ultrasonic controller pulls DL high, turning on the low-side MOSFET to induce a negative inductor current (Figure 3). After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low).
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and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equation:

\[ V_{\text{VISONIC}} = L_{\text{RCS}} = (V_{\text{REFIN}} - V_{\text{FB}}) \times 0.7 \]

where \( V_{\text{FB}} > V_{\text{REFIN}} \) and \( R_{\text{CS}} \) is the current-sense resistance seen across GND to LX.

Valley Current-Limit Protection

The current-limit circuit employs a unique “valley” current-sensing algorithm that senses the inductor current through the low-side MOSFET. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX8792 also implements a negative current limit to prevent excessive reverse inductor currents when \( V_{\text{OUT}} \) is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

Integrated Output Voltage

The MAX8792 regulates the valley of the output ripple, so the actual DC output voltage is higher than the slope-compensated target by 50% of the output ripple voltage. Under steady-state conditions, the MAX8792’s internal integrator corrects for this 50% output ripple-voltage error, resulting in an output voltage that is accurately defined by the following equation:

\[ V_{\text{FB}} = V_{\text{REFIN}} + \left( \frac{V_{\text{RIPPLE}}}{A_{\text{CCV}}} \right) \]

where \( V_{\text{REFIN}} \) is the nominal feedback voltage, \( A_{\text{CCV}} \) is the integrator’s gain, and \( V_{\text{RIPPLE}} \) is the feedback ripple voltage (\( V_{\text{RIPPLE}} = \text{ESR} \times \Delta \text{INDUCTOR} \) as described in the Output Capacitor Selection section). Therefore, the feedback-voltage accuracy specification provided in the Electrical Characteristics table actually refers to the integrated feedback threshold and primarily reflects the offset voltage of the integrator amplifier.

Dynamic Output Voltages

The MAX8792 regulates FB to the voltage set at REFIN. By changing the voltage at REFIN (Figure 1), the MAX8792 can be used in applications that require dynamic output-voltage changes between two set points. For a step-voltage change at REFIN, the rate of change of the output voltage is limited either by the internal 8mV/μs slew-rate circuit or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is slower. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate. Additional load current slows down the output voltage change during a positive REFIN voltage change, and speeds up the output voltage change during a negative REFIN voltage change.
Output Voltages Greater than 2V

Although REFIN is limited to a 0 to 2V range, the output-voltage range is unlimited since the MAX8792 utilizes a high-impedance feedback input (FB). By adding a resistive voltage-divider from the output to FB to analog ground (Figure 4), the MAX8792 supports output voltages above 2V. However, the controller also uses FB to determine the on-time, so the voltage-divider influences the actual switching frequency, as detailed in the On-Time One-Shot section.

Internal Integration

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This internal amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the compensated feedback ripple voltage and internal slope-compensation variation. The integrator amplifier has the ability to shift the output voltage by ±55mV (typ).

The MAX8792 disables the integrator by connecting the amplifier inputs together at the beginning of all downward REFIN transitions done in pulse-skipping mode. The integrator remains disabled until 20μs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and over-voltage conditions. PGOOD is actively held low in shutdown (EN = GND), during soft-start, and soft-shutdown. Approximately 200μs (typ) after the soft-start terminates, PGOOD becomes high impedance as long as the feedback voltage is above the UVP threshold (REFIN - 200mV) and below the OVP threshold (REFIN + 300mV). PGOOD goes low if the feedback voltage drops 200mV below the target voltage (REFIN) or rises 300mV above the target voltage (REFIN), or the SMPS controller is shut down. For a logic-level PGOOD output
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Overvoltage Protection (OVP)
When the internal feedback voltage rises 300mV above the target voltage and OVP is enabled, the OVP comparator immediately pulls DH low and forces DL high, pulls PGOOD low, sets the fault latch, and disables the SMPS controller. Toggle EN or cycle VCC power below the VCC POR to clear the fault latch and restart the controller.

Undervoltage Protection (UVP)
When the feedback voltage drops 200mV below the target voltage (REFIN), the controller immediately pulls PGOOD low and triggers a 200μs one-shot timer. If the feedback voltage remains below the undervoltage fault threshold for the entire 200μs, then the undervoltage fault latch is set and the SMPS begins the shutdown sequence. When the internal target voltage drops below 0.1V, the MAX8792 forces DL low. Toggle EN or cycle VCC power below VCC POR to clear the fault latch and restart the controller.

Thermal-Fault Protection (TSHDN)
The MAX8792 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down the controller. Both DL and DH are pulled low. Toggle EN or cycle VCC power below VCC POR to reactivate the controller after the junction temperature cools by 15°C.

MOSFET Gate Drivers
The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large VIN - VOUT differential exists. The high-side gate driver (DH) sources and sinks 1.5A, and the low-side gate driver (DL) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH high-side MOSFET driver is powered by the internal boost switch charge pump from BST to LX, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply (VDD).
Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8792 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1 in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.9Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to VIN. Applications with high-input voltages and long inductive driver traces may require rising LX edges do not pull up the low-side MOSFETs’ gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET’s gate-to-drain capacitance (C\text{rss}), gate-to-source capacitance (C\text{iss} - C\text{rss}), and additional board parasitics should not exceed the following minimum threshold:

\[ V_{GS(TH)} > V_{IN} \left( \frac{C_{RSS}}{C_{ISS}} \right) \]

Typically, adding a 4700pF between DL and power ground (CNL in Figure 6), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (RBST in Figure 6). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

**Quick-PWM Design Procedure**

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value (V\text{IN(MAX)}) must accommodate the worst-case input supply voltage allowed by the notebook’s AC adapter voltage. The minimum value (V\text{IN(MIN)}) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

- **Maximum load current:** There are two values to consider. The peak load current (I\text{LOAD(MAX)}) determines the instantaneous component stresses and filtering requirements, and thus drives output...
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capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The
continuous load current (ILOAD) determines the thermal stresses and thus drives the selection of input
 capacitors, MOSFETs, and other critical heat-contributing components. Most notebook loads generally
exhibit ILOAD = ILOAD(MAX) x 80%.

• Switching frequency: This choice determines the basic trade-off between size and efficiency. The
 optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that
 are proportional to frequency and VIN^2. The optimum frequency is also a moving target, due to
 rapid improvements in MOSFET technology that are making higher frequencies more practical.

• Inductor operating point: This choice provides
 trade-offs between size vs. efficiency and transient
 response vs. output noise. Low inductor values pro-
 vide better transient response and smaller physical
 size, but also result in lower efficiency and higher
 output noise due to increased ripple current. The
 minimum practical inductor value is one that causes
 the circuit to operate at the edge of critical conduc-
tion (where the inductor current just touches zero
 with every cycle at maximum load). Inductor values
 lower than this grant no further size-reduction bene-
 fit. The optimum operating point is usually found
 between 20% and 50% ripple current.

**Inductor Selection**
The switching frequency and operating point (% ripple
 current or LIR) determine the inductor value as follows:

\[
L = \left(\frac{V_{IN} - V_{OUT}}{SW \cdot ILOAD(MAX) \cdot LIR}\right) \cdot \frac{V_{OUT}}{V_{IN}}
\]

Find a low-loss inductor having the lowest possible DC
resistance that fits in the allotted dimensions. Ferrite
cores are often the best choice, although powdered
iron is inexpensive and can work well at 200kHz. The
core must be large enough not to saturate at the peak
inductor current (IPEAK):

\[
I_{PEAK} = ILOAD(MAX) + \frac{\Delta L}{2}
\]

**Transient Response**
The inductor ripple current impacts transient-response
performance, especially at low VIN - VOUT differentials.
Low inductor values allow the inductor current to slew
faster, replenishing charge removed from the output fil-
ter capacitors by a sudden load step. The amount of
output sag is also a function of the maximum duty factor,
which can be calculated from the on-time and minimum
off-time. The worst-case output sag voltage can be
determined by:

\[
V_{SAG} = \frac{L(\Delta ILOAD(MAX))^2}{2COUT \cdot VOUT} \left[\left(\frac{V_{OUT} \cdot TSW}{V_{IN}}\right) + t_{OFF(MIN)}\right]
\]

where t_{OFF(MIN)} is the minimum off-time (see the Electrical
Characteristics table).

The amount of overshoot due to stored inductor energy
when the load is removed can be calculated as:

\[
V_{SOAR} = \frac{(\Delta ILOAD(MAX))^2 L}{2COUT \cdot VOUT}
\]

**Setting the Valley Current Limit**
The minimum current-limit threshold must be high
 enough to support the maximum load current when the
current limit is at the minimum tolerance value. The
valley of the inductor current occurs at ILOAD(MAX) minus
half the inductor ripple current (ΔL); therefore:

\[
I_{LIMIT(LOW)} = ILOAD(MAX) - \frac{\Delta L}{2}
\]

where I_{LIMIT(LOW)} equals the minimum current-limit
threshold voltage divided by the low-side MOSFETs on-
resistance (RDS(ON)).

The valley current-limit threshold is precisely 1/20 the
voltage seen at ILIM. Connect a resistive divider from
REF to ILIM to analog ground (GND) in order to set a
fixed valley current-limit threshold. The external 400mV to
2V adjustment range corresponds to a 20mV to 100mV
valley current-limit threshold. When adjusting the current-
limit threshold, use 1% tolerance resistors and a divider
current of approximately 5μA to 10μA to prevent signifi-
cant inaccuracy in the valley current-limit tolerance.

The MAX8792 uses the low-side MOSFET’s on-resis-
tance as the current-sense element (RSENSE =
RDS(ON)). Therefore, special attention must be made to
the tolerance and thermal variation of the on-resistance.
Use the worst-case maximum value for RDS(ON) from
the MOSFET data sheet, and add some margin for the
rise in RDS(ON) with temperature. A good general rule is
to allow 0.5% additional resistance for each °C of tem-
perature rise, which must be included in the design
margin unless the design includes an NTC thermistor in
the ILIM resistive voltage-divider to thermally compen-
sate the current-limit threshold.
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*Foldback Current Limit*

Including an additional resistor between ILIM and the output automatically creates a current-limit threshold that folds back as the output voltage drops (see Figure 7). The foldback current limit helps limit the inductor current under fault conditions, but must be carefully designed in order to provide reliable performance under normal conditions. The current-limit threshold must not be set too low, or the controller will not reliably power up. To ensure the controller powers up properly, the minimum current-limit threshold (when \( V_{OUT} = 0V \)) must always be greater than the maximum load during startup (which at least consists of leakage currents), plus the maximum current required to charge the output capacitors:

\[
I_{START} = C_{OUT} \times 1\text{mV/\mu s} + I_{LOAD(START)}
\]

*Output Capacitor Selection*

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements. Additionally, the ESR impacts stability requirements. Capacitors with a high ESR value (polymers/tantalums) will not need additional external compensation components.

In core and chipset converters and other applications where the output is subject to large load transients, the output capacitor’s size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

\[
(R_{ESR} + R_{PCB}) \leq \frac{V_{STEP}}{\Delta L_{LOAD(MAX)}}
\]

In low-power applications, the output capacitor’s size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor’s ESR. The maximum ESR to meet ripple requirements is:

\[
R_{ESR} \leq \left[ \frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT}) V_{OUT}} \right] V_{RIPPLE}
\]

where \( f_{SW} \) is the switching frequency.

---

**Figure 7. Standard Application with Foldback Current-Limit Protection**

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SEE TABLE 1 FOR COMPONENT SELECTION.
Single Quick-PWM Step-Down Controller with Dynamic RFIN

With most chemistries (polymer, tantalum, aluminum electrolytic), the actual capacitance value required relates to the physical size needed to achieve low ESR and the chemistry limits of the selected capacitor technology. Ceramic capacitors provide low ESR, but the capacitance and voltage rating (after derating) are determined by the capacity needed to prevent VSAG and VSOAR from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the VSAG and VSOAR equations in the Transient Response section). Thus, the output capacitor selection requires carefully balancing capacitor chemistry limitations (capacitance vs. ESR vs. voltage rating) and cost.

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the in-phase feedback ripple relative to the switching frequency, which is typically dominated by the output ESR. The boundary of instability is given by the following equation:

\[ f_{SW} \geq \frac{1}{\pi} \frac{1}{2\pi R_{EFF} C_{OUT}} \]

where \( C_{OUT} \) is the total output capacitance, \( R_{ESR} \) is the total equivalent-series resistance of the output capacitors, \( R_{PCB} \) is the parasitic board resistance between the output capacitors and feedback sense point, and \( R_{COMP} \) is the effective resistance of the DC- or AC-coupled current-sense compensation (see Figure 10).

For a standard 300kHz application, the effective zero frequency must be well below 95kHz, preferably below 50kHz. With these frequency requirements, standard tantalum and polymer capacitors already commonly used have typical ESR zero frequencies below 50kHz, allowing the stability requirements to be achieved without any additional current-sense compensation. In the standard application circuit (Figure 1), the ESR needed to support a 15mVp-p ripple is 15mV/(10A x 0.3) = 5mΩ. Two 330μF, 9mΩ polymer capacitors in parallel provide 4.5mΩ (max) ESR and 1/(2\( \pi \) x 330μF x 9mΩ) = 53kHz ESR zero frequency.

![Figure 8. Standard Application with Output Polymer or Tantalum](image)

![Figure 9. Remote-Sense Compensation for Stability and Noise Immunity](image)
Ceramic capacitors have a high ESR zero frequency, but applications with sufficient current-sense compensation may still take advantage of the small size, low ESR, and high reliability of the ceramic chemistry. Using the inductor DCR, applications using ceramic output capacitors may be compensated using either a DC compensation or AC compensation method (Figure 10).

The DC-coupling requires fewer external compensation capacitors, but this also creates an output load line that depends on the inductor’s DCR (parasitic resistance). Alternatively, the current-sense information may be AC-coupled, allowing stability to be dependent only on the inductance value and compensation components and eliminating the DC load line.

**OPTION A: DC-COUPLED CURRENT-SENSE COMPENSATION**

**DC COMPENSATION**

- Fewer compensation components
- Creates output load line
- Less output capacitance required for transient response

**OPTION B: AC-COUPLED CURRENT-SENSE COMPENSATION**

**AC COMPENSATION**

- Not dependent on actual DCR value
- No output load line

**Figure 10. Feedback Compensation for Ceramic Output Capacitors**
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When only using ceramic output capacitors, output overshoot ($V_{SOAR}$) typically determines the minimum output capacitance requirement. Their relatively low capacitance value may allow significant output overshoot when stepping from full-load to no-load conditions, unless designed with a small inductance value and high switching frequency to minimize the energy transferred from the inductor to the capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback-loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement ($I_{RMS}$) imposed by the switching currents. The $I_{RMS}$ requirements may be determined by the following equation:

$$I_{RMS} = \left( \frac{I_{LOAD}}{V_{IN}} \right) \sqrt{V_{OUT}(V_{IN} - V_{OUT})}$$

The worst-case RMS current requirement occurs when operating with $V_{IN} = 2V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than $+10^\circ C$ temperature rise at the RMS input current for optimal circuit longevity.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET ($N_{H}$) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of $N_{H}$ (reducing $R_{DS(ON)}$ but with higher $C_{GATE}$). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of $N_{H}$ (increasing $R_{DS(ON)}$ to lower $C_{GATE}$). If $V_{IN}$ does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin S0s, DPAK, or D2PAK), and is reasonably priced. Make sure that the gate driver can support sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur (see the MOSFET Gate Drivers section).

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET ($N_{H}$), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\left(\text{Resistive}\right) = \left( \frac{V_{OUT}}{V_{IN}} \right)^2 I_{LOAD}^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high-input voltages. However, the $R_{DS(ON)}$ required to stay within package-power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET ($N_{H}$) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very
rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N\textsubscript{H}:

$$PD (N\textsubscript{H} \text{ Switching}) = V_{IN(MAX)} I_{LOAD(SW)} \left( \frac{Q_{G(SW)}}{I_{GATE}} \right) + \frac{C_{OSS} V_{IN}^{2} f_{SW}}{2}$$

where $C_{OSS}$ is the N\textsubscript{H} MOSFET’s output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N\textsubscript{H} MOSFET, and $I_{GATE}$ is the peak gate-drive source/sink current (2.2A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C x V_{IN}^{2} x f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N\textsubscript{L}), the worst-case power dissipation always occurs at maximum input voltage:

$$PD (N\textsubscript{L} \text{ Resistive}) = 1 - \left( \frac{V_{OUT}}{V_{IN(MAX)}} \right) (I_{LOAD})^{2} R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can “overdesign” the circuit to tolerate:

$$I_{LOAD} = I_{VALLEY(MAX)} + \frac{\Delta I}{2} = I_{VALLEY(MAX)} + \left( \frac{I_{LOAD(MAX)} L_{IR}}{2} \right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D\textsubscript{L}) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current during the dead times. This diode is optional and can be removed if efficiency is not critical.

**Boost Capacitors**

The boost capacitors (CB\textsubscript{ST}) must be selected large enough to handle the gate charging requirements of the high-side MOSFETs. Typically, 0.1μF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side, MOSFETs require boost capacitors larger than 0.1μF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs’ gates:

$$CB_{ST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and $Q_{GATE}$ is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high-side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC ($V_{GS} = 5V$). Using the above equation, the required boost capacitance would be:

$$CB_{ST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22μF ceramic capacitor.

**Minimum Input-Voltage Requirements and Dropout Performance**

The output voltage-adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low-input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the on-times. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the VSAG equation in the Quick-PWM Design Procedure section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time ($\Delta I_{DOWN}$) as much as it ramps up during the on-time ($\Delta I_{UP}$). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As $h$ approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and VSAG greatly increases unless additional output capacitance is used.
A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between \( V_{\text{SAG}} \), output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

\[
V_{\text{IN(MIN)}} = \frac{V_{\text{FB}} (V_{\text{OUT}} - V_{\text{DROOP}} + V_{\text{CHG}})}{V_{\text{FB}} - h (V_{\text{OUT}} - V_{\text{DROOP}} + V_{\text{DIS}}) t_{\text{OFF(MIN)SW}}}
\]

where \( V_{\text{FB}} \) is the feedback voltage, \( V_{\text{CHG}} \) and \( V_{\text{DIS}} \) are the parasitic voltage drop in the charge and discharge paths, \( V_{\text{DROOP}} \) is the voltage-positioning droop, and \( t_{\text{OFF(MIN)}} \) is from the Electrical Characteristics table. The absolute minimum input voltage is calculated with \( h = 1 \). If the calculated \( V_{\text{IN(MIN)}} \) is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable \( V_{\text{SAG}} \). If operation near dropout is anticipated, calculate \( V_{\text{SAG}} \) to be sure of adequate transient response.

**Dropout Design Example:**

\[
V_{\text{FB}} = 2V \quad V_{\text{OUT}} = 3.3V \quad f_{\text{SW}} = 300kHz \quad t_{\text{OFF(MIN)}} = 350ns
\]

No droop/load line (\( V_{\text{DROOP}} = 0 \))

\( V_{\text{CHG}} \) and \( V_{\text{DIS}} = 150mV \) (10A load)

\( h = 1.5: \)

\[
V_{\text{IN(MIN)}} = \frac{2V (3.3V - 0V + 0.15V)}{2V - 1.5 \times (3.3V - 0V + 0.15V) \times 350ns \times 300kHz} = 4.74V
\]

Calculating again with \( h = 1 \) gives the absolute limit of dropout:

\[
V_{\text{IN(MIN)}} = \frac{2V (3.3V - 0V + 0.15V)}{2V - 1 \times (3.3V - 0V + 0.15V) \times 350ns \times 300kHz} = 4.21V
\]

Therefore, \( V_{\text{IN}} \) must be greater than 4.21V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 4.74V.

## Applications Information

### PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.

2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the \( V_{\text{CC}} \) bypass capacitor, REF bypass capacitors, REFIN components, and feedback compensation/dividers.

3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single m\( \Omega \) of extra trace resistance causes a measurable efficiency penalty.

4) Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.

5) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

6) Route high-speed switching nodes away from sensitive analog areas (REF, REFIN, FB, ILIM).

### Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C\( _{\text{IN}} \), C\( _{\text{OUT}} \), and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.

2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).

3) Group the gate-drive components (BST capacitors, \( V_{\text{DD}} \) bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as shown in the Standard Application Circuits. This diagram can be viewed as having three separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and \( V_{\text{DD}} \) bypass capacitor go, and the controller’s analog ground plane where sensitive analog components, the GND pin, and \( V_{\text{CC}} \) bypass capacitor go. The analog GND plane must meet the PGND plane only at a
single point directly beneath the IC. Connect to the high-power output ground using a short metal trace from PGND to the source of the low-side MOSFET. This point must also be very close to the output capacitor ground terminal.

5) Connect the output power planes (VOUT and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

**Chip Information**

PROCESS: BiCMOS

**Package Information**

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

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# Single Quick-PWM Step-Down Controller with Dynamic REFIN

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