**General Description**

The MAX77958 is a robust solution for USB Type-C CC detection and power delivery (PD) protocol implementation. It detects connected accessories or devices by using Type-C CC detection and USB PD messaging. The IC protects against overvoltage and overcurrent, and detects moisture and prevents corrosion on the USB Type-C connector. The IC also has a D+/D- USB switch and BC1.2 detection to support legacy USB standards. It contains VCONN switches for USB PD and an enable pin for an external VCONN boost or buck converter.

The IC is compliant with USB Type-C Specification Release 1.3 and PD 3.0. It can be customized easily without affecting the compliance. The IC has an I2C master that can read and write to other devices in the system so that its firmware can configure related devices without the main processor's assistance. For example, it can configure an external charger based on BC1.2 detection, CC detection, and PD communication. The IC has an interrupt output pin to report event detection and status changes. It also has an I2C interface that system can use to read/write and configure internal registers. The IC has nine configurable GPIOs that can be used for detection, as interrupts, and as the enable/disable pin for external devices, or as ADC inputs. The IC is available in a 3.10mm x 2.65mm, 0.5mm pitch, wafer-level package (WLP).

**Applications**

- Smartphones
- Tablets
- Cameras
- Game Players
- Power Banks
- Industrial Equipment PoE to USB Type-C Adapters
- Handheld Devices
- Portable Devices
- Monitors
- Healthcare and Medical Devices
- Other USB Type-C Devices

**Benefits and Features**

- Customizable Firmware
  - USB Compliant Default Embedded Firmware
  - Supports Customizable Actions on Events
  - Firmware Updates for Future Specification Revisions
- USB Type-C Support and USB-PD Support
  - USB Type-C Version 1.3 and PD3.0 Compliant
  - Mode Configuration: Sink/Source/Dual Role Port
  - Programmable Power Supply (PPS) Sink Support
  - Fast Role Swap (FRS) Initial Sink Support
  - Cable Orientation and Power Role Detection
  - Integrated VCONN Switch with OCP
  - Support Try.Snk State
  - Audio and Debug Accessory Sink/Source Mode
- Supports BC1.2 Legacy/Proprietary Charger Detection
  - Integrated D+/D- Switches
- Moisture Detection/Corrosion Prevention
- High Voltage VBUS (28V)
- Short to VBUS Protection on CC Pins (22V)
- Dead Battery Support
- Dual Supply Inputs from SYS and VBUS
- I2C Programmable Configuration
- I2C Master to Control External Charger or Direct Charge IC
- Nine Configurable GPIOs (GPIO6 for SID)
  - SuperSpeed Mux/Detection/IRQ
  - EN/DISABLE External Switches or Devices
- WLP 6x5 Bumps 0.5mm Pitch Package

**Ordering Information** appears at end of data sheet.
MAX77958
Standalone USB Type-C and USB Power Delivery Controller

Simplified Block Diagram
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Description</td>
<td>1</td>
</tr>
<tr>
<td>Applications</td>
<td>1</td>
</tr>
<tr>
<td>Benefits and Features</td>
<td>1</td>
</tr>
<tr>
<td>Simplified Block Diagram</td>
<td>2</td>
</tr>
<tr>
<td>Absolute Maximum Ratings</td>
<td>7</td>
</tr>
<tr>
<td>Package Information</td>
<td>7</td>
</tr>
<tr>
<td>WLP</td>
<td>7</td>
</tr>
<tr>
<td>Electrical Characteristics</td>
<td>9</td>
</tr>
<tr>
<td>Pin Configuration</td>
<td>25</td>
</tr>
<tr>
<td>MAX77958</td>
<td>25</td>
</tr>
<tr>
<td>Pin Description</td>
<td>25</td>
</tr>
<tr>
<td>Detailed Description</td>
<td>27</td>
</tr>
<tr>
<td>USB Type-C Interface and Control</td>
<td>27</td>
</tr>
<tr>
<td>CC/USB PD Interface</td>
<td>27</td>
</tr>
<tr>
<td>USB Type-C Definitions</td>
<td>27</td>
</tr>
<tr>
<td>DRP</td>
<td>27</td>
</tr>
<tr>
<td>Detecting Connected DFP</td>
<td>27</td>
</tr>
<tr>
<td>Detecting Connected UFP</td>
<td>28</td>
</tr>
<tr>
<td>Controls</td>
<td>28</td>
</tr>
<tr>
<td>Try.SNK Support</td>
<td>28</td>
</tr>
<tr>
<td>Audio Accessory Mode Support</td>
<td>28</td>
</tr>
<tr>
<td>DebugAccessory.SRC Support</td>
<td>28</td>
</tr>
<tr>
<td>DebugAccessory.SNK Support</td>
<td>28</td>
</tr>
<tr>
<td>USB Type-C Interface and Control</td>
<td>29</td>
</tr>
<tr>
<td>Automatic Accessory Detection</td>
<td>29</td>
</tr>
<tr>
<td>Autoconfiguration Details</td>
<td>29</td>
</tr>
<tr>
<td>USB Power Delivery</td>
<td>29</td>
</tr>
<tr>
<td>Description</td>
<td>29</td>
</tr>
<tr>
<td>IC Wakeup events</td>
<td>29</td>
</tr>
<tr>
<td>Interrupt Output (INTB)</td>
<td>30</td>
</tr>
<tr>
<td>Interconnected Block Diagram</td>
<td>30</td>
</tr>
<tr>
<td>System Faults</td>
<td>30</td>
</tr>
<tr>
<td>Undervoltage Lockout</td>
<td>30</td>
</tr>
<tr>
<td>VIO Fault</td>
<td>30</td>
</tr>
<tr>
<td>Reset Conditions</td>
<td>31</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>31</td>
</tr>
<tr>
<td>I²C Serial Interface</td>
<td>31</td>
</tr>
<tr>
<td>System Configuration</td>
<td>31</td>
</tr>
</tbody>
</table>

www.maximintegrated.com

Maxim Integrated | 3
## TABLE OF CONTENTS (CONTINUED)

- Bit Transfer ......................................................... 32
- START and STOP Conditions ................................. 32
- Acknowledge ......................................................... 33
- Slave Address ......................................................... 33
- Clock Stretching ..................................................... 33
- General Call Address ............................................. 33
- Communication Speed ............................................ 33
- Communication Protocols ........................................ 34
  - Writing to a Single Register ................................. 34
  - Writing to Sequential Registers ......................... 35
  - Reading from a Single Register ............................ 36
  - Reading from Sequential Registers ..................... 36
  - Engaging HS-Mode for Operation up to 3.4MHz .......... 37
- Register Map .......................................................... 39
- FUNC ................................................................. 39
- Register Details ..................................................... 43
- Typical Application Circuits ................................. 69
  - 2/3-Cell Configurable Charger Application ............ 69
  - 2/3-Cell Autonomous Charger Application ............. 70
  - Autonomous DC-DC Application ............................ 71
  - PD Power Adapter Application .............................. 72
- Ordering Information ............................................... 72
- Revision History ..................................................... 73
LIST OF FIGURES

Figure 1. Interconnected Block Diagram ................................................................. 30
Figure 2. Functional Logic Diagram for Communications Controller ......................... 31
Figure 3. I²C Bit Transfer .................................................................................. 32
Figure 4. I²C Start and Stop ................................................................................ 32
Figure 5. Writing to a Single Register .................................................................. 34
Figure 6. Writing to Sequential Registers ................................................................ 35
Figure 7. Reading from a Single Register ................................................................ 36
Figure 8. Reading from Sequential Registers .......................................................... 37
Figure 9. Engaging HS-Mode ............................................................................... 37
Figure 10. I²C Operating Mode State Diagram ..................................................... 38
Figure 11. Configurable Charger Application .......................................................... 69
Figure 12. Autonomous Charger Application ........................................................ 70
Figure 13. Autonomous DC-DC Application .......................................................... 71
Figure 14. Adapter Application .............................................................................. 72
LIST OF TABLES

Table 1. Rp/Rp Charging Current Values for a DTS Source .................................................. 28
Table 2. I²C Slave Address ....................................................................................................... 33
Absolute Maximum Ratings

TOP and Interface Logic
- SYS to GND: -0.3V to +22.0V
- VBUS to GND: -0.3V to +30.0V
- AVL to GND: -0.3V to +6.0V
- VDD1P8 to GND: -0.3V to +2.2V
- VIO1 to GND: -0.3V to +6.0V
- VIO2 to GND: -0.3V to +6.0V
- SCL, SDA, INTB to GND: -0.3V to VIO1 + 0.3V
- GND_A, GND_D to GND: -0.3V to +0.3V
- CC1, CC2 to GND: -0.3V to +22.0V
- VDD1P1 to GND: -0.3V to VDD1P8 + 0.3V
- SCL_M, SDA_M to GND: -0.3V to VIO2 + 0.3V
- GPIO0, GPIO1, GPIO2, GPIO3, GPIO8 to GND: -0.3V to VIO2 + 0.3V
- GPIO4, GPIO5, GPIO6, GPIO7 to GND: -0.3V to VIO1 + 0.3V

USB Type-C
- VCIN to GND: -0.3V to +6.0V
- DN, DP, DN1, DP2 to GND: -0.3V to +6.0V
- SCL_M, SDA_M to GND: -0.3V to VIO2 + 0.3V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

<table>
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<th>Package Code</th>
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<tr>
<td>Outline Number</td>
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<tr>
<td>Land Pattern Number</td>
<td>Refer to Application Note 1891</td>
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Thermal Resistance, Four-Layer Board:
- Junction to Ambient ($\theta_{JA}$): 41°C/W
- Junction to Case ($\theta_{JC}$): N/A

Continuous Power Dissipation (Multilayer Board) ($T_A = +70^\circ C$, derate 24.4mW/°C above +70°C): 21.0mW to 24.4mW

Operating Temperature Range: -40°C to +85°C

Storage Temperature Range: -65°C to +150°C
MAX77958  Standalone USB Type-C and USB Power Delivery Controller

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.
### MAX77958

**Standalone USB Type-C and USB Power Delivery Controller**

**Electrical Characteristics**

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

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<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>SYS Operating Voltage</td>
<td>$V_{SYS}$</td>
<td>$AVL_{UVL}$ OR $AVL_{UVLOR}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>AVL UVLO Rising</td>
<td>$AVL_{UVLO}$</td>
<td>AVL</td>
<td>2.6</td>
<td>2.7</td>
<td>2.8</td>
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<td>2.4</td>
<td>2.5</td>
<td>2.6</td>
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<td>AVL UVLO Hysteresis</td>
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<td>AVL Operating Voltage</td>
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<td>$AVL_{UVL}$ OR $AVL_{UVLOR}$</td>
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<td></td>
<td>V</td>
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<tr>
<td>SYS OV HR Rising</td>
<td>$SYS_{OV_HR_R}$</td>
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<td>4.87</td>
<td>5.15</td>
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<td>115</td>
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<td>mV</td>
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<td>SYS Factory Ship Supply Current</td>
<td>$I_{FSHIP}$</td>
<td>$AVL = VIO1 = VIO2 = 0V,$</td>
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<td>$CCdetEn = 0,$</td>
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<tr>
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<td>$chgDetEn = 0,$</td>
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<tr>
<td></td>
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<td>$V_{BUS} = 0V$</td>
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<td>SYS Dead Battery Supply Current</td>
<td>$I_{DEADBAT}$</td>
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<td>SYS Shutdown Supply Current</td>
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<td>SYS = $16.8V$</td>
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</tbody>
</table>

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Maxim Integrated | 9
## Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<td>SYS Standby Supply Current</td>
<td>$I_{STANDBY}$</td>
<td>Sink mode, CCdetEn = 1, chgDetEn = 1, VIO1 = VIO2 = 1.8V, $V_{BUS} = 0V$</td>
<td>SYS = 4.2V, SYS_OV_LR</td>
<td>110</td>
<td>158</td>
<td>$\mu A$</td>
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<td>SYS = 4.2V, SYS_OV_HR</td>
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<td></td>
<td>SYS = 8.4V</td>
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<td>SYS = 12.6V</td>
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<td>SYS = 16.8V</td>
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<tr>
<td>$V_{BUS}$ Operating Voltage</td>
<td>$V_{BUS}$</td>
<td></td>
<td>$V_{BDET_\text{R}}$</td>
<td>+28</td>
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<td>$V$</td>
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<td>$V_{BUS}$ Detect Rising</td>
<td>$V_{BDET_\text{R}}$</td>
<td>550mV hysteresis</td>
<td>$V_{BUS}$</td>
<td>3.6</td>
<td>3.8</td>
<td>4.0</td>
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<td>$V_{BUS}$ Detect Falling</td>
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<td>550mV hysteresis</td>
<td>$V_{BUS}$</td>
<td>2.95</td>
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<td>$V_{BUS}$ Detect Hysteresis</td>
<td>$V_{BDET_\text{H}}$</td>
<td>550mV hysteresis</td>
<td>$V_{BUS}$</td>
<td>525</td>
<td></td>
<td>$mV$</td>
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<tr>
<td>$V_{BUS}$ Supply Current</td>
<td>$I_{STANDBY}$</td>
<td>$V_{BUS} = 5V$, VIO1 = 1.8V, VIO2 = 1.8V, CCdetEn = 1, sink only, STOP mode</td>
<td>$V_{SYS} = 4.2V$</td>
<td>150</td>
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<td>$V_{SYS} = 16.8V$</td>
<td>192</td>
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<tr>
<td>$V_{BUS}$ Debounce</td>
<td>$t_{VBDeb}$</td>
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<td>9</td>
<td>10</td>
<td>11</td>
<td>$ms$</td>
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<tr>
<td>VIO_OK</td>
<td>$V_{IO_OK_LV_{-\text{R}}}$</td>
<td>VIO1, VIO2, rising</td>
<td>1.0</td>
<td>1.30</td>
<td>1.65</td>
<td>$V$</td>
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<tr>
<td></td>
<td>$V_{IO_OK_LV_{-\text{F}}}$</td>
<td>VIO1, VIO2, falling</td>
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<td>1.0</td>
<td>1.4</td>
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<td>$V_{IO_OK_LV_{-\text{H}}}$</td>
<td>VIO1, VIO2, hysteresis</td>
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<td>$mV$</td>
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<td>$V_{IO_OK_HV_{-\text{R}}}$</td>
<td>VIO1, VIO2, rising</td>
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<td>1.80</td>
<td>$V$</td>
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<td>$V_{IO_OK_HV_{-\text{F}}}$</td>
<td>VIO1, VIO2, falling</td>
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<td>1.52</td>
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<td>$V_{IO_OK_HV_{-\text{H}}}$</td>
<td>VIO1, VIO2, hysteresis</td>
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<td>$t_{VIO_OK_DEB}$</td>
<td>Debounce</td>
<td>50</td>
<td></td>
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<td>$\mu s$</td>
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<td>Output Low Voltage INTB</td>
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<td>$= 1mA$</td>
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<td></td>
<td>$V$</td>
</tr>
<tr>
<td>Output High Leakage INTB</td>
<td>$V_{\text{INTB}}$</td>
<td>$= 5.5V$, $T_A = +25^\circ C$</td>
<td>-1000</td>
<td>0</td>
<td>+1000</td>
<td>$nA$</td>
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<tr>
<td></td>
<td>$V_{\text{INTB}}$</td>
<td>$= 5.5V$, $T_A = +85^\circ C$</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD_OK</td>
<td>$V_{DD_OK_R}$</td>
<td>VDD1P8, rising</td>
<td>1.30</td>
<td>1.65</td>
<td>1.70</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td>$V_{DD_OK_F}$</td>
<td>VDD1P8, falling</td>
<td>1.15</td>
<td>1.55</td>
<td>1.65</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{DD_OK_H}$</td>
<td>VDD1P8, hysteresis</td>
<td>100</td>
<td></td>
<td></td>
<td>$mV$</td>
</tr>
</tbody>
</table>

### INTERFACE / I^2C INTERFACE AND INTERRUPT

<table>
<thead>
<tr>
<th>SCL, SDA Input Low Level</th>
<th>$T_A = +25^\circ C$</th>
<th>0.3 x $V_{IO1}$</th>
<th>$V$</th>
</tr>
</thead>
</table>
### Electrical Characteristics (continued)

(Limits are 100% tested at \( T_A = +25^\circ C \). Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL, SDA Input High Level</td>
<td>V</td>
<td>( T_A = +25^\circ C )</td>
<td>0.7 x</td>
<td>VIO1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SCL, SDA Input Hysteresis</td>
<td>V</td>
<td>( T_A = +25^\circ C )</td>
<td>0.05 x</td>
<td>VIO1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SCL, SDA Logic Input Current</td>
<td>V</td>
<td>SDA = SCL = 5.5V</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SDA Output Low Voltage</td>
<td>V</td>
<td>Sinking 20mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage INTB</td>
<td>I_{SINK}</td>
<td>1mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output High Leakage INTB</td>
<td>V_{INTB}</td>
<td>5.5V, ( T_A = +25^\circ C )</td>
<td>-1000</td>
<td></td>
<td>+1000</td>
<td>nA</td>
</tr>
</tbody>
</table>

#### INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS

<table>
<thead>
<tr>
<th>Clock Frequency ( f_{SCL} )</th>
<th>( f_{SCL} )</th>
<th>( T_A = +25^\circ C )</th>
<th>1000</th>
<th>kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold Time (Repeated) START</td>
<td>t_{HD;STA}</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK Low Period</td>
<td>t_{LOW}</td>
<td>500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK High Period</td>
<td>t_{HIGH}</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time Repeated START</td>
<td>t_{SU;STA}</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Hold Time</td>
<td>t_{HD;DAT}</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Valid Time</td>
<td>t_{VD;DAT}</td>
<td>450</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Valid Acknowledge Time</td>
<td>t_{VD;ACK}</td>
<td>450</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall Time of SCL</td>
<td>t_{SCL}</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall Time of SDA</td>
<td>t_{SCL}</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Setup time</td>
<td>t_{SU;DAT}</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time for STOP Condition</td>
<td>t_{SU;STO}</td>
<td>260</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Bus-Free Time Between STOP and START</td>
<td>t_{BUF}</td>
<td>500</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse Width of Spikes that Must be Suppressed by the Input Filter</td>
<td></td>
<td></td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

#### INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF)

<table>
<thead>
<tr>
<th>Clock Frequency ( f_{SCL} )</th>
<th>( f_{SCL} )</th>
<th>( T_A = +25^\circ C )</th>
<th>3.4</th>
<th>MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Setup Time Repeated START</td>
<td>t_{SU;STA}</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time (Repeated) START</td>
<td>t_{HD;STA}</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK Low Period</td>
<td>t_{LOW}</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK High Period</td>
<td>$t_{\text{HIGH}}$</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Set-Up time</td>
<td>$t_{\text{SU;DAT}}$</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Hold Time</td>
<td>$t_{\text{HD;DAT}}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall time of SCL</td>
<td>$t_{\text{SCL}}$</td>
<td></td>
<td>10</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall time of SDA</td>
<td>$t_{\text{SDA}}$</td>
<td></td>
<td>10</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Set-Up Time for STOP Condition</td>
<td>$t_{\text{SU;STO}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse Width of Spikes that Must be Suppressed</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

INTERFACE / I\textsuperscript{2}C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Frequency</td>
<td>$f_{\text{SCL}}$</td>
<td></td>
<td>1.7</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Setup Time Repeated START Condition</td>
<td>$t_{\text{SU;STA}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold Time (Repeated) START Condition</td>
<td>$t_{\text{HD;STA}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK Low Period</td>
<td>$t_{\text{LOW}}$</td>
<td></td>
<td>320</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLK High Period</td>
<td>$t_{\text{HIGH}}$</td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Set-Up time</td>
<td>$t_{\text{SU;DAT}}$</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>DATA Hold Time</td>
<td>$t_{\text{HD;DAT}}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall Time of SCL</td>
<td>$t_{\text{SCL}}$</td>
<td></td>
<td>20</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise/Fall Time of SDA</td>
<td>$t_{\text{SDA}}$</td>
<td></td>
<td>10</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time for STOP Condition</td>
<td>$t_{\text{SU;STO}}$</td>
<td></td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse Width of Spikes that Must be Suppressed</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

USB TYPE-C / CHARGER DETECTION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC1.2 State Timeout</td>
<td>$t_{\text{TMO}}$</td>
<td></td>
<td>180</td>
<td>200</td>
<td>220</td>
<td>ms</td>
</tr>
<tr>
<td>Data Contact Detect Timeout</td>
<td>$t_{\text{DCD,mo}}$</td>
<td>DCDCpl = 0b1 (default), DCDCpl = 0b0</td>
<td>700</td>
<td>800</td>
<td>900</td>
<td>ms</td>
</tr>
<tr>
<td>Primary to Secondary Timer</td>
<td>$t_{\text{PDSDWait}}$</td>
<td></td>
<td>27</td>
<td>35</td>
<td>39</td>
<td>ms</td>
</tr>
<tr>
<td>Charger Detection Debounce</td>
<td>$t_{\text{CDDeb}}$</td>
<td></td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>ms</td>
</tr>
<tr>
<td>$I_{\text{WEAK}}$ Current</td>
<td>$I_{\text{WEAK}}$</td>
<td>accurate over 0V to 2.5V</td>
<td>10</td>
<td>100</td>
<td>500</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{\text{DM,DWN}}$ Resistor</td>
<td>$R_{\text{DM,DWN}}$</td>
<td></td>
<td>14.25</td>
<td>20</td>
<td>24.8</td>
<td>kΩ</td>
</tr>
<tr>
<td>$I_{\text{DP, SRC}}$ Current</td>
<td>$I_{\text{DP, SRC}}$</td>
<td>accurate over 0V to 2.5V</td>
<td>-13</td>
<td>-10</td>
<td>-7</td>
<td>μA</td>
</tr>
</tbody>
</table>
## Electrical Characteristics (continued)

(Limits are 100% tested at T<sub>A</sub> = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>CONDITIONS</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DM_SINK Current</td>
<td>IDM_SINK/I&lt;sub&gt;DAT&lt;/sub&gt;_SINK</td>
<td>Accurate over 0.15V to 3.6V</td>
<td>50</td>
<td>80</td>
<td>110</td>
<td>μA</td>
</tr>
<tr>
<td>V&lt;sub&gt;LGC&lt;/sub&gt; Threshold</td>
<td>V&lt;sub&gt;LGC&lt;/sub&gt;</td>
<td></td>
<td>1.62</td>
<td>1.7</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;LGC&lt;/sub&gt; Hysteresis</td>
<td>V&lt;sub&gt;LGC_H&lt;/sub&gt;</td>
<td></td>
<td>0.015</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DAT_REF&lt;/sub&gt; Threshold</td>
<td>V&lt;sub&gt;DAT_REF&lt;/sub&gt;</td>
<td></td>
<td>0.25</td>
<td>0.32</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;DAT_REF&lt;/sub&gt; Hysteresis</td>
<td>V&lt;sub&gt;DAT_REF_H&lt;/sub&gt;</td>
<td></td>
<td>0.015</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>OVX Comparator Falling Threshold</td>
<td>VOVX&lt;sub&gt;THF&lt;/sub&gt;</td>
<td>Falling DP/DN threshold with respect to AVL</td>
<td>-40</td>
<td>+80</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>OVX Comparator Rising Threshold</td>
<td>VOVX&lt;sub&gt;THR&lt;/sub&gt;</td>
<td>Rising DP/DN threshold with respect to AVL</td>
<td>0</td>
<td>150</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>DP/DN Overvoltage Debounce</td>
<td>tOVX Deb</td>
<td></td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>μs</td>
</tr>
<tr>
<td>DN/DP Load Resistor</td>
<td>R&lt;sub&gt;USB&lt;/sub&gt;</td>
<td>Load resistor on DP/DN</td>
<td>3</td>
<td>6.1</td>
<td>12</td>
<td>MΩ</td>
</tr>
<tr>
<td>V&lt;sub&gt;D33&lt;/sub&gt; Voltage</td>
<td>V&lt;sub&gt;D33&lt;/sub&gt;/DM&lt;sub&gt;_3p3VSRC&lt;/sub&gt;/VSRC33</td>
<td>Tested at zero load and at 200μA load</td>
<td>2.6</td>
<td>3.0</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>VSRC33ILIM Current Limit</td>
<td>I&lt;sub&gt;LIMVSRC33&lt;/sub&gt;</td>
<td>Force 1.6V on DP/DN, measure current</td>
<td>1.5</td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>VDN_SRC Voltage</td>
<td>V&lt;sub&gt;DNlington&lt;/sub&gt;/VSRC&lt;sub&gt;C06&lt;/sub&gt;</td>
<td>Accurate over I&lt;sub&gt;LOAD&lt;/sub&gt; = 0 to 200μA</td>
<td>0.5</td>
<td>0.6</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>VDP_SRC Voltage</td>
<td>V&lt;sub&gt;DPlington&lt;/sub&gt;/VSRC&lt;sub&gt;C06&lt;/sub&gt;</td>
<td>Accurate over I&lt;sub&gt;LOAD&lt;/sub&gt; = 0 to 200μA</td>
<td>0.5</td>
<td>0.6</td>
<td>0.7</td>
<td>V</td>
</tr>
</tbody>
</table>

### USB Type-C / CC DETECTION

| PARAMETER                          | SYMBOL                | CONDITIONS                  | MIN  | TYP  | MAX  | UNITS |
| CC Pin Voltage, in DFP 1.5A Mode    | V<sub>CC_PIN</sub>   | Measured at CC pins with 126kΩ load, IDFP1.5_CC enable and V<sub>AVL</sub> ≥ 2.6V | 1.85 |      |      | V     |
| CC Pin Voltage, in DFP 3.0A Mode    | V<sub>CC_PIN</sub>   | Measured at CC pins with 126kΩ load, IDFP3.0_CC enable and AVL ≥ 3.65V | 3.1  |      |      | V     |
| CC Pin Clamp Voltage                | V<sub>CC CIAMP</sub> | 60μA ≤ I<sub>CC</sub> ≤ 600μA | 0.88 | 1.1  | 1.32 | V     |
| CC UFP Pulldown Resistance          | R<sub>PD_UFP</sub>  | -10% to 5.1 +10%            |      |      |      | kΩ    |
| CC DFP Low-Power Mode               | V<sub>DFPLP_CC</sub>| AVL ≥ 2.6V, ID<sub>DFPULP_CC</sub> current source enabled, 1.1V | 1.2  |      |      | V     |
| CC DFP Ultra-Low-Power Current Source | ID<sub>DFPULP_CC</sub> | Measured at CC = 0.5V | -10% | 1    | +10% | μA    |
| | | Measured at CC = 1.0V, T<sub>A</sub> = +25°C | -10% | 1    | +10% | μA    |
| | | Measured at CC = 1.0V | -12% | 1    | +12% |       |
| CC DFP 0.5A Current Source          | ID<sub>DFP0.5_CC</sub>| -20% to 80 +20%            |      |      |      | μA    |
| CC DFP 1.5A Current Source          | ID<sub>DFP1.5_CC</sub>| -8% to 180 +8%             |      |      |      | μA    |
| CC DFP 3A Current Source            | ID<sub>DFP3A_CC</sub>| -8% to 330 +8%             |      |      |      | μA    |
| CC RA RD Threshold                  | VR<sub>AR</sub> RD0.5 |                             | 0.15 | 0.2  | 0.25 | V     |
Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC UFP 0.5A RD Threshold</td>
<td>$V_{UFP_RD0.5}$</td>
<td></td>
<td>0.61</td>
<td>0.66</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>CC UFP 0.5A RD Hysteresis</td>
<td>$V_{UFP_RD0.5_H}$</td>
<td></td>
<td></td>
<td>0.015</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CC UFP 1.5A RD Threshold</td>
<td>$V_{UFP_RD1.5}$</td>
<td></td>
<td>1.16</td>
<td>1.23</td>
<td>1.31</td>
<td>V</td>
</tr>
<tr>
<td>CC UFP 1.5A RD Hysteresis</td>
<td>$V_{UFP_RD1.5_H}$</td>
<td></td>
<td></td>
<td>0.015</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CC DFP V_OPEN Detect Threshold</td>
<td>$V_{DFP_VOPEN}$</td>
<td></td>
<td>1.5</td>
<td>1.575</td>
<td>1.65</td>
<td>V</td>
</tr>
<tr>
<td>CC DFP V_OPEN Hysteresis</td>
<td>$V_{DFP_VOPEN_H}$</td>
<td></td>
<td></td>
<td>0.030</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CC DFP V_OPEN 3.0A Detect Threshold</td>
<td>$V_{DFP_VOPEN3A}$</td>
<td>$V_{AVL} \geq 3.5V$</td>
<td>2.45</td>
<td>2.6</td>
<td>2.75</td>
<td>V</td>
</tr>
<tr>
<td>CC DFP V_OPEN 3.0A Detect Hysteresis</td>
<td>$V_{DFP_VOPEN3A_H}$</td>
<td>$V_{AVL} \geq 3.5V$</td>
<td></td>
<td>0.030</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{BUS}$ Discharge Value Threshold</td>
<td>$V_{SAFE0V}$</td>
<td>Falling voltage level where a connected UFP finds the $V_{BUS}$ removed</td>
<td>0.6</td>
<td>0.67</td>
<td>0.75</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BUS}$ Discharge Value Hysteresis</td>
<td>$V_{SAFE0V_h}$</td>
<td>Rising hysteresis</td>
<td></td>
<td>40</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>CC Pin Power-Up Time</td>
<td>$t_{ClampSwap}$</td>
<td>Max time allowed from removal of voltage clamp until a 5.1k$\Omega$ resistor attached</td>
<td></td>
<td></td>
<td></td>
<td>15 ms</td>
</tr>
<tr>
<td>CC Detection Debounce</td>
<td>$t_{CCDeb}$</td>
<td></td>
<td>100</td>
<td>119</td>
<td>200</td>
<td>ms</td>
</tr>
<tr>
<td>Type-C Debounce</td>
<td>$t_{PDDeb}$</td>
<td></td>
<td>10</td>
<td>15</td>
<td>20</td>
<td>ms</td>
</tr>
<tr>
<td>Type-C Quick Debounce</td>
<td>$t_{QDeb}$</td>
<td></td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
<td>ms</td>
</tr>
<tr>
<td>VSAFE0V Debounce</td>
<td>$t_{VSAFE0VDeb}$</td>
<td></td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>ms</td>
</tr>
<tr>
<td>Type-C Error Recovery Delay</td>
<td>$t_{ErrorRecovery}$</td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Type-C DRP Toggle Time</td>
<td>$t_{DRP}$</td>
<td></td>
<td>50</td>
<td>75</td>
<td>100</td>
<td>ms</td>
</tr>
<tr>
<td>DFP Duty Cycle at DRP</td>
<td></td>
<td>Programmable from 35% to 50% in 5% step, $CCDRPPhase = 0b00$</td>
<td>35</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Type-C DRP Try</td>
<td>$t_{DRPtry}$</td>
<td></td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>ms</td>
</tr>
<tr>
<td>DRP Transition Time</td>
<td>$t_{DRPTrans}$</td>
<td>Time for a role swap from DFP to UFP or the reverse is completed</td>
<td>1</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$V_{CONN}$ Enable Time</td>
<td>$t_{VCONN}$</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$V_{CONN}$ Disable Time</td>
<td>$t_{VCONNOFF}$</td>
<td>Time from UFP detached or as directed by $I^2C$ command until $V_{CONN}$ is removed</td>
<td>35</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>CC Pin Current Change Time</td>
<td>$I_{SINKADJ}$</td>
<td>Time from CC pin changes state in UFP mode until current drawn from DFP reaches a new value</td>
<td>60</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$V_{BUS}$ On Time</td>
<td>$t_{VBUSON}$</td>
<td>Time from UFP is attached until $V_{BUS}$ ON</td>
<td></td>
<td>275</td>
<td></td>
<td>ms</td>
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</tbody>
</table>
**Electrical Characteristics (continued)**

(Limits are 100% tested at $T_A = +25^\circ{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

<table>
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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>$V_{BUS}$ Off Time</td>
<td>$t_{VBUSOFF}$</td>
<td>Time from UFP is detached until $V_{BUS}$ reaches $V_{SAFE0V}$</td>
<td>650</td>
<td>ms</td>
<td></td>
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<tr>
<td>$V_{BUS}$ Input Self-Discharge Resistance</td>
<td>$R_{VBUS_SD_US}$</td>
<td></td>
<td>10</td>
<td>kΩ</td>
<td></td>
<td></td>
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<tr>
<td>CC1/2 Water Comp Threshold</td>
<td>$V_{CC_Comp}$</td>
<td>1.0V Comp</td>
<td>-8%</td>
<td>1.00</td>
<td>+8%</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.8V Comp</td>
<td>-8%</td>
<td>0.8</td>
<td>+8%</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.6V Comp</td>
<td>-8%</td>
<td>0.6</td>
<td>+8%</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.4V Comp</td>
<td>-8%</td>
<td>0.4</td>
<td>+8%</td>
<td>V</td>
</tr>
<tr>
<td>CC1/2 Water Comp Hysteresis</td>
<td>$V_{CC_Comp_H}$</td>
<td></td>
<td>0.015</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CC_OVP Threshold</td>
<td>$CC_OVP$</td>
<td>Rising</td>
<td>5.375</td>
<td>5.735</td>
<td>6.325</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling</td>
<td>5.175</td>
<td>5.670</td>
<td>6.275</td>
<td>V</td>
</tr>
<tr>
<td>CC_OVP Hysteresis</td>
<td>$CC_OVP_H$</td>
<td></td>
<td>85</td>
<td>mV</td>
<td></td>
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</tr>
</tbody>
</table>

**USB TYPE-C / $V_{CONN}$ Switch**

| $V_{CIN\_PRES}$ | $V_{CIN\_PRES\_R}$ | Rising | 0.75 | 1.38 | 2.45 | V |
| | $V_{CIN\_PRES\_F}$ | Falling | 0.45 | 0.75 | 1.75 | V |
| | $V_{CIN\_PRES\_H}$ | Hysteresis | 600 | mV |
| | $t_{VIN\_PRES\_DEB}$ | Debounce | 50 | μs |
| $V_{CIN\_OK}$ | $CC\_V_{CIN\_OK\_R}$ | Rising | 2.40 | 2.75 | 3.00 | V |
| | $CC\_V_{CIN\_OK\_F}$ | Falling | 2.35 | 2.72 | 3.00 | V |
| | $CC\_V_{CIN\_OK\_H}$ | Hysteresis | 30 | mV |
| | $t_{V_{CIN\_OK\_DEB}}$ | Debounce | 50 | μs |
| $V_{CONN}$ Source Requirements | | | 3.0 | 5.5 | V |
| $V_{CONN}$ SW Ron | $R_{VCONN\_SW}$ | $V_{CIN} = 5.0V$, $ICC = 0.5A$ | 500 | 900 | mΩ |
| OCP Accuracy | | $V_{CIN} = 5.0V$, $T_A = +25^\circ{C}$ | -40 | -20 | % |
| OCP_ShortCircuit Protection | $I_{SCP}$ | | 700 | mA |
| OCP Programmable Step | $I_{STEP}$ | Programmable range is 200mA to 500mA | 100 | mA |
| OCP Interrupt Debounce Time T1 | $t_{Deb1}$ | From detecting OCP to generating INT | 2 | ms |
| Wait Time Before Turn Off T2 | $t_{Deb2}$ | From generating INT to turning OFF $V_{CONN}$ switch | 12 | ms |
**Electrical Characteristics (continued)**

(Limits are 100% tested at \( T_A = +25^\circ C \). Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

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</tr>
</thead>
<tbody>
<tr>
<td>Startup Time At 90%</td>
<td></td>
<td>Time from ( V_{\text{CONN}} ) switch enable to CC settled at 90% of final value with ( V_{\text{CIN}} = 3.0V )</td>
<td>0.05</td>
<td>0.2</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Turn Off Time At 10%</td>
<td></td>
<td>Time from ( V_{\text{CONN}} ) switch disable to CC settled at 10% of final value with ( V_{\text{CIN}} = 3.0V )</td>
<td>0.05</td>
<td>0.06</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>VCIN Leakage Current</td>
<td></td>
<td>VCIN detection disabled, ( V_{\text{CIN}} = 4.4V )</td>
<td>-2000</td>
<td></td>
<td>+2000</td>
<td>nA</td>
</tr>
</tbody>
</table>

**USB TYPE-C / PD Controller**

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Time Until BMC Bus Drive End</td>
<td>( t_{\text{EndDriveBMC}} )</td>
<td>Time to cease driving the line after the end of the last bit of the frame, Min value is limited by ( t_{\text{HoldLowBMC}} )</td>
<td>23</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Transmit Hold Time</td>
<td>( t_{\text{HoldLowBMC}} )</td>
<td>Time to cease driving the line after the final high-to-low transition</td>
<td>1</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>BMC TX Rise Time</td>
<td>( t_{\text{Rise}} )</td>
<td>10% to 90% with no load on CC wires</td>
<td>300</td>
<td>410</td>
<td>540</td>
<td>ns</td>
</tr>
<tr>
<td>BMC TX Fall Time</td>
<td>( t_{\text{Fall}} )</td>
<td>90% to 10% with no load on CC wires</td>
<td>300</td>
<td>410</td>
<td>540</td>
<td>ns</td>
</tr>
<tr>
<td>BMC TX Swing</td>
<td>( V_{\text{SWING}} )</td>
<td>Applies to no load and with max load defined by cable/receiver model for both Sink and Source</td>
<td>1.05</td>
<td>1.125</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>BMC Driver Output Impedance</td>
<td>( z_{\text{Driver}} )</td>
<td>Source output impedance at the Nyquist frequency of [USB 2.0] low speed (750kHz)</td>
<td>42</td>
<td>75</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>BMC Receiver Noise Filter</td>
<td>( t_{\text{RXFilter}} )</td>
<td>Time constant of noise filter in RX path</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Time To Detect Non-Idle Bus</td>
<td>( t_{\text{TransitionWind ow}} )</td>
<td></td>
<td>12</td>
<td>20</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Receiver Detect Rising Threshold in SRC Mode</td>
<td></td>
<td></td>
<td>0.63</td>
<td>0.66</td>
<td>0.68</td>
<td>V</td>
</tr>
<tr>
<td>Receiver Detect Falling Threshold in SRC Mode</td>
<td></td>
<td></td>
<td>0.56</td>
<td>0.58</td>
<td>0.61</td>
<td>V</td>
</tr>
<tr>
<td>Receiver Detect Rising Threshold SNK Mode</td>
<td></td>
<td></td>
<td>0.51</td>
<td>0.54</td>
<td>0.56</td>
<td>V</td>
</tr>
<tr>
<td>Receiver Detect Falling Threshold in SNK Mode</td>
<td></td>
<td></td>
<td>0.44</td>
<td>0.46</td>
<td>0.49</td>
<td>V</td>
</tr>
<tr>
<td>Hysteresis of BMC RX</td>
<td>( RX_{\text{Hys}} )</td>
<td></td>
<td></td>
<td>60</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

**USB TYPE-C / \( V_{\text{BUS}} \) ADC**

| \( V_{\text{BUS}} \) ADC Threshold 1 | \( \text{THV}_{\text{BUS}} \_01 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00000 \) | 3.0 | 3.5 | 4.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 2 | \( \text{THV}_{\text{BUS}} \_02 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00001 \) | 4.0 | 4.5 | 5.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 3 | \( \text{THV}_{\text{BUS}} \_03 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00010 \) | 5.0 | 5.5 | 6.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 4 | \( \text{THV}_{\text{BUS}} \_04 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00011 \) | 6.0 | 6.5 | 7.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 5 | \( \text{THV}_{\text{BUS}} \_05 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00100 \) | 7.0 | 7.5 | 8.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 6 | \( \text{THV}_{\text{BUS}} \_06 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00101 \) | 8.0 | 8.5 | 9.0 | V |
| \( V_{\text{BUS}} \) ADC Threshold 7 | \( \text{THV}_{\text{BUS}} \_07 \) | \( \text{ADCIN\_SEL} = 0 \) | \( \text{VBADC} = 0b00110 \) | 9.0 | 9.5 | 10.0 | V |
Electrical Characteristics (continued)

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

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<thead>
<tr>
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<tbody>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 8</td>
<td>TH$V_{\text{BUS}}$_08</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}00111$</td>
<td>10.0</td>
<td>10.5</td>
<td>11.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 9</td>
<td>TH$V_{\text{BUS}}$_09</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10000$</td>
<td>11.0</td>
<td>11.5</td>
<td>12.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 10</td>
<td>TH$V_{\text{BUS}}$_10</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10001$</td>
<td>12.0</td>
<td>12.5</td>
<td>13.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 11</td>
<td>TH$V_{\text{BUS}}$_11</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01010$</td>
<td>13.0</td>
<td>13.5</td>
<td>14.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 12</td>
<td>TH$V_{\text{BUS}}$_12</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01011$</td>
<td>14.0</td>
<td>14.5</td>
<td>15.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 13</td>
<td>TH$V_{\text{BUS}}$_13</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01100$</td>
<td>15.0</td>
<td>15.5</td>
<td>16.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 14</td>
<td>TH$V_{\text{BUS}}$_14</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01101$</td>
<td>16.0</td>
<td>16.5</td>
<td>17.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 15</td>
<td>TH$V_{\text{BUS}}$_15</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01110$</td>
<td>17.0</td>
<td>17.5</td>
<td>18.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 16</td>
<td>TH$V_{\text{BUS}}$_16</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}01111$</td>
<td>18.0</td>
<td>18.5</td>
<td>19.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 17</td>
<td>TH$V_{\text{BUS}}$_17</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10000$</td>
<td>19.0</td>
<td>19.5</td>
<td>20.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 18</td>
<td>TH$V_{\text{BUS}}$_18</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10001$</td>
<td>20.0</td>
<td>20.5</td>
<td>21.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 19</td>
<td>TH$V_{\text{BUS}}$_19</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10010$</td>
<td>21.0</td>
<td>21.5</td>
<td>22.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 20</td>
<td>TH$V_{\text{BUS}}$_20</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10011$</td>
<td>22.0</td>
<td>22.5</td>
<td>23.0</td>
<td>V</td>
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<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 21</td>
<td>TH$V_{\text{BUS}}$_21</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10100$</td>
<td>23.0</td>
<td>23.5</td>
<td>24.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 22</td>
<td>TH$V_{\text{BUS}}$_22</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10101$</td>
<td>24.0</td>
<td>24.5</td>
<td>25.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 23</td>
<td>TH$V_{\text{BUS}}$_23</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10110$</td>
<td>25.0</td>
<td>25.5</td>
<td>26.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 24</td>
<td>TH$V_{\text{BUS}}$_24</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}10111$</td>
<td>26.0</td>
<td>26.5</td>
<td>27.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Threshold 25</td>
<td>TH$V_{\text{BUS}}$_25</td>
<td>$\text{ADCIN_SEL} = 0$ $\text{VBADC} = 0\text{b}11000$</td>
<td>27.0</td>
<td>27.5</td>
<td>28.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{BUS}}$ ADC Hysteresis</td>
<td>$HV_{\text{BUS}}$</td>
<td>$\text{ADCIN_SEL} = 0$</td>
<td>150</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

**USB TYPE-C / ADC ADC**

<table>
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<tr>
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<tr>
<td>GPIO ADC Threshold 1</td>
<td>THGPIO_01</td>
<td>$\text{ADCIN_SEL} = 1$ $\text{VBADC} = 0\text{b}00000$</td>
<td>0.6</td>
<td>0.7</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>GPIO ADC Threshold 2</td>
<td>THGPIO_02</td>
<td>$\text{ADCIN_SEL} = 1$ $\text{VBADC} = 0\text{b}00001$</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>GPIO ADC Threshold 3</td>
<td>THGPIO_03</td>
<td>$\text{ADCIN_SEL} = 1$ $\text{VBADC} = 0\text{b}00010$</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>GPIO ADC Threshold 4</td>
<td>THGPIO_04</td>
<td>$\text{ADCIN_SEL} = 1$ $\text{VBADC} = 0\text{b}00011$</td>
<td>1.2</td>
<td>1.3</td>
<td>1.4</td>
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## Electrical Characteristics (continued)

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Electrical Characteristics (continued)

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<td>THCC_13, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b01100</td>
<td>0.945</td>
<td>0.980</td>
<td>1.008</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 14</td>
<td>THCC_14, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b01101</td>
<td>1.008</td>
<td>1.045</td>
<td>1.071</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 15</td>
<td>THCC_15, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b01110</td>
<td>1.071</td>
<td>1.104</td>
<td>1.134</td>
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<tr>
<td>CC ADC Threshold 16</td>
<td>THCC_16, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b01111</td>
<td>1.134</td>
<td>1.166</td>
<td>1.197</td>
<td>V</td>
</tr>
<tr>
<td>CC ADC Threshold 17</td>
<td>THCC_17, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b10000</td>
<td>1.197</td>
<td>1.227</td>
<td>1.260</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 18</td>
<td>THCC_18, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b10001</td>
<td>1.260</td>
<td>1.293</td>
<td>1.323</td>
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<tr>
<td>CC ADC Threshold 19</td>
<td>THCC_19, ADCIN_SEL = 001 or 011</td>
<td>VBADC = 0b10010</td>
<td>1.323</td>
<td>1.357</td>
<td>1.386</td>
<td>V</td>
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**Electrical Characteristics (continued)**

(Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

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<tr>
<td>CC ADC Threshold 20</td>
<td>THCC_20</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b10010</td>
<td>1.386</td>
<td>1.421</td>
<td>1.449</td>
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<td>CC ADC Threshold 21</td>
<td>THCC_21</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b10100</td>
<td>1.449</td>
<td>1.484</td>
<td>1.512</td>
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<tr>
<td>CC ADC Threshold 22</td>
<td>THCC_22</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b10101</td>
<td>1.512</td>
<td>1.545</td>
<td>1.575</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 23</td>
<td>THCC_23</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b10110</td>
<td>1.575</td>
<td>1.612</td>
<td>1.638</td>
<td>V</td>
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<td>CC ADC Threshold 24</td>
<td>THCC_24</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b10111</td>
<td>1.638</td>
<td>1.671</td>
<td>1.701</td>
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<td>CC ADC Threshold 25</td>
<td>THCC_25</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b11000</td>
<td>1.701</td>
<td>1.731</td>
<td>1.764</td>
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<td>CC ADC Hysteresis</td>
<td>HCC</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>15</td>
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**USB TYPE-C / CC ADC RANGE 3**

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<tr>
<td>CC ADC Threshold 1</td>
<td>THCC_01</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00000</td>
<td>0.150</td>
<td>0.175</td>
<td>0.200</td>
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<td>CC ADC Threshold 2</td>
<td>THCC_02</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00001</td>
<td>0.200</td>
<td>0.225</td>
<td>0.250</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 3</td>
<td>THCC_03</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00010</td>
<td>0.250</td>
<td>0.275</td>
<td>0.300</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 4</td>
<td>THCC_04</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00011</td>
<td>0.300</td>
<td>0.325</td>
<td>0.350</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 5</td>
<td>THCC_05</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00100</td>
<td>0.350</td>
<td>0.375</td>
<td>0.400</td>
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<td>CC ADC Threshold 6</td>
<td>THCC_06</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00101</td>
<td>0.400</td>
<td>0.425</td>
<td>0.450</td>
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<td>CC ADC Threshold 7</td>
<td>THCC_07</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00110</td>
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<td>0.475</td>
<td>0.500</td>
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<tr>
<td>CC ADC Threshold 8</td>
<td>THCC_08</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b00111</td>
<td>0.500</td>
<td>0.525</td>
<td>0.550</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 9</td>
<td>THCC_09</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01000</td>
<td>0.550</td>
<td>0.575</td>
<td>0.600</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 10</td>
<td>THCC_10</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01001</td>
<td>0.600</td>
<td>0.625</td>
<td>0.650</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 11</td>
<td>THCC_11</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01010</td>
<td>0.650</td>
<td>0.675</td>
<td>0.700</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 12</td>
<td>THCC_12</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01011</td>
<td>0.700</td>
<td>0.725</td>
<td>0.750</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 13</td>
<td>THCC_13</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01100</td>
<td>0.750</td>
<td>0.775</td>
<td>0.800</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 14</td>
<td>THCC_14</td>
<td>ADCIN_SEL = 001 or 011 VBADC = 0b01101</td>
<td>0.800</td>
<td>0.825</td>
<td>0.850</td>
<td>V</td>
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</table>
### Electrical Characteristics (continued)

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<tbody>
<tr>
<td>CC ADC Threshold 15</td>
<td>THCC_15</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>0.850</td>
<td>0.875</td>
<td>0.900</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 16</td>
<td>THCC_16</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>0.900</td>
<td>0.925</td>
<td>0.950</td>
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<tr>
<td>CC ADC Threshold 17</td>
<td>THCC_17</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>0.950</td>
<td>0.975</td>
<td>1.000</td>
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<tr>
<td>CC ADC Threshold 18</td>
<td>THCC_18</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.000</td>
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<td>1.050</td>
<td>V</td>
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<td>CC ADC Threshold 19</td>
<td>THCC_19</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.050</td>
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<td>1.100</td>
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<td>CC ADC Threshold 20</td>
<td>THCC_20</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.100</td>
<td>1.125</td>
<td>1.150</td>
<td>V</td>
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<tr>
<td>CC ADC Threshold 21</td>
<td>THCC_21</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.150</td>
<td>1.175</td>
<td>1.200</td>
<td>V</td>
</tr>
<tr>
<td>CC ADC Threshold 22</td>
<td>THCC_22</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.200</td>
<td>1.225</td>
<td>1.250</td>
<td>V</td>
</tr>
<tr>
<td>CC ADC Threshold 23</td>
<td>THCC_23</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.250</td>
<td>1.275</td>
<td>1.300</td>
<td>V</td>
</tr>
<tr>
<td>CC ADC Threshold 24</td>
<td>THCC_24</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.300</td>
<td>1.325</td>
<td>1.350</td>
<td>V</td>
</tr>
<tr>
<td>CC ADC Threshold 25</td>
<td>THCC_25</td>
<td>ADCIN_SEL = 001 or 011</td>
<td>1.350</td>
<td>1.375</td>
<td>1.400</td>
<td>V</td>
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<tr>
<td>CC ADC Hysteresis</td>
<td>HCC</td>
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<td>7</td>
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<td>mV</td>
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**USB TYPE-C / USB ANALOG SWITCH (DN1/DP2)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Analog Signal Range</td>
<td>$V_{DN1}$, $V_{DP2}$</td>
<td>$V_{AVL}$</td>
<td>0</td>
<td></td>
<td>$V_{AVL}$</td>
<td>V</td>
</tr>
<tr>
<td>On-Resistance</td>
<td>$R_{ONUSB}$</td>
<td>$AVL = 3.0V$, $I_{DN}/I_{DP} = 10mA$, $V_{DN}/V_{DP} = 0V$ to $3.0V$</td>
<td>3</td>
<td>6</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Off-Leakage Current</td>
<td>$I_{LUSBOFF}$</td>
<td>$AVL = 4.2V$; Switch opened; $V_{DN1}$ or $V_{DP2} = 0.3V$, $2.5V$, $V_{DN}$ or $V_{DP} = 2.5V$, $0.3V$</td>
<td>-360</td>
<td>+360</td>
<td>nA</td>
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**USB TYPE-C / DYNAMIC PERFORMANCE**

<table>
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<th>UNITS</th>
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<tbody>
<tr>
<td>Analog Switch Turn On Time</td>
<td>$I_{ON}$</td>
<td>$I^{2}$C stop to switch on; $RL = 50\Omega$</td>
<td>0.1</td>
<td>0.3</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Analog Switch Turn Off Time</td>
<td>$I_{OFF}$</td>
<td>$I^{2}$C stop to switch off; $RL = 50\Omega$</td>
<td>0.1</td>
<td>0.3</td>
<td>ms</td>
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**USB TYPE-C / GPIO0, 1, 2, 3, 8**

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<th>MIN</th>
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<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Low Voltage</td>
<td>$V_{IL}$</td>
<td>$0.3 \times V_{IO2}$</td>
<td>V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

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### Electrical Characteristics (continued)

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<tr>
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<tbody>
<tr>
<td>Input High Voltage</td>
<td>$V_{IH}$</td>
<td></td>
<td>$0.7 \times V_{IO2}$</td>
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<tr>
<td>Input Hysteresis (Schmitt)</td>
<td>$V_{IHYS}$</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$I_{SINK} = 2mA$</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
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<tr>
<td>Output High Voltage</td>
<td>$V_{OH}$</td>
<td>$I_{SINK} = 2mA$</td>
<td>$0.7 \times V_{IO2}$</td>
<td></td>
<td></td>
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<tr>
<td>Input Leakage Current</td>
<td>$I_{L}$</td>
<td>$T_A = +25^\circ C$</td>
<td>100</td>
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<td>nA</td>
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<tr>
<td>Input Pullup Resistor</td>
<td>$R_{PU}$</td>
<td></td>
<td>100</td>
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<tr>
<td>Input Pulldown Resistor</td>
<td>$R_{PD}$</td>
<td></td>
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#### USB TYPE-C / GPIO4, 5, 6, 7

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<tr>
<td>Input Low Voltage</td>
<td>$V_{IL}$</td>
<td></td>
<td>$0.3 \times V_{IO1}$</td>
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<tr>
<td>Input High Voltage</td>
<td>$V_{IH}$</td>
<td></td>
<td>$0.7 \times V_{IO1}$</td>
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<tr>
<td>Input Hysteresis (Schmitt)</td>
<td>$V_{IHYS}$</td>
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<td>250</td>
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<td>mV</td>
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<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$I_{SINK} = 2mA$</td>
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<td>0.4</td>
<td></td>
<td>V</td>
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<tr>
<td>Output High Voltage</td>
<td>$V_{OH}$</td>
<td>$I_{SINK} = 2mA$</td>
<td>$0.7 \times V_{IO1}$</td>
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<tr>
<td>Input Leakage Current</td>
<td>$I_{L}$</td>
<td>$T_A = +25^\circ C$</td>
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<td>µA</td>
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<td>Input Pullup Resistor</td>
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<td>kΩ</td>
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<td>Input Pulldown Resistor</td>
<td>$R_{PD}$</td>
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#### USB TYPE-C / I^2C Master / I^2C Logic level

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<th>UNITS</th>
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<tbody>
<tr>
<td>SCL_M, SDA_M Input Low Level</td>
<td></td>
<td>$T_A = +25^\circ C$</td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
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<td>SCL_M, SDA_M Input High Level</td>
<td></td>
<td>$T_A = +25^\circ C$</td>
<td>$0.7 \times V_{IO2}$</td>
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<td></td>
<td>V</td>
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<tr>
<td>SCL_M, SDA_M Input Hysteresis</td>
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<td>$T_A = +25^\circ C$</td>
<td>0.05</td>
<td>$V_{IO2}$</td>
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<td>V</td>
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<tr>
<td>SCL_M, SDA_M Logic Input Current</td>
<td></td>
<td>$SCL_M = SD_AM = V_{IO2} = 5.5V$</td>
<td>-1000</td>
<td>+1000</td>
<td></td>
<td>nA</td>
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<tr>
<td>SCL_M, SDA_M Input Capacitance</td>
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<td>10</td>
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<td></td>
<td>pF</td>
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<tr>
<td>SCL_M, SDA_M Output Low Voltage</td>
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<td>Sinking 3mA</td>
<td>$V_{IO} = HV$</td>
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<td>0.4</td>
<td>V</td>
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<td></td>
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<td>$V_{IO} = LV$</td>
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<td>V</td>
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<tr>
<td>SCL_M, SDA_M Input Leakage Current</td>
<td>$I_{LK}$</td>
<td>$T_A = +25^\circ C$</td>
<td>-1000</td>
<td>+1000</td>
<td></td>
<td>nA</td>
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<td></td>
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<td>$T_A = +85^\circ C$</td>
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<tr>
<td>Clock Frequency</td>
<td>$f_{SCL}$</td>
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<td>1000</td>
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<td>kHz</td>
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## Electrical Characteristics (continued)

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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold Time (Repeated) START Condition</td>
<td>$t_{HD;STA}$</td>
<td></td>
<td>0.26</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>CLK Low Period</td>
<td>$t_{LOW}$</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>CLK High Period</td>
<td>$t_{HIGH}$</td>
<td></td>
<td>0.26</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Setup Time Repeated START Condition</td>
<td>$t_{SU;STA}$</td>
<td></td>
<td>0.26</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>DATA Hold Time</td>
<td>$t_{HD;DAT}$</td>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>DATA Valid Time</td>
<td>$t_{VD;DAT}$</td>
<td></td>
<td>0.45</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>DATA Valid Acknowledge Time</td>
<td>$t_{VD;ACK}$</td>
<td></td>
<td>0.45</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>DATA Setup time</td>
<td>$t_{SU;DAT}$</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Setup Time for STOP Condition</td>
<td>$t_{SU;STO}$</td>
<td></td>
<td>0.26</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Bus-Free Time Between STOP and START</td>
<td>$t_{BUF}$</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Pulse Width of Spikes that Must be Suppressed by the Input Filter</td>
<td>$t_{BUF}$</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### USB TYPE-C / MTP

<table>
<thead>
<tr>
<th>VCIN Input Supply</th>
<th>VCIN_MTP</th>
<th>Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VCIN_MTP</td>
<td>Reading, Erasing, Programming</td>
<td>4.5</td>
<td>5.15</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VCIN Current Consumption</td>
<td>IVCIN_MTP_ERASE</td>
<td>Erasing</td>
<td>8</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>IVCIN_MTP_PROG</td>
<td>Programming</td>
<td>16</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>MTP Erasing / Programming Time</td>
<td>tMTP_ERASE</td>
<td>Erasing (1 page = 128 * 32-bits word)</td>
<td>100</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>tMTP_PROG</td>
<td>Programing</td>
<td>500</td>
<td></td>
<td></td>
<td>μs / 32-bit word</td>
</tr>
<tr>
<td>MTP Write Capacity</td>
<td>NWrite</td>
<td>VDD1P8 = 2V, VCIN = 5.5V</td>
<td>100</td>
<td></td>
<td></td>
<td>Write</td>
</tr>
<tr>
<td>MTP Data Retention</td>
<td>tMTP</td>
<td>VDD1P8 = 2V, VCIN = 5.5V</td>
<td>10</td>
<td></td>
<td></td>
<td>Year</td>
</tr>
</tbody>
</table>

### USB TYPE-C / Power Supply

<table>
<thead>
<tr>
<th>LDO—Output Voltage</th>
<th>$I_L = 1mA$</th>
<th>1.05</th>
<th>1.25</th>
<th>1.2</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDO—Current Limit</td>
<td>-19</td>
<td>-11</td>
<td>-5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>LDO—Power Up Consumption</td>
<td>5</td>
<td>12</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>LDO—Turn On Time</td>
<td>From BMC_PWDN_LDO = 0 to V1P1 = 95% of final value</td>
<td>300</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDO—Output Pulldown Current</td>
<td>VDD1P1 = 1.125V and BMC_LDO_LOAD = 1</td>
<td>330</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Pin Configuration

MAX77958

TOP VIEW
(BUMP SIDE DOWN)

Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>VIO1</td>
<td>System IO Voltage Input. Connect a 1μF/6.3V ceramic capacitor to GND.</td>
</tr>
<tr>
<td>C1</td>
<td>VIO2</td>
<td>System IO Voltage Input. Connect a 1μF/6.3V ceramic capacitor to GND.</td>
</tr>
<tr>
<td>A6</td>
<td>VBUS</td>
<td>VBUS Input. VBUS provides power for internal circuitry when SYS is less than VBUS. Bypass VBUS to GND with a 1μF (min) ceramic capacitor.</td>
</tr>
<tr>
<td>B6</td>
<td>SYS</td>
<td>Power Input. SYS provides power for internal circuitry when VBUS is less than SYS. Bypass SYS to GND with a 1μF (min) ceramic capacitor.</td>
</tr>
<tr>
<td>C6</td>
<td>AVL</td>
<td>Analog Voltage Level. Output of the on-chip LDO is used to power the on-chip and low-noise circuits. Bypass with a 2.2μF/10V ceramic capacitor to GND. Powering external loads from AVL is not recommended, other than pullup resistors.</td>
</tr>
<tr>
<td>B5</td>
<td>VDD1P8</td>
<td>1.8V Internal LDO Output. Bypass the pin to ground with a 1μF/6.3V ceramic capacitor.</td>
</tr>
<tr>
<td>A2</td>
<td>VDD1P1</td>
<td>Digital Supply Voltage of 1.1V. Bypass with a 1μF/6.3V ceramic capacitor.</td>
</tr>
<tr>
<td>B3</td>
<td>SDA</td>
<td>I²C Serial Data. Add an external 2.2kΩ pullup resistor to VIO1.</td>
</tr>
</tbody>
</table>
## Pin Description (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2</td>
<td>SCL</td>
<td>I²C Serial Clock. Add an external 2.2kΩ pullup resistor to VIO1.</td>
</tr>
<tr>
<td>A1</td>
<td>INTB</td>
<td>Interrupt Output. Active-low open-drain output. Add a 200kΩ pullup resistor to VIO1.</td>
</tr>
<tr>
<td>E1</td>
<td>DN1</td>
<td>USB Input 1 for D-</td>
</tr>
<tr>
<td>E2</td>
<td>DP2</td>
<td>USB Input 2 for D+</td>
</tr>
<tr>
<td>D1</td>
<td>DN</td>
<td>Common Negative Output 1. Connect to D- on USB Type-C connector.</td>
</tr>
<tr>
<td>D2</td>
<td>DP</td>
<td>Common Positive Output 2. Connect to D+ on USB Type-C connector.</td>
</tr>
<tr>
<td>A3</td>
<td>CC1</td>
<td>USB Type-C CC Pin 1</td>
</tr>
<tr>
<td>A4</td>
<td>CC2</td>
<td>USB Type-C CC Pin 2</td>
</tr>
<tr>
<td>A5</td>
<td>VCIN</td>
<td>VCONN Power Supply. Supplies VCONN to the unused CC pin if required.</td>
</tr>
<tr>
<td>E6</td>
<td>GPIO0</td>
<td>GPIO0—ADC Input 0</td>
</tr>
<tr>
<td>B4</td>
<td>GPIO1</td>
<td>GPIO1—ADC Input 1</td>
</tr>
<tr>
<td>E5</td>
<td>GPIO2</td>
<td>GPIO2</td>
</tr>
<tr>
<td>D5</td>
<td>GPIO3</td>
<td>GPIO3</td>
</tr>
<tr>
<td>E4</td>
<td>GPIO4</td>
<td>GPIO4</td>
</tr>
<tr>
<td>E3</td>
<td>GPIO5</td>
<td>GPIO5</td>
</tr>
<tr>
<td>D4</td>
<td>GPIO6</td>
<td>SID Selection <a href="#">Table 2</a></td>
</tr>
<tr>
<td>D3</td>
<td>GPIO7</td>
<td>GPIO7</td>
</tr>
<tr>
<td>C4</td>
<td>GPIO8</td>
<td>GPIO8</td>
</tr>
<tr>
<td>C5</td>
<td>GND_A</td>
<td>Analog GND</td>
</tr>
<tr>
<td>D6</td>
<td>GND_D</td>
<td>Digital GND</td>
</tr>
<tr>
<td>C3</td>
<td>SDA_M</td>
<td>Master I²C Serial Data. Add an external 2.2kΩ pullup resistor to VIO2.</td>
</tr>
<tr>
<td>C2</td>
<td>SCL_M</td>
<td>Master I²C Serial Clock. Add an external 2.2kΩ pullup resistor to VIO2.</td>
</tr>
</tbody>
</table>
Detailed Description
The MAX77958 is a robust solution for USB Type-C CC detection and power delivery (PD) protocol implementation. It detects connected accessories or devices by using Type-C CC detection and USB PD messaging. The IC protects against overvoltage and overcurrent, and detects moisture and prevents corrosion on the USB Type-C connector. The IC also has a D+/D- USB switch and BC1.2 detection to support legacy USB standards. It contains V\textsubscript{CONN} switches for USB PD and an enable pin for an external V\textsubscript{CONN} boost or buck converter.

The IC can be used in sink mode to determine the source capabilities of the connected device to optimize power into the sink device. The IC can also be used in source mode to advertise the power capabilities of the source to connected devices and accessories.

The IC is compliant with USB Type-C Version 1.3 and PD 3.0. It can be further customized without affecting the compliance. Customization is available through the customization script in the evaluation kit (EV kit) GUI to support different Maxim chargers.

USB Type-C Interface and Control
The MAX77958 is a complete solution for USB port charger detection and High-Power USB charging on a single USB Type-C connector. It can also be used in any power sink or source application.

The USB Type-C is an internal block that detects connected accessories by using USB Type-C, USB PD messaging and USB BC1.2 charger detection. The USB Type-C block auto-configures switches for common connected accessories including USB cables (SDP/CDP/DCP).

CC/USB PD Interface
The MAX77958 works as a Dual Role Port (DRP) compliant to USB Type-C Version 1.3. The USB Type-C functions are controlled by a logic state machine which follows the USB Type-C requirements. There is support for the optional Try.Sink function which places priority on the sink role. This creates the appearance of legacy operation when the device is connected to another DRP. The IC automatically becomes a sink and draws power from the source. The IC firmware can optionally set an external charger's input current limit based on the current advertised on the CC lines through the master I\textsubscript{2}C interface.

USB Type-C Definitions
- **UFP**—Upstream Facing Port. Typical USB device role for data transfer.
- **DFP**—Down Stream Facing Port. Typical USB host role for data transfer.
- **DRP**—Dual Role Port. USB Type-C port that can operate in either DFP or UFP roles.
- **Source**—Initial power state for a DFP. Power role can be swapped by USB Power Delivery command.
- **Sink**—Initial power state for a UFP. Power role can be swapped by USB Power Delivery command.

DRP
The USB Type-C connector management block supports DRP operation. The port cycles between advertising DFP/source and UFP/sink operations while waiting for a port to be connected. The internal state machine handles all the tasks of detecting and configuring the CC pins for the correct mode. A manual mode allows forcing either DFP or UFP operation in cases where the DRP operation is not appropriate.

Detecting Connected DFP
When a DFP is detected (either from DRP mode or force UFP mode), the USB Type-C Connection State Machine detects the active CC line and reports this with an interrupt to the host application processor (AP). The AP then uses this information to de-mux the SuperSpeed USB lines as required. The USB Type-C Connection State Machine also auto detects the UFP advertised current (default, 1.5A and 3.0A). Upon detection of a change in the advertised current, an interrupt is sent to the AP.
Detecting Connected UFP
When a UFP is detected (either from DRP mode or force DFP mode), the USB Type-C State Machine detects the active CC line. If the Interrupt is enabled, and an AP is present, the IC toggles the INT line to report this to the host AP. Additionally, if an active cable is connected, the IC detects the presence of \( R_A \) on the unconnected CC line to determine if it is necessary to turn on \( V_{CONN} \). The advertised initial supply current is the default USB current (500mA/900mA depending on if SuperSpeed is active). The advertised current can be changed through an \( I^2C \) command or automatically to 1.5A. 3.0A is optionally available but is disabled by default.

Controls
Reported Status and Interrupts
- Connected Device Detection
- Active CC Line
- \( V_{CONN} \) Enabled (\( R_A \) Present)
- Advertised Current in UFP (Source) Mode
- Error State

Operation Controls
- Force Source (DFP) or Sink (UFP) State
- Control Swap of Power Role or \( V_{CONN} \) Role
- Enable/Disable of Audio or Debug Accessories
- Set Advertisement of CC Pin Current in Source Role

Try.SNK Support
The MAX77958 operates as a DRP by default. This type of port can act as either a Power Sink/USB Data Peripheral or a Power Source/USB Data Host. The USB Type-C logic state machine cycles between Source and Sink at a rate typically around 75ms. This means that when the IC is connected to another device, which is also a DRP (for example, PC with a C port), the source and sink roles are randomly assigned. The customer prefers that the mobile phone assumes the sink role if connected to a PC. The IC includes support for Try.SNK, which allows it to be set to strongly prefer the sink role if connected to a standard DRP. If two devices with Try.SNK enable are connected, the role setting is again random.

Audio Accessory Mode Support
The IC detects an audio accessory device when both the CC1 and CC2 pins are pulled down to ground by an \( R_A \) resistor from the connected device.

DebugAccessory.SRC Support
The IC detects a connection to a debug and test system (DTS) when it operates in source power role. A debug accessory device is detected when the CC1 and CC2 pins are pulled down to ground by an \( R_D \) resistor from the connected device.

DebugAccessory.SNK Support
The IC detects a connection to a DTS when it operates in sink power role. A debug accessory device is detected when the CC1 and CC2 pins are pulled up by an \( R_P \) resistor from the connected device. The voltage levels on the CC1 and CC2 pins give the orientation and current capability.

Table 1. Rp/Rp Charging Current Values for a DTS Source

<table>
<thead>
<tr>
<th>MODE OF OPERATION</th>
<th>CC1</th>
<th>CC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default USB Power</td>
<td>Rp for 3A</td>
<td>Rp for 1.5A</td>
</tr>
<tr>
<td>USB Type-C Current at 1.5A</td>
<td>Rp for 1.5A</td>
<td>Rp for Default</td>
</tr>
<tr>
<td>USB Type-C Current at 3A</td>
<td>Rp for 3A</td>
<td>Rp for Default</td>
</tr>
</tbody>
</table>
USB Type-C Interface and Control

Automatic Accessory Detection

Autoconfiguration Details
CCDetEn = 0 or ChgDetEn = 0
1. Nothing happens when \( V_{\text{BUS}} \) is attached. Nothing occurs when ChgDetMan is set to 1.

CCDetEn = 1 and ChgDetEn = 1
1. Charger detection runs automatically when \( V_{\text{BUS}} \) is attached
2. If \( V_{\text{BUS}} \) voltage enters the valid range, all switches connected to DP/DN are opened
3. Charger detection algorithm begins.
4. When charger detection finishes, DP/DN switch settings are restored.

USBAuto = 0
1. No automatic switch configuration happens

USBAuto = 1
1. Operates only after charger detection completes, SDP or CDP is found, and if no special charger is found (SpChgTyp = 000 unknown).
2. Set DP/DN connected to DP2/DN1, over-riding any previous switch setting.
3. At any time, the AP is allowed to change these switch settings.
4. If AP has not changed the switch settings when \( V_{\text{BUS}} \) drops below the valid level, DP/DN sets to Hi-Z.

USB Power Delivery

Description
The IC supports USB Power Delivery Revision 3.0. The power delivery subsystem is separated into 2 parts: Automatic Power Control and Application Processor Message Passthrough.

Automatic Power Control
When a USB Type-C connection is made, the IC automatically handles the initial PD power contract. If a source is connected, the IC reads selects an appropriate voltage and current from the offered capabilities. The IC automatically configures the companion chip input current limit based on the contract if the \( I_{\text{LIM FW}} \) bit is set to 1. The AP may later negotiate a new operating power and manually set the input limiter and charger. If a sink is connected, the IC sends a capabilities message to the attached sink.

Application Processor Message Passthrough
There are many USB PD messages that are unrelated to power control. These messages pass on to the AP to decode and reply. USB PD messages have time critical components and the IC automatically handles these time critical events.

IC Wakeup events
The IC automatically operates in the lowest possible power state. The IC power consumption depends on the following conditions:
- Request has been made across the \( I^2C \) bus
- USB Type-C end-to-end detection is valid
- \( V_{\text{BUS}} \) is present

The lowest possible power consumption state is no \( V_{\text{BUS}} \), CCDetEn = 0, and no \( I^2C \) traffic requests.
Interrupt Output (INTB)
INTB is an open-drain and active-low output. It reports an interrupt event to the main microprocessor. Individual interrupt sources can be masked. Once the main microprocessor reads the interrupt registers, the INTB pin is cleared.

Interconnected Block Diagram

System Faults
The IC monitors the system for the following faults:
- Undervoltage lockout
- VIO fault

Undervoltage Lockout
When the $V_{AVL}$ falls below $AVL\text{UVLOF}$ (2.6V max) for more than 8ms, the MAX77958 enters into a shutdown state. Once the $V_{AVL}$ voltage is higher than $AVL\text{UVLOR}$ (2.8V max), the MAX77958 exits shutdown state to be functional.

VIO Fault
When VIO1 and VIO2 fall below 1.0V, the IC goes into shutdown state. Once VIO1 and VIO2 voltages rise higher than 1.3V, the IC comes out of shutdown state.
Reset Conditions
The IC has different levels of reset as follows:

- **Type S**: Registers are reset each time when VDD1P8 < VDD_OK
- **Type O**: Registers are reset each time when VDD1P8 < VDD_OK or when the software reset command is transmitted (SW_RESET = 0x0F)

WDT Reset
1. Firmware restarts a watchdog timer in 1.86s.
2. If the watchdog timer is not kicked in 1.86s, it executes the following actions:
   a.) MAX77958 reboots
   b.) MAX77958 notifies MA_SYSERROR_BOOT_WDT

I²C Serial Interface
The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration
The I²C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

![Figure 2. Functional Logic Diagram for Communications Controller](image-url)
Bit Transfer
One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of the SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

![Figure 3. I²C Bit Transfer](image)

START and STOP Conditions
When the I²C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the I²C serial interface until the next START condition, minimizing digital noise and feed-through.

![Figure 4. I²C Start and Stop](image)
**Acknowledge**
Both the I²C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

**Slave Address**
The IC acts as a slave transmitter/receiver. The slave address of the IC is 0x4Ah/0x4Bh, 0x4Ch/0x4Dh and 0x4Eh/0x4Fh depending on configuration of GPIO6. The least significant bit is the read/write indicator (1 for read, 0 for write).

<table>
<thead>
<tr>
<th>Table 2. I²C Slave Address</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GPIO6</strong></td>
</tr>
<tr>
<td>GND</td>
</tr>
<tr>
<td>Pullup (330kΩ) to VIO1</td>
</tr>
<tr>
<td>Pulldown (330kΩ) to GND</td>
</tr>
</tbody>
</table>

**Clock Stretching**
In general, the clock signal generation for I²C bus is the responsibility of the master device. I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

**General Call Address**
The IC does not implement an I²C specification general call address. If the IC sees general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

**Communication Speed**
The IC provides I²C 3.0-compatible (1MHz) serial interface.
- I²C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
- Does not Support I²C Clock Stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the “Pullup Resistor Sizing” section of the I²C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V²/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I²C 3.0 specification. The major considerations with respect to the IC are:
- I²C bus master uses current source pullups to shorten the signal rise times.
- \( \text{I}^2\text{C} \) slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the Communication Protocols section.

**Communication Protocols**

The IC supports both writing and reading from its registers.

**Writing to a Single Register**

Figure 5 shows the protocol for the \( \text{I}^2\text{C} \) master device to write one byte of data to the IC. This protocol is the same as SMBus specification’s “Write Byte” protocol.

The “Write Byte” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

<table>
<thead>
<tr>
<th>NUMBER OF BITs</th>
<th>R/W</th>
<th>SLAVE ADDRESS</th>
<th>REGISTER POINTER</th>
<th>DATA</th>
<th>A</th>
<th>P or Sr*</th>
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<td>1</td>
<td>1</td>
<td>8</td>
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</table>

* P FORCES THE BUS FILTERS TO SWITCH TO THEIR ≤ 1MHz MODE. Sr LEAVES THE BUS FILTERS IN THEIR CURRENT STATE.

**Figure 5. Writing to a Single Register**
Writing to Sequential Registers

Figure 6 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The “Writing to Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Figure 6. Writing to Sequential Registers
Reading from a Single Register

The I²C master device reads one byte of data to the IC. This protocol is the same as SMBus specification’s “Read Byte” protocol.

The “Read Byte” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

---

Reading from Sequential Registers

Figure 8 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data—when the master has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.
Figure 8. Reading from Sequential Registers

Engaging HS-Mode for Operation up to 3.4MHz

Figure 9 shows the protocol for engaging HS-Mode operation. HS-Mode operation allows for a bus operating speed up to 3.4MHz.

The “Engaging HS-Mode” protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START command (S).
3. The master sends the 8-bit master code of 0000 1xx0b, where ‘xx’ are don’t care bits.
4. The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5. The master may now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation.

Figure 9. Engaging HS-Mode
The MAX77958 I²C supports the HS mode extension feature. The HS extension feature keeps the high-speed operation even after a ‘STOP’ condition. This eliminates the need for HS master code issued by the I²C master controller when the I²C master controller wants to stay in HS mode for multiple read/write cycles.

As shown in Figure 10, the HS extension mode can be enabled by setting HS_EXT bit in I²C_CFG register (ADDR 0x15) from LS mode only (entering HS extension mode from HS mode is not supported).

*Figure 10. I²C Operating Mode State Diagram*
Register Map

**FUNC**

I²C Slave Address

The MAX77958 has a total of 4 slave addresses. See Table 2 for more information.

**Functional Reset Conditions**

The IC has different levels of reset as follows:

- Type S: Registers are reset each time when VDD1P8 < VDD_OK
- Type O: Registers are reset each time when VDD1P8 < VDD_OK or when the software reset command is transmitted (SW_RESET = 0x0F)

**Functional Register Reset Type Summary**

<table>
<thead>
<tr>
<th>REGISTER ADDRESS (HEX)</th>
<th>REGISTER FUNCTION</th>
<th>REGISTER NAME</th>
<th>RESET TYPE</th>
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<td>UIC_FW_REV</td>
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<tr>
<td>Field</td>
<td>APCmdResI</td>
<td>SYSMsgI</td>
<td>VBUSDetI</td>
<td>VbADCI</td>
<td>DCDTmoI</td>
<td>StopModel</td>
<td>ChgTypI</td>
<td>AttachedHoldl</td>
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<td>Reset</td>
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<tr>
<td>APCmdResI</td>
<td>7</td>
<td>AP Command Response Interrupt</td>
<td>0b0: No interrupt. 0b1: AP command response pending.</td>
</tr>
<tr>
<td>SYSMsgI</td>
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<td>USBC System Message Interrupt</td>
<td>0b0: No interrupt. 0b1: USBC system message pending.</td>
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<td>0b0: No interrupt. 0b1: New VBUSDet status interrupt.</td>
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<tr>
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<td>VBUS Voltage ADC Interrupt</td>
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<td>DCDTmoI</td>
<td>3</td>
<td>DCD Timer Interrupt</td>
<td>0b0: No interrupt. 0b1: New DCDTmo status interrupt.</td>
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<tr>
<td>StopModel</td>
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<td>Stop Mode Interrupt</td>
<td>0b0: No interrupt. 0b1: New stop mode status interrupt.</td>
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<tr>
<td>ChgTypI</td>
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<td>Charger Type Interrupt</td>
<td>0b0: No interrupt. 0b1: New ChgTyp status interrupt.</td>
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<td>AttachedHoldI</td>
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<td>Attached Hold Interrupt</td>
<td>0b0: No interrupt. 0b1: New attached hold status interrupt.</td>
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## PD_INT (0x6)

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<td>VCONN OCP Interrupt</td>
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<td>VSAFE0VI</td>
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<td>VSAFE0V Interrupt</td>
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<td>CC Detection Abort Interrupt</td>
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<td>Wtrl</td>
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<td>Moisture/Dry Interrupt</td>
<td>0b0: No interrupt. 0b1: New moisture/dry status interrupt.</td>
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<td>CCPinStatl</td>
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<td>CC Pin State Interrupt</td>
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<td>CCIStat Interrupt</td>
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## PD_MSG (0x6)

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<td>PD Message Interrupt</td>
<td>0b0: No interrupt. 0b1: New PD message issued.</td>
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<td>DataRoleI</td>
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<td>Data Role Change Interrupt</td>
<td>0b0: No interrupt.  0b1: DataRole status is changed.</td>
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<td>Spare</td>
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<tr>
<td>RSVD</td>
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<td>Spare</td>
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<td>DisplayPortI</td>
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<td>Display Port Interrupt</td>
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Access Type: Read Only

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<td>7:3</td>
<td>Indicates Value on VBUS Input</td>
<td>0x00: VBUS &lt; 3.5V  0x01: 3.5V ≤ VBUS &lt; 4.5V  0x02: 4.5V ≤ VBUS &lt; 5.5V  0x03: 5.5V ≤ VBUS &lt; 6.5V  0x04: 6.5V ≤ VBUS &lt; 7.5V  0x05: 7.5V ≤ VBUS &lt; 8.5V  0x06: 8.5V ≤ VBUS &lt; 9.5V  0x07: 9.5V ≤ VBUS &lt; 10.5V  0x08: 10.5V ≤ VBUS &lt; 11.5V  0x09: 11.5V ≤ VBUS &lt; 12.5V  0x0A: 12.5V ≤ VBUS &lt; 13.5V  0x0B: 13.5V ≤ VBUS &lt; 14.5V  0x0C: 14.5V ≤ VBUS &lt; 15.5V  0x0D: 15.5V ≤ VBUS &lt; 16.5V  0x0E: 16.5V ≤ VBUS &lt; 17.5V  0x0F: 17.5V ≤ VBUS &lt; 18.5V  0x10: 18.5V ≤ VBUS &lt; 19.5V  0x11: 19.5V ≤ VBUS &lt; 20.5V  0x12: 20.5V ≤ VBUS &lt; 21.5V  0x13: 21.5V ≤ VBUS &lt; 22.5V  0x14: 22.5V ≤ VBUS &lt; 23.5V  0x15: 23.5V ≤ VBUS &lt; 24.5V  0x16: 24.5V ≤ VBUS &lt; 25.5V  0x17: 25.5V ≤ VBUS &lt; 26.5V  0x18: 26.5V ≤ VBUS &lt; 27.5V  0x19: 27.5V ≤ VBUS  0x1A: RSVD</td>
</tr>
<tr>
<td>RSVD</td>
<td>2:0</td>
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</table>
### Bitfield Bits Description Decode

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<tr>
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<th>BITS</th>
<th>DESCRIPTION</th>
<th>DECODE</th>
</tr>
</thead>
</table>
| SYSMsg   | 7:0  | SYSMsg      | 0x00: SYSERROR_NONE  
|          |      |             | 0x01: Reserved  
|          |      |             | 0x02: Reserved  
|          |      |             | 0x03: SYSERROR_BOOT_WDT  
|          |      |             | 0x04: SYSERROR_BOOT_SWRSTREQ  
|          |      |             | 0x05: SYSMSG_BOOT_POR  
|          |      |             | 0x10: SYSERROR_HV_NOVBUS  
|          |      |             | 0x11: SYSERROR_HV_FMETHOD_RXPERR  
|          |      |             | 0x12: SYSERROR_HV_FMETHOD_RXBUFOW  
|          |      |             | 0x13: SYSERROR_HV_FMETHOD_RXTFR  
|          |      |             | 0x14: SYSERROR_HV_FMETHOD_MPNACK  
|          |      |             | 0x15: SYSERROR_HV_FMETHOD_RESET_FAIL  
|          |      |             | 0x20: SYSMsg_AFC_Done  
|          |      |             | 0x30: SYSERROR_SYSPOS  
|          |      |             | 0x31: SYSERROR_APCMD_UNKNOWN  
|          |      |             | 0x32: SYSERROR_APCMD_INPROGRESS  
|          |      |             | 0x33: SYSERROR_APCMD_FAIL  |

### BC_STATUS (0xA)

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<tr>
<td>Field</td>
<td>VBUSDet</td>
<td>RSVD</td>
<td>PrChgTyp[2:0]</td>
<td>DCDTmo</td>
<td>ChgTyp[1:0]</td>
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<tr>
<td>Reset</td>
<td>0b0</td>
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<tr>
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<th>BITS</th>
<th>DESCRIPTION</th>
<th>DECODE</th>
</tr>
</thead>
</table>
| VBUSDet  | 7    | Status of VBUS Detection | 0b0: VBUS < VBDET  
|          |      |             | 0b1: VBUS > VBDET |
| RSVD     | 6    | Spare       |        |
| PrChgTyp | 5:3  | Output of Proprietary Charger Detection | 0b000: Unknown  
|          |      |             | 0b001: RSVD  
|          |      |             | 0b010: RSVD  
|          |      |             | 0b011: RSVD  
|          |      |             | 0b100: RSVD  
|          |      |             | 0b101: RSVD  
|          |      |             | 0b110: 3A DCP (If enabled AND chgTyp=DCP)  
|          |      |             | 0b111: Nikon TA (If enabled AND chgTyp=SDP) |
| DCDTmo   | 2    | During Charger Detection, DCD Detection Timed Out. Indicates D+/D- are open. BC1.2 detection continues as required by BC1.2 specification but SDP most likely is found. | 0b0: No timeout or detection has not run.  
|          |      |             | 0b1: DCD timeout occurred. |
| ChgTyp   | 1:0  | Output of Charger Detection | 0b00: Nothing attached.  
|          |      |             | 0b01: SDP, USB cable attached.  
|          |      |             | 0b10: CDP, Charging Downstream Port: current depends on USB operating speed.  
|          |      |             | 0b11: DCP, Dedicated Charger: current up to 1.5A. |
### CC_STATUS0 (0xC)

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**BITFIELD** | **BITS** | **DESCRIPTION** | **DECODE**
--- | --- | --- | ---
CCPinStat | 7:6 | Output of Active CC Pin | 0b00: No determination 0b01: CC1 Active 0b10: CC2 Active 0b11: RFU
CCIStat | 5:4 | CC Pin Detected and Allows VBUS Current in UFP Mode | 0b00: Not in UFP mode 0b01: 500mA 0b10: 1.5A 0b11: 3.0A
CCVcnStat | 3 | Status of VCONN Output | 0b0: VCONN disabled 0b1: VCONN enabled
CCStat | 2:0 | CC Pin State Machine Detection | 0b000: No connection 0b001: SINK 0b010: SOURCE 0b011: Audio accessory 0b100: DebugSrc accessory 0b101: Error 0b110: Disabled 0b111: DebugSnk accessory

### CC_STATUS1 (0xD)

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<tr>
<td>Field</td>
<td>RSVD[1:0]</td>
<td>VCONN OCP</td>
<td>VCONNSC</td>
<td>VSafeOV</td>
<td>DetAbrt</td>
<td>Wtr</td>
<td>RSVD</td>
<td></td>
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<tr>
<td>Reset</td>
<td>0b00</td>
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</table>

**BITFIELD** | **BITS** | **DESCRIPTION** | **DECODE**
--- | --- | --- | ---
RSVD | 7:6 | Spare | 0b0: VCONN current < VCONN_ILIM 0b1: VCONN current > VCONN_ILIM
VCONN OCP | 5 | VCONN Overcurrent Detection | 0b0: VCONN current < VCONN_ILIM 0b1: VCONN current > VCONN_ILIM
VCONNSC | 4 | VCONN Short-Circuit Detection | 0b0: VCONN current < VCONN_SC 0b1: VCONN current > VCONN_SC
VSafeOV | 3 | Status of VBUS Detection. Valid only in Attached.SRC_CCx, Attached.SNK_CCx state. | 0b0: VBUS < VSAFE0V 0b1: VBUS > VSAFE0V
### BITFIELD DESCRIPTION

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<tbody>
<tr>
<td>DetAbrt</td>
<td>2</td>
<td>Charger Detection Abort Status</td>
<td>0b0: Charger detection runs if CHGDetEn = 1 and VBUS is valid for the debounce time. 0b1: Charger detection is aborted by USB Type-C State Machine. Charger does not run if CHGDetEn = 1 and VBUS is valid for the debounce time. CHGDetMan allows manual run of charger detection. If charger detection is in progress, DetAbrt = 1 immediately stops the in progress detection.</td>
</tr>
<tr>
<td>Wtr</td>
<td>1</td>
<td>Moisture/Dry Status</td>
<td>0x0: Dry 0x1: Moisture</td>
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<tr>
<td>RSVD</td>
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### PD_STATUS0 (0xFE)

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<tr>
<td>PDMsg</td>
<td>7:0</td>
<td>PD Message</td>
<td>0x00: Nothing happened 0x01: Sink_PD_PSRdy_received 0x02: Sink_PD_Error Recovery 0x03: Sink_PD_SenderResponseTimer_Timeout 0x04: Source_PD_PSRdy_Sent 0x05: Source_PD_Error Recovery 0x06: Source_PD_SenderResponseTimer_Timeout 0x07: PD_DR_Swap_Request_Received 0x08: PD_PR_Swap_Request_Received 0x09: PD_VCONN_Swap_Request_Received 0x0a: Samsung accessory is attached 0x11: VDM Attention message received</td>
</tr>
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### PD_STATUS1 (0xF)

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<th>BITFIELD</th>
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<tbody>
<tr>
<td>DataRole</td>
<td>7</td>
<td>Current Data Role</td>
<td>0b0: UFP 0b1: DFP</td>
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<tr>
<td>PowerRole</td>
<td>6</td>
<td>Power Role</td>
<td>0b0: Sink 0b1: Source</td>
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<tr>
<td>VCONNS</td>
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<td>VCONNS</td>
<td>0b0: VCONN Sink 0b1: VCONN Source</td>
</tr>
<tr>
<td>PSRDY</td>
<td>4</td>
<td>PSRDY Received as Sink</td>
<td>0b0: Nothing happened 0b1: PSRDY received</td>
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### UIC_INT_M (0x10)

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<tbody>
<tr>
<td>APCmdResM</td>
<td>7</td>
<td>APCmdRes Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
</tr>
<tr>
<td>SYSMsgM</td>
<td>6</td>
<td>SYSMsg Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
</tr>
<tr>
<td>VBUSDetM</td>
<td>5</td>
<td>VBUSDet Interrupt Mask</td>
<td>0 = Unmask 1 = Mask</td>
</tr>
<tr>
<td>VbADCM</td>
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<td>VbADC Interrupt Mask</td>
<td>0 = Unmask 1 = Mask</td>
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<td>DCDTmoM</td>
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<td>DCDTmo Interrupt Mask</td>
<td>0 = Unmask 1 = Mask</td>
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<td>StopModeM</td>
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<td>Fake VBUS Interrupt Mask</td>
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<tr>
<td>ChgTypM</td>
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<td>ChgTyp Interrupt Mask</td>
<td>0 = Unmask 1 = Mask</td>
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<tr>
<td>AttachedHoldM</td>
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<td>UIDADC Interrupt Mask</td>
<td>0 = Unmask 1 = Mask</td>
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### CC_INT_M (0x11)

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<tr>
<td>VCONNOCPM</td>
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<td>VCONNOCP Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
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<tr>
<td>VSAFE0VM</td>
<td>6</td>
<td>VSAFE0V Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
</tr>
<tr>
<td>DetAbrtM</td>
<td>5</td>
<td>DetAbrt Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
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<td>WtrM</td>
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<td>Wtr Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
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<td>CCPinStatM</td>
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<td>CCPinStat Interrupt Mask</td>
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<td>CCIStat Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
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<tr>
<td>CCVcnStatM</td>
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<td>CCVcnStat Interrupt Mask</td>
<td>0b0: Unmask 0b1: Mask</td>
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**PD_INT_M (0x12)**

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<td>Display Port Configure Interrupt Mask</td>
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**AP_DATAOUT0 (0x21)**

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### BITFIELD

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| AP_REQUEST_OPCODE | 7:0 | All configuration and control commands to the USBC are sent and received as a packet using an opcode to identify the packet. **A. Messages sent to the USBC**  
• 0x21—Opcode sent to USBC.  
• 0x22 to 0x41—Message sent to USBC.  
• Message size can be as short as 1 byte (Opcode only) and up to 33 bytes (Opcode plus 32 bytes). But all messages must write to all bytes even if the rest of the message is stuffed with 0s.  
• Registers 0x21 to 0x41 act as a scratch pad for writing the message to the USBC. The message is latched in when a value is written to register 0x41.  
• All messages are acknowledged by the USBC by sending and generating an interrupt.  
• Data written to 0x21 to 0x41 is not auto cleared—the data remains in the registers until the application processor overwrites it with a new message.  
**B. Messages received from USBC**  
• 0x51—Opcode identifying the message type.  
• 0x52 to 0x71—Message sent to application processor.  
• Message size can be as short as 1 byte (Opcode only) and up to 33 bytes (Opcode plus 32 bytes).  
• Data written to 0x51 to 0x71 is not auto cleared—the data remains in the registers until the USBC overwrites them with a new message. |

### AP_DATAOUT1 (0x22)

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<tr>
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### MAX77958

#### Standalone USB Type-C and USB Power Delivery Controller

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MAX77958

Standalone USB Type-C and USB Power Delivery Controller

www.maximintegrated.com
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## MAX77958

Standalone USB Type-C and USB Power Delivery Controller

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MAX77958 Standalone USB Type-C and USB Power Delivery Controller

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### SW_RESET (0x80)

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<td>Access Type</td>
<td>Write, Read</td>
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<td>UIC_SWRST</td>
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<td>UIC (and MAXQ) Software Reset</td>
<td>When AP writes 0xF, UIC is reset (registers and MAXQ).</td>
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### I2C_CNFG (0xE0)

Spare mask register.

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### MAX77958 Standalone USB Type-C and USB Power Delivery Controller

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<td>I²C Pair Address Mode Control</td>
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<td>PAIR[2]: Pair address mode of Shared Bus 3</td>
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<td></td>
<td>channel: Slave ID 3 Functional</td>
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<tr>
<td></td>
<td></td>
<td>Pair address mode option at burst write operation</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>on customer registers.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Pair address mode is enabled for the channel.</td>
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</tr>
<tr>
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<td></td>
<td>0 = Pair address mode is disabled and sequential</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>mode is used.</td>
<td></td>
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<tr>
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<td></td>
<td>PAIR[1]: Pair address mode of Shared Bus 2</td>
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<td>channel: Slave ID 2 Functional</td>
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<td>Pair address mode option at burst write operation</td>
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<tr>
<td></td>
<td></td>
<td>on customer registers.</td>
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</tr>
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<td>1 = Pair address mode is enabled for the channel.</td>
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</tr>
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<td>0 = Pair address mode is disabled and sequential</td>
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<tr>
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<td>mode is used.</td>
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<td>PAIR[0]: Pair address mode of Shared Bus 1</td>
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<td>Pair address mode option at burst write operation</td>
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<td>1 = Pair address mode is enabled for the channel.</td>
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<td>0 = Pair address mode is disabled and sequential</td>
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<td>mode is used.</td>
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<td>HS-mode Extension Control</td>
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<td>0x0: HS-mode Extension is disabled. (I²C Rev. 4</td>
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<td>Compliant)</td>
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<td>0x1: HS-mode Extension is enabled. HS-mode is</td>
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<td>enabled without HS-mode entrance code and</td>
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<td>keeps HS-mode during STOP condition.</td>
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Typical Application Circuits

2/3-Cell Configurable Charger Application

Figure 11 illustrates a configurable charger application diagram using the MAX77958 and buck-boost charger devices. In this application, the USB Type-C connector is used for SINK as well as SOURCE. The SINK role is automatically active when the battery is charged using USB Type-C SOURCE that is connected to the USB Type-C connector in Figure 11. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates power contract with the SOURCE connected to the USB Type-C connector. AP can choose appropriate SOURCE PDO and configure charging current in the buck-boost charger accordingly.

The SOURCE role is active when SINK device is attached to the USB Type-C connector as shown in Figure 11. The IC becomes a power provider with the SOURCE role and advertises its capability to a device connected to USB Type-C connector.

In this scenario, AP configures the buck-boost charger as reverse-buck mode to provide OTG voltage to the device connected to the USB Type-C connector. The communication between the IC.

![Figure 11. Configurable Charger Application](image-url)
2/3-Cell Autonomous Charger Application

Figure 12 illustrates an autonomous charger application diagram using the MAX77958 and a buck-boost charger device. In this application, the USB Type-C connector is used for SINK as well as SOURCE. The SINK role is automatically active when the battery is charged using the USB Type-C SOURCE that is connected to the USB Type-C connector. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates a power contract with the SOURCE connected to the USB Type-C connector. The IC chooses an appropriate SOURCE PDO, and configures charging current in the buck-boost charger accordingly through the master I²C interface in the IC.

The SOURCE role is active when a SINK device is attached to the USB Type-C connector as shown in Figure 12. The IC becomes a power provider with the SOURCE role and advertises its capability to a device connected to USB Type-C connector. In this scenario, the IC configures the buck-boost charger to reverse-buck mode to provide OTG voltage to the device connected to the USB Type-C connector.

Figure 12. Autonomous Charger Application
Typical Application Circuits (continued)

Autonomous DC-DC Application

Figure 13 illustrates an autonomous DC-DC application diagram using the MAX77958. In this application, the USB Type-C connector is used for SINK. Based on the CC detection result, the SOURCE advertises its capability. The IC negotiates a power contract with the SOURCE connected to the USB Type-C connector. The IC chooses an appropriate SINK PDO among PDOs as shown in Figure 13. The IC then sets the Enable on the DC-DC converter to supply power to the application device.

Figure 13. Autonomous DC-DC Application
Typical Application Circuits (continued)

PD Power Adapter Application

Figure 14 illustrates an adapter application diagram using the MAX77958 device. In this application, the USB Type-C connector is only used for SOURCE. The IC negotiates a power contract with the SINK connected to the USB Type-C connector. When SINK is attached, the IC advertises its SOURCE PDO to the SINK. Based on contracts, the IC controls GPIOs to adjust $V_{BUS}$ that the SINK is requesting. When disconnection happens, the IC also controls GPIOs to disconnect the power path on the $V_{BUS}$ path and discharges capacitors on the $V_{BUS}$ path to meet the USB Type-C specification.

![Figure 14. Adapter Application](image)

Ordering Information

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<tr>
<td>MAX77958EWV+</td>
<td>-40°C to +85°C</td>
<td>6x5 WLP, 0.5mm pitch, 3.1mm x 2.65mm</td>
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*Denotes a lead(Pb)-free/RoHS-compliant package.

$T$ = Tape and reel.
### Revision History

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<td>Updated data sheet title, updated $V_{\text{CIN_OK}}$ and added USB Type-C/MTP section to the Electrical Characteristics table, updated AVL in the Pin Description section, updated the Detailed Description and Register Map sections, updated Typical Application Circuits Figures 11, 12, and 13</td>
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