**General Description**

The MAX77827 is a high-efficiency buck-boost regulator targeted for one-cell Li-ion powered applications with the lowest typical quiescent current in the industry of 6μA. It supports input voltages of 1.8V to 5.5V and an output voltage range of 2.3V to 5.3V. The IC provides two different switching current levels (1.8A and 3.1A) to optimize external component sizing based on given load current requirements. With the 1.8A switching current-limit option, the IC can support up to 1.0A load current in buck mode and 900mA in boost mode (V_IN = 3.0V, V_OUT = 3.3V).

The peak efficiency of 96% makes the IC one of the best solutions as a DC/DC converter to supply a rail for battery-powered portable applications.

The IC features an adjustable output voltage, which can be programmed from 2.3V to 5.3V through a single resistor. Two GPIO pins are available to support force PWM enable function and power-OK (POK) indicator. A unique control algorithm allows high-efficiency, outstanding line/load transient response, and seamless transition between buck and boost modes. These options provide design flexibility that allow the IC to cover a wide range of applications and use cases while minimizing board space.

The MAX77827 is available in a 1.61mm x 2.01mm, 12-bump wafer-level package (WLP), and a 2.5mm x 2.5mm, 14-lead FC2QFN package.

**Benefits and Features**

- 1.8V to 5.5V Input Voltage Range
- 2.3V to 5.3V Single Resistor Adjustable Output Voltage
- 1.6A Maximum Output Current (3.1A I_LIM Option, Buck Mode)
- 900mA Maximum Output Current (1.8A I_LIM Option, Boost Mode 3.0V_IN, 3.3V_OUT)
- 96% Peak Efficiency (3.3V_IN, 3.3V_OUT)
- SKIP Mode for Higher Light-Load Efficiency
- 6μA Ultra-Low Typical Quiescent Current (At T_J = +25°C)
- 2.5MHz Nominal Switching Frequency
- Enable Pin
- GPIO Pins for System Design Convenience
  - FPWM (Forced PWM) Mode Selection Pin
  - POK Indicator Pin
- UVLO, Soft-Start, Active-Output Discharge, Overcurrent, and Thermal Shutdown Protections
- 1.61mm x 2.01mm, 12-Bump WLP
- 2.5mm x 2.5mm, 14-Lead FC2QFN

**Applications**

- 1-Cell Li+ Battery Powered Equipment
- Smartphones/Portable/Wearables
- Internet of Things (IoT) Devices
- LPWAN (LTE/NB-IoT, LTE/Cat-M1)

**Simplified Block Diagram**

![Simplified Block Diagram](image-url)
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MAX77827  5.5V Input, 1.8A/3.1A Switch Buck-Boost Converter with 6μA I_Q

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Absolute Maximum Ratings

IN, OUT, BIAS to PGND
-0.3V to +6V
PGND to AGND
-0.3V to +0.3V
EN, SEL, FPWM, POK to AGND
-0.3V to VBIAS + 0.3V
FB to AGND
-0.3V to VOUT + 0.3V
LX1 to PGND
-0.3V to +6.0V
LX2 to PGND
-0.3V to +6.0V
IN, LX1, LX2, OUT Continuous RMS current
1.6A
Operating Junction Temperature Range
-40°C to +125°C

Maximum Junction Temperature
+150°C
Storage Temperature Range
-65°C to +150°C
Soldering Temperature (reflow)
+260°C
Continuous Power Dissipation
WLP Package (T_A = +70°C, derate 13.73mW/°C above +70°C)
1098.4mW
FC2QFN Package (T_A = +70°C, derate 15.77mW/°C above +70°C)
1261.8mW

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 WLP

<table>
<thead>
<tr>
<th>Package Code</th>
<th>W121H2+1</th>
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<tbody>
<tr>
<td>Outline Number</td>
<td>21-100302</td>
</tr>
<tr>
<td>Land Pattern Number</td>
<td>Refer to Application Note 1891</td>
</tr>
</tbody>
</table>

Thermal Resistance, Four-Layer Board:

- Junction to Ambient (θ_JA)
  72.82°C/W
- Junction to Case (θ_JC)
  N/A

14 FC2QFN

<table>
<thead>
<tr>
<th>Package Code</th>
<th>F142A2F+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline Number</td>
<td>21-100382</td>
</tr>
<tr>
<td>Land Pattern Number</td>
<td>90-100127</td>
</tr>
</tbody>
</table>

Thermal Resistance, Four-Layer Board:

- Junction to Ambient (θ_JA)
  63.4°C/W
- Junction to Case (θ_JC)
  N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.
## Electrical Characteristics

(V\(_{\text{IN}}\) = 3.8V, V\(_{\text{OUT}}\) = 3.3V, typicals are at T\(_{\text{A}}\) ≈ T\(_{\text{J}}\) = +25°C. Limits are 100% production tested at T\(_{\text{J}}\) = +25°C. Limits over the operating temperature range (T\(_{\text{J}}\) = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>(V_{\text{IN}})</td>
<td>For A and D options</td>
<td>1.8</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For B and C options</td>
<td>2.6</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>(I_{\text{SHDN}})</td>
<td>EN = Low, T(_{\text{J}}) = +25°C</td>
<td>0.1</td>
<td>2</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EN = Low, T(_{\text{J}}) = -40°C to +125°C (Note 2)</td>
<td>3</td>
<td>8</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Input Supply Current</td>
<td>(I_{\text{Q_SKIP}})</td>
<td>SKIP mode, no switching</td>
<td>6</td>
<td>14</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td></td>
<td>(I_{\text{Q_PWM}})</td>
<td>FPWM mode, no load, no switching</td>
<td>2</td>
<td>6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Active Discharge Resistance</td>
<td>(R_{\text{DISCHG}})</td>
<td>Rising, +20°C hysteresis</td>
<td>100</td>
<td></td>
<td></td>
<td>(\Omega)</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>(T_{\text{SHDN}})</td>
<td>Rising, +20°C hysteresis</td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

### H-BRIDGE

| Output Voltage Range       | \(V_{\text{OUT}}\) | External resistor programmable | 2.3 | 5.3 |     | V     |
|                            | \(V_{\text{OUT\_ACC1}}\) | PWM mode, T\(_{\text{J}}\) = +25°C | -1  | 1   |     | %     |
|                            |                    | PWM mode, T\(_{\text{J}}\) = -40°C to +125°C | -2  | +2  |     |       |
|                            | \(V_{\text{OUT\_ACC2}}\) | SKIP mode, no load, T\(_{\text{J}}\) = +25°C | -1  | +4.5 |    |       |
| Line Regulation            | \(V_{\text{IN}}\) = 1.8V to 5.5V (for A and D options) | 0.4 |     |     | %/V   |
|                            | \(V_{\text{IN}}\) = 2.6V to 5.5V (for B and C options) | 0.4 |     |     |       |
| Load Regulation            | Note 1 | 0.25 |     |     | %/A   |
| Line Transient Response    | \(V_{\text{OS1/VUS1}}\) | \(I_{\text{OUT}} = 0.5\text{A}, V_{\text{IN}}\) changes from 3.4V to 2.9V in 25\(\mu\text{s}\) (20mV/\(\mu\text{s}\)), \(L = 1\mu\text{H}, C_{\text{OUT\_NOM}} = 8\mu\text{F}\) (Note 1) | 50  |     |     | mV    |
| Load Transient Response    | \(V_{\text{OS2/VUS2}}\) | \(I_{\text{OUT}}\) changes from 10mA to 0.5A in 15\(\mu\text{s}\), \(L = 1\mu\text{H}, C_{\text{OUT\_NOM}} = 8\mu\text{F}\) (Note 1) | 250 |     |     | mV    |
| LX1/2 Current Limit        | \(I_{\text{LIM\_LX}}\) | T\(_{\text{J}}\) = -40°C to +125°C, for A and C options | 2.5 | 3.1 | 3.7 | A     |
|                            |                    | T\(_{\text{J}}\) = -40°C to +125°C, for B and D options | 1.3 | 1.8 | 2.3 |       |
| High-Side PMOS On Resistance| \(R_{\text{DSON\_P}}\) | \(I_{\text{LX}} = 100\text{mA per switch}\) | 10  | 130 |     | mΩ    |
| Low-Side NMOS On Resistance| \(R_{\text{DSON\_N}}\) | \(I_{\text{LX}} = 100\text{mA per switch}\) | 15  | 110 |     | mΩ    |
| Switching Frequency        | \(f_{\text{SW}}\) | PWM mode, T\(_{\text{J}}\) = +25°C | 2.25 | 2.5 | 2.75 | MHz   |
|                            |                    | PWM mode, T\(_{\text{J}}\) = -40°C to +125°C | 2.2 | 2.5 | 2.8 |       |
| Turn-On Delay Time         | \(t_{\text{ON\_DLY}}\) | From EN asserting to SEL detection (Note 2) | 100 |     |     | \(\mu\text{s}\) |
| SEL Detection Time         | \(t_{\text{SEL}}\) | After turn-on delay to LX switching (Note 2) | 600 |     |     | \(\mu\text{s}\) |
**Electrical Characteristics (continued)**

(V\(_{\text{IN}}\) = 3.8V, V\(_{\text{OUT}}\) = 3.3V, typicals are at T\(_{\text{A}}\) ≈ T\(_{\text{J}}\) = +25°C. Limits are 100% production tested at T\(_{\text{J}}\) = +25°C. Limits over the operating temperature range (T\(_{\text{J}}\) = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft-Start Time</td>
<td>t(_{\text{SS}})</td>
<td>After SEL detection to soft-start timer finish</td>
<td>(I_{\text{OUT}} = 10\text{mA (Note 1), for B and D options})</td>
<td>1500</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(I_{\text{OUT}} = 10\text{mA (Note 1), for A and C options})</td>
<td>200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Effective Output Capacitance</td>
<td>C(_{\text{EFF_MIN}})</td>
<td>0A &lt; (I_{\text{OUT}}) &lt; 1A</td>
<td>8</td>
<td></td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td>LX1, LX2 Leakage Current</td>
<td>I(_{\text{LK_85}})</td>
<td>(V_{\text{LX1/2}} = 0\text{V or 5.5V, } V_{\text{OUT}} = 5.5\text{V, } V_{\text{IN}} = 5.5\text{V, } T_{\text{J}} = +85^\circ\text{C})</td>
<td>0.1</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>SYS Undervoltage-Lockout Threshold</td>
<td>(V_{\text{UVLO_R}})</td>
<td>SYS rising, options B and C</td>
<td>2.4</td>
<td>2.5</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYS rising, options A and D</td>
<td>1.70</td>
<td>1.75</td>
<td>1.80</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{UVLO_F}})</td>
<td>SYS falling, options B and C</td>
<td>1.9</td>
<td>2.05</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYS falling, options A and D</td>
<td>1.62</td>
<td>1.68</td>
<td>1.74</td>
<td></td>
</tr>
</tbody>
</table>

**ENABLE INPUT (EN)**

| EN Logic-Low Threshold | \(V_{\text{EN_L}}\) | 0.4 | V |
| EN Logic-High Threshold | \(V_{\text{EN_H}}\) | 1.3 | V |

**FPWM INPUT**

| FPWM Logic-Low Threshold | \(V_{\text{IL}}\) | 0.4 | V |
| FPWM Logic-High Threshold | \(V_{\text{IH}}\) | 1.3 | V |
| FPWM Internal Pulldown Resistance | \(R_{\text{PD}}\) | Pulldown resistor to GND | 400 | 800 | 1600 | kΩ |

**POK OUTPUT**

| POK Output Low Voltage | \(V_{\text{POK_L}}\) | \(I_{\text{SINK}} = 1\text{mA}\) | 0.4 | V |
| POK Output High Leakage | \(I_{\text{POK_25C}}\) | \(T_{\text{J}} = +25^\circ\text{C}\) | -1 | +1 | µA |
| POK Threshold | \(I_{\text{POK_R}}\) | \(V_{\text{OUT}}\) rising, expressed as a percentage of \(V_{\text{OUT}}\) | 92.5 | | % |
| | \(I_{\text{POK_F}}\) | \(V_{\text{OUT}}\) falling, expressed as a percentage of \(V_{\text{OUT}}\) | 90 | | |

**Note 1:** Guaranteed by ATE characterization. Not directly tested in production.

**Note 2:** Guaranteed by design. Production tested through scan.
Typical Operating Characteristics

\( V_{\text{IN}} = 3.8V, V_{\text{OUT}} = 3.3V, L = 1\mu H \) (Coilcraft XAL4020-102ME), Skip Mode, \( I_{\text{LIM,LX}} = 1.8A \), \( T_{\text{A}} = +25^\circ C \), unless otherwise noted.

![Graphs showing typical operating characteristics](image-url)
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1\mu H (Coilcraft XAL4020-102ME), Skip Mode, I_{LIM_LX} = 1.8A, T_A = +25°C, unless otherwise noted.)
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1\mu H (Coilcraft XAL4020-102ME), Skip Mode, I_{LIM_LX} = 1.8A, T_A = +25°C, unless otherwise noted.)

5.5V Input, 1.8A/3.1A Switch Buck-Boost Converter with 6\mu A I_Q
Pin Configurations

12 WLP

**MAX77827**
5.5V Input, 1.8A/3.1A Switch Buck-Boost Converter with 6μA I_Q

12 WLP
(1.61mm x 2.01mm, 0.4mm PITCH)

FPWM
PGND
POK
IN
LX1
BIAS
AGND

TOP VIEW
(BUMP SIDE DOWN)

14 FC2QFN

**MAX77827**

14 FC2QFN
(2.5mm x 2.5mm x 0.55mm PITCH)

FPWM
PGND
POK
IN
LX1
BIAS
AGND

TOP VIEW

14 FC2QFN
(2.5mm x 2.5mm x 0.55mm PITCH)
Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
<th>TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 WLP</td>
<td>14 FC2QFN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>8</td>
<td>LX1 Switching Node 1</td>
<td>Power</td>
</tr>
<tr>
<td>A2</td>
<td>6, 7</td>
<td>IN Input. Bypass to PGND with a 10V 10μF capacitor.</td>
<td>Power</td>
</tr>
<tr>
<td>A3</td>
<td>5</td>
<td>BIAS Internal Bias. Bypass to PGND with a 10V 1μF capacitor.</td>
<td>Analog</td>
</tr>
<tr>
<td>A4</td>
<td>4</td>
<td>AGND Analog Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>B1</td>
<td>9</td>
<td>PGND Power Ground</td>
<td>Ground</td>
</tr>
<tr>
<td>B2</td>
<td>14</td>
<td>FPWM FPWM Mode Selection (active-high)</td>
<td>Digital Input</td>
</tr>
<tr>
<td>B3</td>
<td>2</td>
<td>POK Power-OK Open-Drain Output (active-high)</td>
<td>Digital Output</td>
</tr>
<tr>
<td>B4</td>
<td>1</td>
<td>SEL Select the output voltage with resistor (see Table 2).</td>
<td>Analog</td>
</tr>
<tr>
<td>C1</td>
<td>10</td>
<td>LX2 Switching Node 2</td>
<td>Power</td>
</tr>
<tr>
<td>C2</td>
<td>11, 12</td>
<td>OUT Output. Bypass to PGND with a 10V 22μF capacitor.</td>
<td>Power</td>
</tr>
<tr>
<td>C3</td>
<td>13</td>
<td>OUTS Output Sense</td>
<td>Analog</td>
</tr>
<tr>
<td>C4</td>
<td>3</td>
<td>EN Enable Pin</td>
<td>Digital Input</td>
</tr>
</tbody>
</table>

Functional Diagrams

Function Diagram
Detailed Description

Start Up
When the EN pin is set to high, the IC turns on the internal bias circuitry which takes typically 100µs (\(t_{\text{ON-DLY}}\)) to settle. After the internal bias circuitry is settled, the controller senses the SEL pin resistance to set the reference voltage. The \(R_{\text{SEL}}\) reading takes about 600µs (typ). After the IC reads the \(R_{\text{SEL}}\) value, it begins the soft-start process. During the soft-start process, the IC lowers the \(I_{\text{LIM}}\) level from normal \(I_{\text{LIM}}\) level and ramps the output voltage. This prevents the buck-boost from drawing too much current from the input supply during start up. The soft-start process takes 1.5ms (typ) for options B and D, and takes 200µs (typ) for options A and C.

![Start-Up Waveform](image)

The buck-boost is in FPWM mode for the entire duration of \(T_{SS}\). Current limit during soft-start (\(I_{\text{LIM}_{SS}}\)) increases to \(I_{\text{LIM}}\) after approximately half of \(T_{SS}\). See Table 1 for a list of parts with their respective soft-start and normal operation \(I_{\text{LIM}}\) levels.

**Table 1. \(I_{\text{LIM}}\) Levels**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>(I_{\text{LIM}_{SS}}) (A)</th>
<th>(I_{\text{LIM}}) (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX77827BEWC+T, MAX77827BEFD+T, MAX77827DEWC+T, MAX77827DEFD+T</td>
<td>1.15</td>
<td>1.8</td>
</tr>
<tr>
<td>MAX77827AEWC+T, MAX77827AEFD+T, MAX77827CEWC+T, MAX77827CEFD+T</td>
<td>1.8</td>
<td>3.1</td>
</tr>
</tbody>
</table>
Immediate Shutdown Conditions
The following events immediately shutdown the buck-boost:

- Thermal Protection ($T_J > +165^\circ C$)
- $V_{SYS} < SYS$ UVLO Falling Threshold ($V_{UVLO,F}$)

The events in this category shutdown the output until fault conditions are removed from the system.

Power Down
When EN pin is set to low, the IC stops switching and turns on the discharge switches until the output is discharged.

Buck-Boost Regulator
The IC buck-boost regulator utilizes a four-switch H-bridge configuration to realize buck and boost operating modes. This topology maintains output voltage regulation when the input voltage is greater than, equal to, or less than the output voltage. The buck-boost is ideal in one-cell Li-ion battery powered applications and two-cell Alkaline battery powered applications, providing 2.3V to 5.3V of output voltage range. High-switching frequency and a unique control algorithm allow for the smallest solution size, low output noise, and the highest-efficiency across a wide input voltage and output current range.

Buck-Boost Control Scheme
The buck-boost converter operates using a 2.5MHz fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor and output capacitor. The H-bridge topology has three switching phases. See Figure 2 for details.

- **Φ1 Switch period (Phase 1: HS1 = ON, LS2 = ON)** stores energy in the inductor. Inductor current ramps up at a rate proportional to the input voltage divided by inductance: $V_{IN}/L$.
- **Φ2 Switch period (Phase 2: HS1 = ON, HS2 = ON)** ramps inductor current up or down depending on the differential voltage across the inductor: $(V_{IN} - V_{OUT})/L$.
- **Φ3 Switch period (Phase 3: LS1 = ON, HS2 = ON)** ramps inductor current down at a rate proportional to the output voltage divided by inductance: $(-V_{OUT})/L$.

Boost operation ($V_{IN} < V_{OUT}$) utilizes phase 1 and phase 2 within a single clock period. See the representation of inductor current waveform for boost mode operation in Figure 2.

Buck operation ($V_{IN} > V_{OUT}$) utilizes phase 2 and phase 3 within a single clock period. See the representation of inductor current waveform for buck mode operation in Figure 2.
Output Voltage Configuration
The IC allows a SEL pin to configure the output voltage. Resistors with 1% tolerance (or better) should be chosen, with nominal values specified in Table 2.

Table 2. RSEL Selection Table

<table>
<thead>
<tr>
<th>RSEL (kΩ)</th>
<th>VOUT (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>909</td>
<td>2.3</td>
</tr>
<tr>
<td>768</td>
<td>2.4</td>
</tr>
<tr>
<td>634</td>
<td>2.5</td>
</tr>
<tr>
<td>536</td>
<td>2.6</td>
</tr>
<tr>
<td>452</td>
<td>2.7</td>
</tr>
<tr>
<td>383</td>
<td>2.8</td>
</tr>
<tr>
<td>324</td>
<td>2.8</td>
</tr>
<tr>
<td>267</td>
<td>2.85</td>
</tr>
<tr>
<td>191</td>
<td>2.9</td>
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<td>133</td>
<td>3</td>
</tr>
<tr>
<td>113</td>
<td>3</td>
</tr>
<tr>
<td>95.3</td>
<td>3.1</td>
</tr>
<tr>
<td>80.6</td>
<td>3.15</td>
</tr>
<tr>
<td>66.5</td>
<td>3.15</td>
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</table>
Table 2. \textbf{R}_{\text{SEL}} Selection Table (continued)

<table>
<thead>
<tr>
<th>\textbf{R}_{\text{SEL}} (\text{k}\Omega)</th>
<th>\textbf{V}_{\text{OUT}} (V)</th>
</tr>
</thead>
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<tr>
<td>56.2</td>
<td>3.2</td>
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<tr>
<td>Open</td>
<td>3.3</td>
</tr>
<tr>
<td>Short to GND</td>
<td>3.3</td>
</tr>
<tr>
<td>47.5</td>
<td>3.4</td>
</tr>
<tr>
<td>40.2</td>
<td>3.45</td>
</tr>
<tr>
<td>34</td>
<td>3.5</td>
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<tr>
<td>28</td>
<td>3.6</td>
</tr>
<tr>
<td>23.7</td>
<td>3.7</td>
</tr>
<tr>
<td>20</td>
<td>3.75</td>
</tr>
<tr>
<td>16.9</td>
<td>3.8</td>
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<tr>
<td>14</td>
<td>3.9</td>
</tr>
<tr>
<td>11.8</td>
<td>4</td>
</tr>
<tr>
<td>10</td>
<td>4.1</td>
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<tr>
<td>8.45</td>
<td>4.2</td>
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<tr>
<td>7.15</td>
<td>4.4</td>
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<td>5.9</td>
<td>4.5</td>
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<td>4.99</td>
<td>5</td>
</tr>
<tr>
<td>226</td>
<td>5.2</td>
</tr>
<tr>
<td>162</td>
<td>5.3</td>
</tr>
</tbody>
</table>

\textbf{FPWM Mode Enable}

The IC automatically defaults to SKIP mode operation at no load and light load conditions. Transition from skip mode to PWM occurs when load current increases past a certain threshold. Another way to enable PWM operation is by connecting the FPWM pin to logic HIGH level. This forces PWM mode (FPWM) regardless of load current at the output. FPWM mode benefits applications where the lowest output ripple is required, whereas skip mode helps maximize the buck-boost regulator’s efficiency at light loads.

\textbf{Power-OK (POK) Indicator}

The device features an open-drain POK output to monitor the output voltage. The POK pin requires an external pull-up resistor and goes high (high-impedance) after the output increases above 92.5\% (typ) of the target output voltage (\(V_{\text{OUT\_TARGET}}\)). The POK pin goes low when the regulator output drops below 90\% (typ) of \(V_{\text{OUT\_TARGET}}\).

\textbf{Protection Features}

\textbf{Undervoltage Lockout (UVLO)}

The device supports a UVLO feature that prevents operation in abnormal input voltage conditions when \(V_{\text{IN}}\) falls below the \(V_{\text{IN\_UVLO\_F}}\) threshold. Regardless of the EN pin status, the device disables until the input voltage \(V_{\text{IN}}\) rises above the \(V_{\text{IN\_UVLO\_R}}\) threshold.

\textbf{Soft-Start}

The IC is equipped with a soft-start feature to limit large input-current draw from the system supply during device start-up. During the soft-start time, the IC lowers the switching current-limit level from normal level and operates in FPWM mode. See Table 1 for the \(I_{\text{LIM}}\) levels of each part number.
Output Active Discharge
The buck-boost provides an internal 100Ω switch for output active discharge function. The internal switch provides a path to discharge the energy stored in the output capacitor to PGND whenever the regulator is disabled. While the regulator remains enabled, the internal switch is disconnected from the output.

Overcurrent Protection (OCP)
The device features a robust switching current-limit scheme that protects the device and the inductor during overload and fast transient conditions. The current-sense circuit takes current information from the high-side MOSFETs to determine the peak-switching current ($R_{DS(ON)} \times I_L$).

The IC provides two different cycle-by-cycle current limit levels (1.8A (typ) and 3.1A (typ)) for the high-side MOSFET. If the switching current ($I_{LIM}$) hits current limit for about 3ms, the IC shuts off the output for about 12ms, retries, and repeats this cycle until the over-current condition is removed from the system.

![Figure 3. Short-Circuit Waveform](image)

Thermal Shutdown
The device has an internal thermal-protection circuit which monitors die temperature. The buck-boost disables if the die temperature exceeds $T_{SHDN}$ (+165°C typ). The buck-boost enables again after the die temperature cools by approximately +20°C.
Applications Information

Inductor Selection

Buck-boost is optimized for a 1µH inductance. The lower the inductor DCR, the higher the buck-boost efficiency. Users need to trade off inductor size with DCR value and choose a suitable inductor for the buck-boost.

The saturation current of the inductor should be higher than the maximum switching current limit to avoid inductor saturation during operation. See the Electrical Characteristics table specifications for the maximum I_{LM} of each IC option. Table 3 lists recommended inductors for the IC. Always choose the inductor carefully by consulting the manufacturer’s latest released data sheet.

Table 3. Inductor Recommendations

<table>
<thead>
<tr>
<th>MFGR.</th>
<th>SERIES</th>
<th>NOMINAL INDUCTANCE (µH)</th>
<th>TYPICAL DC RESISTANCE (mΩ)</th>
<th>CURRENT RATING (A)</th>
<th>CURRENT RATING (A)</th>
<th>CURRENT RATING (A)</th>
<th>OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-30 (ΔL/L)</td>
<td>ΔT = 40°C RISE</td>
<td>ΔT = 40°C RISE</td>
<td></td>
</tr>
<tr>
<td>Murata</td>
<td>DFE18SBN1R0ME0</td>
<td>1.0</td>
<td>120</td>
<td>3.1</td>
<td>2.4</td>
<td>1.6 x 0.8 x 0.8</td>
<td>B, D</td>
</tr>
<tr>
<td>Samsung</td>
<td>CIGT201610EH1R0MNE</td>
<td>1.0</td>
<td>38</td>
<td>4.5</td>
<td>4.3</td>
<td>2.0 x 1.6 x 1.0</td>
<td>A, B, C, D</td>
</tr>
<tr>
<td>Taiyo-Yuden</td>
<td>MEKK2016H1ROM</td>
<td>1.0</td>
<td>41</td>
<td>4.5</td>
<td>3.7</td>
<td>2.0 x 1.6 x 1.0</td>
<td>A, B, C, D</td>
</tr>
<tr>
<td>Cyntec</td>
<td>HTEH20120H-1R0MSR</td>
<td>1.0</td>
<td>45</td>
<td>3.8</td>
<td>3.5</td>
<td>2.0 x 1.2 x 0.8</td>
<td>A, B, C, D</td>
</tr>
<tr>
<td>Samsung</td>
<td>CIGT252010EH1ROMNE</td>
<td>1.0</td>
<td>26</td>
<td>5.0</td>
<td>4.3</td>
<td>2.5 x 2.0 x 1.0</td>
<td>A, B, C, D</td>
</tr>
<tr>
<td>Sumida</td>
<td>CDMT4OD20HF-1R0NC</td>
<td>1.0</td>
<td>26</td>
<td>8.7</td>
<td>9.6</td>
<td>4.3 x 4.3 x 2.1</td>
<td>A, B, C, D</td>
</tr>
<tr>
<td>Coilcraft</td>
<td>XAL4020-102MEB</td>
<td>1.0</td>
<td>13</td>
<td>8.7</td>
<td>9.6</td>
<td>4.0 x 4.0 x 2.1</td>
<td>A, B, C, D</td>
</tr>
</tbody>
</table>

Input Capacitor Selection

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10V 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor, C_{OUT}, is required to keep the output-voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, the buck-boost requires 8µF of minimum effective output capacitance. Considering DC bias characteristic of ceramic capacitors, a 10V 22µF capacitor is recommended for most applications.
PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 5 shows an example PCB layout for the MAX77827 FC2QFN package. For the WLP package, a high density interconnect (HDI) PCB is required. Figure 4 shows an example HDI PCB layout for the MAX77827 WLP package.

When designing the PCB, follow these guidelines:

1. Place the input capacitors \( C_{in} \) and output capacitors \( C_{out} \) immediately next to the IN pin and OUT pin, respectively, of the IC. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.

2. Place the inductor next to the LX bumps/pins (as close as possible) and make the traces between the LX bumps/pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Furthermore, do not allow LX traces to take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.

3. Prioritize the low-impedance ground plane of the PCB directly underneath the IC, \( C_{out} \), \( C_{in} \), and the inductor. Cutting this ground plane risks interrupting the switching current loops.

4. AGND must carefully connect to PGND on the PCBs low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.

5. The IC requires a supply input (BIAS) which is often the same net as IN. Carefully bypass BIAS to PGND with a dedicated capacitor (\( C_{bias} \)) as close as possible to the IC. Route a dedicated trace between \( C_{bias} \) and the BIAS bump/pin. Avoid connecting BIAS directly to the nearest IN bumps/pins without dedicated bypassing.

6. Connect the OUTS bump/pin to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.

7. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.

8. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the Output Capacitor Selection section and refer to Tutorial 5527 for more information.

Figure 4. PCB Layout Example (WLP—B and D Options)
Figure 5. PCB Layout Example (FC2QFN—B and D Options)

Typical Application Circuits

Typical Application Circuit
## Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TYP I\textsubscript{LIM} (A)</th>
<th>UVLO RISING MAX (V)</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX77827AEWC+T</td>
<td>3.1</td>
<td>1.8</td>
<td>12 WLP</td>
</tr>
<tr>
<td>MAX77827BEWC+T</td>
<td>1.8</td>
<td>2.6</td>
<td>12 WLP</td>
</tr>
<tr>
<td>MAX77827CEWC+T</td>
<td>3.1</td>
<td>2.6</td>
<td>12 WLP</td>
</tr>
<tr>
<td>MAX77827DEWC+T</td>
<td>1.8</td>
<td>1.8</td>
<td>12 WLP</td>
</tr>
<tr>
<td>MAX77827AEFD+T</td>
<td>3.1</td>
<td>1.8</td>
<td>14 FC2QFN</td>
</tr>
<tr>
<td>MAX77827BEFD+T</td>
<td>1.8</td>
<td>2.6</td>
<td>14 FC2QFN</td>
</tr>
<tr>
<td>MAX77827CEFD+T</td>
<td>3.1</td>
<td>2.6</td>
<td>14 FC2QFN</td>
</tr>
<tr>
<td>MAX77827DEFD+T</td>
<td>1.8</td>
<td>1.8</td>
<td>14 FC2QFN</td>
</tr>
</tbody>
</table>

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
Revision History

<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
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<tr>
<td>0</td>
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<td>Initial release</td>
<td>—</td>
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<tr>
<td>1</td>
<td>5/19</td>
<td>Updated Ordering Information table</td>
<td>22</td>
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<tr>
<td>2</td>
<td>6/19</td>
<td>Updated Ordering Information table</td>
<td>22</td>
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<td>3</td>
<td>10/19</td>
<td>Updated General Description, Applications, Benefits and Features, and Package Information sections, replaced all Typical Operating Characteristics and FC2QFN Pin Configuration, updated Pin Description table, Table 1, Figure 2, and Table 3, replaced PCB Layout Guidelines section, updated Ordering Information table</td>
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<td>8/21</td>
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<td>16, 17</td>
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