**General Description**

The MAX6920 is a 12-output, 76V, vacuum fluorescent display (VFD) tube driver that interfaces a multiplexed VFD tube to a VFD controller such as the MAX6850–MAX6853 or to a microcontroller. The MAX6920 is also ideal for driving either static VFD tubes or telecom relays.

Data is inputted using an industry-standard 4-wire serial interface (CLOCK, DATA, LOAD, BLANK) for compatibility with both industry-standard drivers and Maxim's VFD controllers.

For easy display control, the active-high BLANK input forces all driver outputs low, turning the display off, and automatically puts the MAX6920 into shutdown mode. Display intensity may also be controlled by pulse-width modulating the BLANK input.

The MAX6920 has a serial interface data output pin, DOUT, allowing any number of devices to be cascaded on the same serial interface.

The MAX6920 is available in a 20-pin SO package. Maxim also offers VFD drivers with either 20 (MAX6921/MAX6931) or 32 outputs (MAX6922 and MAX6932).

**Applications**

- White Goods
- Gaming Machines
- Avionics
- Industrial Weighing
- Security
- Telecom

**Features**

- 5MHz Industry-Standard 4-Wire Serial Interface
- 3V to 5.5V Logic Supply Range
- 8V to 76V Grid/Anode Supply Range
- Push-Pull CMOS High-Voltage Outputs
- Outputs can Source 40mA, Sink 4mA Continuously
- Outputs can Source 75mA Repetitive Pulses
- Outputs can be Paralleled for Higher Current Drive
- Any Output can be Used as a Grid or an Anode Driver
- Blank Input Simplifies PWM Intensity Control
- Small 20-Pin SO Package
- -40°C to +125°C Temperature Range

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX6920AWP</td>
<td>-40°C to +125°C</td>
<td>20 Wide SO</td>
</tr>
</tbody>
</table>

**Pin Configuration**

**Typical Operating Circuit**
**Absolute Maximum Ratings**

Voltage (with respect to GND)
- \( V_{BB} \): -0.3V to +80V
- \( V_{CC} \): -0.3V to +6V
- \( \text{OUT}_\text{Sink} \): -0.3V to \((V_{BB} + 0.3V)\)
- All Other Pins: -0.3V to \((V_{CC} + 0.3V)\)
- \( \text{OUT}_\text{Continuous Source Current} \): -45mA
- \( \text{OUT}_\text{Pulsed (1ms max, 1/4 max duty) Source Current} \): -80mA
- Total \( \text{OUT}_\text{Continuous Source Current} \): -540mA
- Total \( \text{OUT}_\text{Continuous Sink Current} \): 60mA
- Total \( \text{OUT}_\text{Pulsed (1ms max, 1/4 max duty)} \text{Source Current} \): -960mA
- Source Current: -960mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Electrical Characteristics**

(Typical Operating Circuit, \( V_{BB} = 8\)V to 76V, \( V_{CC} = 3\)V to 5.5V, \( T_A = T_{MIN} \) to \( T_{MAX} \), unless otherwise noted.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Supply Voltage</td>
<td>( V_{CC} )</td>
<td>All outputs ( \text{OUT}_\text{low}, \text{CLK} = \text{idle} ) ( T_A = +25)°C</td>
<td>3</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Tube Supply Voltage</td>
<td>( V_{BB} )</td>
<td>All outputs ( \text{OUT}_\text{low}, \text{CLK} = \text{idle} ) ( T_A = -40)°C to +125°C</td>
<td>8</td>
<td>76</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Supply Operating Current</td>
<td>( I_{CC} )</td>
<td>All outputs ( \text{OUT}_\text{low}, \text{CLK} = \text{idle} ) ( T_A = +25)°C</td>
<td>72</td>
<td>170</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All outputs ( \text{OUT}_\text{high}, \text{CLK} = \text{idle} ) ( T_A = +40)°C to +125°C</td>
<td>200</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tube Supply Operating Current</td>
<td>( I_{BB} )</td>
<td>All outputs ( \text{OUT}_\text{low} ) ( T_A = +25)°C</td>
<td>1</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All outputs ( \text{OUT}_\text{high} ) ( T_A = -40)°C to +125°C</td>
<td>4.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-Voltage ( \text{OUT}_\text{low} )</td>
<td>( V_H )</td>
<td>( V_{BB} \geq 15)V, ( I_{OUT} = -25mA ) ( T_A = +25)°C</td>
<td>( V_{BB} - 1.1 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +85°C ( V_{BB} = 2 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +125°C ( V_{BB} = 2.5 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{BB} \geq 15)V, ( I_{OUT} = -40mA )</td>
<td>( T_A = +25)°C</td>
<td>( V_{BB} - 3.5 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +85°C ( V_{BB} = 4.0 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +125°C ( V_{BB} = 4.0 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-Voltage ( \text{OUT}_\text{low} )</td>
<td>( V_L )</td>
<td>( V_{BB} \geq 15)V, ( I_{OUT} = 1mA ) ( T_A = +25)°C</td>
<td>0.75</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +85°C</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +125°C</td>
<td>1.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( 8V &lt; V_{BB} &lt; 15)V, ( I_{OUT} = 1mA )</td>
<td>( T_A = +25)°C</td>
<td>0.8</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +85°C</td>
<td>1.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( T_A = -40)°C to +125°C</td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Continuous Power Dissipation**
- 20-Pin Wide SO (derate 10mW/°C over \( T_A = +70\)°C) ... 800mW

**Operating Temperature Range** (\( T_{MIN} \) to \( T_{MAX} \))
- -40°C to +125°C

**Junction Temperature**
- +150°C

**Storage Temperature Range**
- -65°C to +150°C

**Lead Temperature (soldering, 10s)**
- +300°C

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**Electrical Characteristics (continued)**

(Typical Operating Circuit, V_{BB} = 8V to 76V, V_{CC} = 3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time OUT_ (20% to 80%)</td>
<td>t_R</td>
<td>V_{BB} = 60V, C_L = 50pF, R_L = 2.3kΩ</td>
<td>0.9</td>
<td>2</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Fall Time OUT_ (80% to 20%)</td>
<td>t_F</td>
<td>V_{BB} = 60V, C_L = 50pF, R_L = 2.3kΩ</td>
<td>0.6</td>
<td>1.5</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**SERIAL INTERFACE TIMING CHARACTERISTICS**

| LOAD Rising to OUT_ Falling Delay      |          | (Notes 2, 3)                             | 0.9 | 1.8 |     | µs    |
| LOAD Rising to OUT_ Rising Delay       |          | (Notes 2, 3)                             | 1.2 | 2.4 |     | µs    |
| BLANK Rising to OUT_ Falling Delay     |          | (Notes 2, 3)                             | 0.9 | 1.8 |     | µs    |
| BLANK Falling to OUT_ Rising Delay     |          | (Notes 2, 3)                             | 1.3 | 2.5 |     | µs    |
| Input Leakage Current                  | I_{IH}, I_{IL} |                                      | 0.05 | 10  |     | µA    |
| Logic-High Input Voltage               | V_{IH}  |                                       | 0.8 x V_{CC} |       |       | V    |
| Logic-Low Input Voltage                | V_{IL}  |                                       | 0.3 x V_{CC} |       |       | V    |
| Hysteresis Voltage                     | ΔV_{I}  |                                       | 0.6 |     |     | V    |
| High-Voltage DOUT                      | V_{OH}  | I_{SOURCE} = -1.0mA                    | V_{CC} - 0.5 |     |       | V    |
| Low-Voltage DOUT                       | V_{OL}  | I_{SINK} = 1.0mA                       | 0.5 |     |     | V    |
| Rise and Fall Time DOUT                | C_{DOUT} = 10pF |                                 | 3V to 4.5V | 60  | 100  | ns  |
|                                        |         |                                         | 4.5V to 5.5V | 30  | 80   | ns  |
| CLK Clock Period                       | t_{CP} |                                       | 200 |     |     | ns    |
| CLK Pulse-Width High                  | t_{CH} |                                       | 90  |     |     | ns    |
| CLK Pulse-Width Low                   | t_{CL} |                                       | 90  |     |     | ns    |
| CLK Rise to LOAD Rise Hold Time       | t_{CSH} | (Note 2)                               | 100 |     |     | ns    |
| DIN Setup Time                         | t_{DS} |                                       | 5   |     |     | ns    |
| DIN Hold Time                          | t_{DH} | 3V to 4.5V                             | 20  |     |     | ns    |
|                                        |         | 4.5V to 5.5V                           | 15  |     |     | ns    |
| DOUT Propagation Delay                 | t_{DO} | C_{DOUT} = 10pF                      | 3.0V to 4.5V | 25  | 120  | 240  | ns  |
|                                        |         |                                         | 4.5V to 5.5V | 20  | 75   | 150  | ns  |
| LOAD Pulse High                        | t_{CSW} |                                           | 55  |     |     | ns    |

**Notes:**
- **Note 1:** All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
- **Note 2:** Guaranteed by design.
- **Note 3:** Delay measured from control edge to when output OUT_ changes by 1V.

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Typical Operating Characteristics

(V_{CC} = 5.0\text{V}, \, V_{BB} = 76\text{V}, \text{ and } T_A = +25^\circ\text{C}, \text{ unless otherwise noted.})

**TUBE SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS LOW)**
- **vs. TEMPERATURE (OUTPUTS HIGH)**

**LOGIC SUPPLY CURRENT (I_{CC})**

- **vs. TEMPERATURE (OUTPUTS LOW)**

**SUPPLY CURRENT (I_{CC})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT VOLTAGE (V_{BB} - V_{IH})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT RISE AND FALL WAVEFORM**

**SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS LOW)**

**TUBE SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS LOW)**

**SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT VOLTAGE (V_{BB} - V_{IH})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT RISE AND FALL WAVEFORM**

**SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS LOW)**

**TUBE SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS LOW)**

**SUPPLY CURRENT (I_{BB})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT VOLTAGE (V_{BB} - V_{IH})**

- **vs. TEMPERATURE (OUTPUTS HIGH)**

**OUTPUT RISE AND FALL WAVEFORM**
### Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_{BB}</td>
<td>VFD Tube Supply Voltage</td>
</tr>
<tr>
<td>2</td>
<td>DOUT</td>
<td>Serial-Clock Output. Data is clocked out of the internal shift register to DOUT on CLK’s rising edge.</td>
</tr>
<tr>
<td>3–8, 13–18</td>
<td>OUT0 to OUT11</td>
<td>VFD Anode and Grid Drivers. OUT0 to OUT11 are push-pull outputs swinging from V_{BB} to GND.</td>
</tr>
<tr>
<td>9</td>
<td>BLANK</td>
<td>Blanking Input. High forces outputs OUT0 to OUT11 low, without altering the contents of the output latches. Low enables outputs OUT0 to OUT11 to follow the state of the output latches.</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>CLK</td>
<td>Serial-Clock Input. Data is loaded into the internal shift register on CLK’s rising edge.</td>
</tr>
<tr>
<td>12</td>
<td>LOAD</td>
<td>Load Input. Data is loaded transparently from the internal shift register to the output latch while LOAD is high. Data is latched into the output latch on LOAD’s rising edge, and retained while LOAD is low.</td>
</tr>
<tr>
<td>19</td>
<td>DIN</td>
<td>Serial-Data Input. Data is loaded into the internal shift register on CLK’s rising edge.</td>
</tr>
<tr>
<td>20</td>
<td>V_{CC}</td>
<td>Logic Supply Voltage</td>
</tr>
</tbody>
</table>

![Figure 1. MAX6920 Functional Diagram](image-url)
Detailed Description

The MAX6920 is a VFD tube driver comprising a 4-wire serial interface driving 12 high-voltage rail-to-rail output ports. The driver is suitable for both static and multiplexed displays.

The output ports feature high current-sourcing capability to drive current into grids and anodes of static or multiplex VFDs. The ports also have active current sinking for fast discharge of capacitive display electrodes in multiplexing applications.

The 4-wire serial interface comprises a 12-bit shift register and a 12-bit transparent latch. The shift register is written through a clock input CLK and a data input DIN and the data propagates to a data output DOUT. The data output allows multiple drivers to be cascaded and operated together. The output latch is transparent to the shift register outputs when LOAD is high, and latches the current state on the falling edge of LOAD.

Each driver output is a slew-rated controlled CMOS push-pull switch driving between \( V_{BB} \) and GND. The output rise time is always slower than the output fall time to avoid shoot-through currents during output transitions. The output slew rates are slow enough to minimize EMI, yet are fast enough so as not to impact the typical 100\( \mu \)s digit multiplex period and affect the display intensity.

Initial Power-Up and Operation

An internal reset circuit clears the internal registers of the MAX6920 on power-up. All outputs OUT0 to OUT11 and the interface output DOUT initialize low regardless of the initial logic levels of the CLK, DIN, BLANK, and LOAD inputs.

4-Wire Serial Interface

The MAX6920 uses a 4-wire serial interface with three inputs (DIN, CLK, LOAD) and a data output (DOUT). This interface is used to write output data to the MAX6920 (Figure 3) (Table 1). The serial interface data word length is 12 bits, D0–D11.

The functions of the four serial interface pins are:

- CLK input is the interface clock, which shifts data into the MAX6920’s 12-bit shift register on its rising edge.
- LOAD input passes data from the MAX6920’s 12-bit shift register to the 12-bit output latch when LOAD is high (transparent latch), and latches the data on LOAD’s falling edge.

![Figure 2. MAX6920 CMOS Output Driver Structure](https://www.maximintegrated.com/datasheet-pdf-pdf-fillable_MAX6920.pdf)

![Figure 3. 4-Wire Serial Interface Timing Diagram](https://www.maximintegrated.com/datasheet-pdf-pdf-fillable_MAX6920.pdf)
DIN is the interface data input, and must be stable when it is sampled on the rising edge of CLK.

DOUT is the interface data output, which shifts data out from the MAX6920's 12-bit shift register on the falling edge of CLK. Data at DIN is propagated through the shift register and appears at DOUT (20 CLK cycles + \( t_{DO} \)) later.

A fifth input pin, BLANK, can be taken high to force outputs OUT0 to OUT11 low, without altering the contents of the output latches. When the BLANK input is low, outputs OUT0 to OUT11 follow the state of the output latches. A common use of the BLANK input is PWM intensity control. The BLANK input's function is independent of the operation of the serial interface. Data can be shifted into the serial interface shift register and latched regardless of the state of BLANK.

### Writing Device Registers Using the 4-Wire Serial Interface

The MAX6920 is written using the following sequence:

1) Take CLK low.
2) Clock 12 bits of data in order D11 first to D0 last into DIN, observing the data setup and hold times.
3) Load the 12 output latches with a falling edge on LOAD.

LOAD may be high or low during a transmission. If LOAD is high, then the data shifted into the shift register at DIN appears at the OUT0 to OUT11 outputs.

CLK and DIN may be used to transmit data to other peripherals. Activity on CLK always shifts data into the MAX6920's shift register. However, the MAX6920 only updates its output latch on the rising edge of LOAD, and the last 12 bits of data are loaded. Therefore, multiple devices can share CLK and DIN as long as they have unique LOAD controls.

### Determining Driver Output Voltage Drop

The outputs are CMOS drivers, and have a resistive characteristic. The typical and maximum sink and source output resistances can be calculated from the \( V_H \) and \( V_L \) electrical characteristics. Use this calculated resistance to determine the output voltage drop at different output currents.

### Output Current Ratings

The continuous current source capability is 40mA per output. Outputs may drive up to 75mA as a repetitive peak current, subject to the on time (output high) being no longer than 1ms, and the duty cycle being such that the output power dissipation is no more than the dissipation for the continuous case. The repetitive peak rating allows outputs to drive a higher current in multiplex grid driver applications, where only one grid is on at a time, and the multiplex time per grid is no more than 1ms.

---

**Table 1. 4-Wire Serial Interface Truth Table**

<table>
<thead>
<tr>
<th>SERIAL DATA INPUT</th>
<th>CLOCK</th>
<th>SHIFT REGISTER CONTENTS</th>
<th>LOAD INPUT</th>
<th>LATCH CONTENTS</th>
<th>BLANKING INPUT</th>
<th>OUTPUT CONTENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIN</td>
<td>CLK</td>
<td>D0 D1 D2 ... Dn-1 Dn</td>
<td>LOAD D0 D1 D2 ... Dn-1 Dn</td>
<td>LOAD D0 D1 D2 ... Dn-1 Dn</td>
<td>BLANK D0 D1 D2 ... Dn-1 Dn</td>
<td>OUTPUT D0 D1 D2 ... Dn-1 Dn</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>H</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>L</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
<td>R0 R1 R2 ... Rn-2 Rn</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X X X ... X X L</td>
<td>X X P0 P1 P2 ... Pn-1 Pn</td>
<td>X X P0 P1 P2 ... Pn-1 Pn</td>
<td>X X P0 P1 P2 ... Pn-1 Pn</td>
<td>X X P0 P1 P2 ... Pn-1 Pn</td>
</tr>
</tbody>
</table>

- \( L \) = Low logic level.
- \( H \) = High logic level.
- \( X \) = Don't care.
- \( P \) = Present state (shift register).
- \( R \) = Previous state (latched).
Since dissipation is proportional to current squared, the maximum current that can be delivered for a given multiplex ratio is given by:

$$I_{\text{PEAK}} = (\text{grids} \times 1600)^{1/2} \text{mA}$$

where grids is the number of grids in a multiplexed display. This means that a duplex application (two grids) can use a repetitive peak current of 56.5mA, a triplex application (three grids) can use a repetitive peak current of 69.2mA, and higher multiplex ratios are limited to 75mA.

**Paralleling Outputs**

Any number of outputs within the same package may be paralleled in order to raise the current drive or reduce the output resistance. Only parallel outputs directly (by shorting outputs together) if the interface control can be guaranteed to set the outputs to the same level. Although the sink output is relatively weak (typically 750\(\Omega\)), that resistance is low enough to dissipate 530mW when shorted to an opposite level output at a V\(_{BB}\) voltage of only 20V. A safe way to parallel outputs is to use diodes to prevent the outputs from sinking current (Figure 4). Because the outputs cannot sink current from the VFD tube, an external discharge resistor, \(R\), is required. For static tubes, \(R\) can be a large value such as 100k\(\Omega\). For multiplexed tubes, the value of the resistor can be determined by the load capacitance and timing characteristics required. Resistor \(R\) discharges tube capacitance C to 10% of the initial voltage in 2.3 x RC seconds. So, for example, a 15k\(\Omega\) value for \(R\) discharges 100pF tube grid or anode from 40V to 4V in 3.5\(\mu\)s, but draws an additional 2.7mA from the driver when either output is high.

**Power Dissipation**

Take care to ensure that the maximum package dissipation ratings for the chosen package are not exceeded. Over dissipation is unlikely to be an issue when driving static tubes, but the peak currents are usually higher for multiplexed tubes. When using multiple driver devices, try to share the average dissipation evenly between the drivers.

Determine the power dissipation (\(P_D\)) for the MAX6920 for static tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{\text{ANODE}} \times A))$$

where:

- \(A\) = number of anodes driven (a MAX6920 can drive a maximum of 12).
- \(I_{\text{ANODE}}\) = maximum anode current.
- \((V_{BB} - V_H)\) is the output voltage drop at the given maximum anode current \(I_{OUT}\).

A static tube dissipation example follows:

\[V_{CC} = 5V \pm 5\%, V_{BB} = 10V\] to 18V, \(A = 12, I_{OUT} = 2mA\)

\[P_D = (5.25V \times 0.7mA) + (18V \times 0.9mA) + ((2.5V \times 2mA/25mA) \times 2mA \times 12) = 24.7mW\]

Determine the power dissipation (\(P_D\)) for the MAX6920 for multiplex tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{\text{ANODE}} \times A)) + ((V_{BB} - V_H) \times I_{\text{GRID}}))$$

where:

- \(A\) = number of anodes driven
- \(G\) = number of grids driven
- \(I_{\text{ANODE}}\) = maximum anode current
- \(I_{\text{GRID}}\) = maximum grid current

The calculation presumes all anodes are on but only one grid is on. The calculated \(P_D\) is the worst case, presuming one digit is always being driven with all its anodes lit. Actual \(P_D\) can be estimated by multiplying this \(P_D\) figure by the actual tube drive duty cycle, taking into account interdigit blanking and any PWM intensity control.

A multiplexed tube dissipation example follows:

\[V_{CC} = 5V \pm 5\%, V_{BB} = 36V\] to 42V, \(A = 6, G = 6, I_{\text{ANODE}} = 0.4mA, I_{\text{GRID}} = 24mA\)

\[P_D = (5.25V \times 0.7mA) + (42V \times 0.9mA) + ((2.5V \times 0.4mA/25mA) \times 0.4mA \times 6) + ((2.5V \times 24mA/25mA) \times 24mA) = 99mW\]

Thus, for a 20-pin wide SO package (\(T_{JA} = 1/0.01 = +100^\circ\text{C/W}\) from *Absolute Maximum Ratings*), the maximum allowed ambient temperature \(T_A\) is given by:

\[T_{J(MAX)} = T_A + (PD \times T_{JA}) = +150^\circ\text{C} = T_A + (0.099 \times +100^\circ\text{C/W})\]

So \(T_A = +140^\circ\text{C}\).
This means that the driver can be operated in this application up to the MAX6920’s +125°C maximum operating temperature.

Power-Supply Considerations
The MAX6920 operates with multiple power-supply voltages. Bypass the V_{CC} and V_{BB} power-supply pins to GND with a 0.1µF capacitor close to the device. For multiplex applications, it may be necessary to add an additional 1µF bulk electrolytic capacitor, or greater, to the V_{BB} supply.

Power-Supply Sequencing
The order of the power-supply sequencing is not important. The MAX6920 will not be damaged if either V_{CC} or V_{BB} is grounded (or maintained at any other voltage below the data sheet minimum), while the other supply is maintained up to its maximum rating. However, as with any CMOS device, do not drive the MAX6920’s logic inputs if the logic supply V_{CC} is not operational because the input protection diodes clamp the signals.

Chip Information
PROCESS: BiCMOS

Typical Application Circuit

Package Information
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

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<th>PACKAGE TYPE</th>
<th>PACKAGE CODE</th>
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## Revision History

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<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
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<tr>
<td>0</td>
<td>10/03</td>
<td>Initial Release</td>
<td>—</td>
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<tr>
<td>1</td>
<td>8/14</td>
<td>Removed automotive reference from data sheet</td>
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