**General Description**

The MAX6880–MAX6883 dual-/triple-voltage monitors are designed to sequence power supplies during power-up condition. When all of the voltages exceed their respective thresholds, these devices turn on voltages to the system sequentially, enhancing n-channel MOSFETs used as switches. The time between each sequenced voltage is determined by an external capacitor, thus allowing flexibility in delay timing. The MAX6880/MAX6881 sequence three voltages and the MAX6882/MAX6883 sequence two voltages.

These devices initially monitor all of the voltages and when all of them are within their tolerances, the internal charge pumps enhance external n-channel MOSFETs in a sequential manner to apply voltages to the system. Internal charge pumps drive the gate voltages 5V above the respective input voltage thereby ensuring the MOSFETs are fully enhanced to reduce the on-resistance.

The MAX6880–MAX6883 feature capacitor-adjustable slew-rate control to provide controlled turn-on characteristics. After all of the voltages reach 92.5% of their final value, a power-good output (MAX6880/MAX6882) signal is active. The power-good output (PG/RST) can be delayed with an external capacitor to create a power-on reset delay. After the initial power-up phase, the MAX6880–MAX6883 continue to monitor the voltages. If any of the voltages falls below its threshold, the MOSFETs are quickly turned off and the voltages are tracked down together. An internal 100Ω pulldown resistor ensures that the capacitance at the MOSFET's source is discharged quickly. The power-good output goes low to provide a system reset.

The MAX6880–MAX6883 are available in small 4mm x 4mm 24-pin and 16-pin thin QFN packages and specified over the -40°C to +85°C extended operating temperature range.

**Features**

- Capacitor-Adjustable Power-Up Sequencing Delay
- Internal Charge Pumps to Enhance External n-Channel FETs
- Capacitor-Adjustable Timeout Period Power-Good Output (MAX6880/MAX6882)
- Adjustable Undervoltage Lockout or Logic-Enable Input
- Internal 100Ω Pulldown for Each Output to Discharge Capacitive Load Quickly
- 0.5V to 5.5V Nominal IN_/OUT_ Range
- 2.7V to 5.5V Operating Voltage Range
- Immune to Short Voltage Transients
- Small 4mm x 4mm 24-Pin or 16-Pin Thin QFN Packages

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
<th>PKG CODE</th>
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<td>MAX6880</td>
<td>-40°C to +85°C</td>
<td>24 Thin QFN</td>
<td>T2444-4</td>
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<tr>
<td>MAX6881</td>
<td>-40°C to +85°C</td>
<td>16 Thin QFN</td>
<td>T1644-4</td>
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<td>MAX6882</td>
<td>-40°C to +85°C</td>
<td>16 Thin QFN</td>
<td>T1644-4</td>
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<tr>
<td>MAX6883</td>
<td>-40°C to +85°C</td>
<td>16 Thin QFN</td>
<td>T1644-4</td>
</tr>
</tbody>
</table>

+ Denotes lead-free package.

**Applications**

Multivoltage Systems  
Networking Systems  
Telecom  
Storage Equipment  
Servers/Workstations

*Selector Guide appears at end of data sheet.*
**Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors**

**ABSOLUTE MAXIMUM RATINGS**

(All voltages referenced to GND, unless otherwise noted.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>ICC</td>
<td>IN1 = 5.5V, IN2 = IN3 = 3.3V, no load</td>
<td>1.1</td>
<td>1.8</td>
<td>mA</td>
<td></td>
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<tr>
<td>SET_ Threshold Range</td>
<td>VTH</td>
<td>SET_ falling, TA = +25°C</td>
<td>0.4925</td>
<td>0.5075</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SET_ falling, TA = -40°C to +85°C</td>
<td>0.4875</td>
<td>0.5125</td>
<td>V</td>
<td></td>
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<tr>
<td>SET_ Threshold Hysteresis</td>
<td>VTH_HYST</td>
<td>SET_ rising</td>
<td>0.5</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SET_ Input Current</td>
<td>ISET</td>
<td>SET_ = 0.5V</td>
<td>-100</td>
<td>+100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>EN/UV Input Voltage</td>
<td>VEN_R</td>
<td>Input rising</td>
<td>1.286</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VEN_F</td>
<td>Input falling</td>
<td>1.22</td>
<td>1.28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN/UV Input Current</td>
<td>IEN</td>
<td>EN/UV falling, 100mV overdrive</td>
<td>-5</td>
<td>+5</td>
<td>µA</td>
<td></td>
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<tr>
<td>EN/UV Input Pulse Width</td>
<td>IEN</td>
<td>EN/UV falling, 100mV overdrive</td>
<td>7</td>
<td>µs</td>
<td></td>
<td></td>
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<tr>
<td>DELAY, TIMEOUT Output Current</td>
<td>ID</td>
<td>(Notes 2, 3)</td>
<td>2.12</td>
<td>2.5</td>
<td>2.88</td>
<td>µA</td>
</tr>
<tr>
<td>DELAY, TIMEOUT Threshold Voltage</td>
<td>VCC = 3.3V</td>
<td>1.25</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SLEW Output Current</td>
<td>IS</td>
<td>(Note 4)</td>
<td>22.5</td>
<td>25</td>
<td>27.5</td>
<td>µA</td>
</tr>
<tr>
<td>Sequence Slew-Rate Timebase Accuracy</td>
<td>SR</td>
<td>CSLEW = 200pF</td>
<td>-15</td>
<td>+15</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Timebase/CSLEW Ratio</td>
<td></td>
<td>100pF &lt; CSLEW &lt; 1nF</td>
<td>104</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew-Rate Accuracy during Power-Up and Power-Down</td>
<td></td>
<td>CSLEW = 200pF, VIN_ = 5.5V (Note 4)</td>
<td>-50</td>
<td>+50</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

(IN1, IN2, or IN3 = +2.7V to +5.5V, EN/UV = MARGIN = ABP, TA = -40°C to +85°C, unless otherwise specified. Typical values are at TA = +25°C, unless otherwise noted.) (Note 1)
ELECTRICAL CHARACTERISTICS (continued)

(IN1, IN2, or IN3 = +2.7V to +5.5V, EN/UV = MARGIN = ABP, TA = -40°C to +85°C, unless otherwise specified. Typical values are at TA = +25°C, unless otherwise noted.) (Note 1)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Notes</th>
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<tbody>
<tr>
<td>Power-Good Threshold</td>
<td>VTH_PG</td>
<td>91.5</td>
<td>93.5</td>
<td>%</td>
</tr>
<tr>
<td>Power-Good Threshold Hysteresis</td>
<td>VHY_PG</td>
<td>92.5</td>
<td>93.5</td>
<td>%</td>
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<td>GATE_ Output High</td>
<td>VGOH</td>
<td>4.2</td>
<td>5.8</td>
<td>V</td>
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<tr>
<td>GATE_ Pullup Current</td>
<td>IGUP</td>
<td>2.5</td>
<td>4</td>
<td>µA</td>
</tr>
<tr>
<td>GATE_ Pulldown Current</td>
<td>IG</td>
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<td>µA</td>
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<td>GATE_ Pulldown Current</td>
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<td>Ω</td>
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<tr>
<td>OUT to GND Pulldown Impedance</td>
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<td>Ω</td>
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<td>MARGIN Pullup Current</td>
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<td>MARGIN Input Voltage</td>
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<tr>
<td>MARGIN Glitch Rejection</td>
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<td>2.0</td>
<td>ns</td>
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</tbody>
</table>

Note 1: Specifications guaranteed for the stated global conditions. 100% production tested at TA = +25°C and TA = +85°C. Specifications at TA = -40°C to +85°C are guaranteed by design. These devices meet the parameters specified when at least one of IN1/IN2/IN3 is between 2.7V to 5.5V, while the remaining IN1/IN2/IN3 are between 0 and 5.5V.

Note 2: A current |I0| = 2.5µA ±15% is generated internally and is used to set the DELAY and TIMEOUT periods and used as a reference for tDELY and tTIMEOUT.

Note 3: The total DELAY is tDELAY = 200µs + (500kΩ x CDelay). Leave DELAY unconnected for 200µs delay. The total TIMEOUT is tTIMEOUT = 200µs + (500kΩ x CTIMEOUT). Leave TIMEOUT unconnected for 200µs timeout.

Note 4: A current |I0| = 25µA ±10% is generated internally and used as a reference for tFAULT, tRETRY, and slew rate.

Note 5: During power-up, only the condition OUT_ < ramp - VTRK is checked in order to stop the ramp. However, both conditions OUT_ < ramp - VTRK_F and OUT_ > ramp + VTRK_F cause a fault. During power-down, only the condition OUT > ramp + VTRK is checked in order to stop the ramp. However, both conditions OUT_ < ramp - VTRK_F and OUT_ > ramp + VTRK_F cause a fault (see Figure 10). Therefore, if OUT1, OUT2, and OUT3 (during power-up tracking and power-down) differ by more than 2 x VTRK_F, a fault condition is asserted.

Note 6: A 100Ω pulldown to GND activated by a fault condition. See the Internal Pulldown section.
**Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors**

Figure 1. Stop Ramp/Fault Window During Power-Up and Power-Down

Figure 2. Sequencing In Normal Mode
IN\_VEN\_R

IN1 = 3.3V
IN2 = 1.8V
IN3 = 0.7V

MONITORED THROUGH SET THRESHOLDS ON SET\_ INPUTS

OUT\_ OUT2 = 1.8V
OUT3 = 0.7V
OUT1 = 3.3V

MONITORED THROUGH SET THRESHOLDS ON SET\_ INPUTS

CAPACITOR-
ADJUSTED
SLEW RATE

OUT\_ FORCED
BELOW \textit{V}_{TH,PG}\n
BUS VOLTAGE MONITORED THROUGH EN/UV INPUT

FORCED INTO QUICK SHUTDOWN WHEN OUT1 FALLS BELOW 92.5\% of IN1

Figure 3. Sequencing In Fast Shutdown Mode
**Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors**

**Figure 4. Timing Diagram (Aborted Sequencing)**

**Figure 5. tFAULT and tRETRY Timing Diagram in Sequencing**
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

Typical Operating Characteristics

(V_{IN_} = 2.7V to 5.5V, C_{SLEW} = 200pF, EN = MARGIN = ABP, T_A = +25°C, unless otherwise noted.)
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

Typical Operating Characteristics (continued)

(VIN_ = 2.7V to 5.5V, C_{SLEW} = 200pF, EN = MARGIN = ABP, TA = +25°C, unless otherwise noted.)

[Graphs and tables of typical operating characteristics are shown here, including voltage vs. current plots and waveforms for sequencing and shutdown modes.]
## Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

### Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
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<tbody>
<tr>
<td>MAX6880</td>
<td>MAX6881</td>
<td>MAX6882</td>
</tr>
<tr>
<td>1, 11, 12, 15</td>
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<td>—</td>
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<td>—</td>
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## Pin Description (continued)

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<tr>
<td>24</td>
<td>1</td>
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</table>

**MAX6880–MAX6883**

**Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors**

Power-Good Output, Open-Drain. **PG/RST** asserts high **TIMEOUT** after all **OUT** voltages exceed the **VTH_PG** thresholds.

Channel 3 Monitored Output Voltage. Connect **OUT3** to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.

Gate Drive for External n-Channel FET. An internal charge pump boosts **GATE3** to **VIN3 + 5V** to fully enhance the external n-channel FET when power-up is complete.

Channel 2 Monitored Output Voltage. Connect **OUT2** to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.

Gate Drive for External n-Channel FET. An internal charge pump boosts **GATE2** to **VIN2 + 5V** to fully enhance the external n-channel FET when power-up is complete.

Channel 1 Monitored Output Voltage. Connect **OUT1** to the source of an n-channel FET. A fault condition activates a 100Ω pulldown to ground.

Gate Drive for External n-Channel FET. An internal charge pump boosts **GATE1** to **VIN1 + 5V** to fully enhance the external n-channel FET when power-up is complete.

Supply Input Voltage. IN1, IN2, or IN3 must be greater than the internal undervoltage lockout (**VABP = 2.7V**) to enable the sequencing functionality. Each **IN** input is simultaneously monitored by **SET** inputs to ensure all supplies have stabilized before power-up is enabled. If **IN** is connected to ground or left unconnected and **SET** is above 0.5V, then no sequencing control is performed on that channel. Each **IN** is internally pulled down by a 100kΩ resistor.
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

Detailed Description
The MAX6880–MAX6883 multivoltage power sequencers/supervisors monitor three (MAX6880/MAX6881) and two (MAX6882/MAX6883) system voltages and provide proper power-up and power-down control for systems requiring voltage sequencing. These devices ensure the controlled voltages sequence in the proper order as system power supplies are enabled. The MAX6880–MAX6883 generate all required voltages and timing to control up to three external n-channel pass FETs for the OUT1/OUT2/OUT3 supply voltages.

The MAX6880–MAX6883 feature adjustable undervoltage thresholds for each input supply. When all of the voltages are above the adjusted thresholds these devices turn on the external n-channel MOSFETs to sequence the voltages to the system. The outputs are turned on one after the other, OUT1 first and OUT3 last.

The MAX6880–MAX6883 feature internal charge pumps to fully enhance the external FETs for low-voltage drops at highpass currents. The MAX6880/MAX6882 also feature a power-good output (PG/RST) with a selectable timeout period that can be used for system reset.

The MAX6880–MAX6883 monitor up to three voltages. Devices may be configured to exclude any IN_. To disable sequencing operation of any IN_, connect the IN_ to ground (or leave unconnected) and connect SET_ to a voltage greater than 0.5V. The channel exclusion feature adds more flexibility to the device in a variety of different applications. As an example, the MAX6880 can sequence two voltages using IN1 and IN2 while IN3 is left disabled.

Powering the MAX6880–MAX6883
These devices derive power from either IN1, IN2, or IN3 voltage inputs (see the Functional Diagram). In order to ensure proper operation, at least one of the IN_ inputs must be at least +2.7V.

The highest input voltage on IN1/IN2/IN3 supplies power to the devices. Internal hysteresis ensures that the supply input that initially powers these devices continues to power the MAX6880–MAX6883 when multiple input voltages are within 100mV (typ) of each other.

Sequencing
The sequencing operation can be initiated after all input conditions for power-up are met: VATUV > 1.25V and all SET_ inputs are above the internal SET_ threshold (0.5V). In sequencing mode, the outputs are turned on sequentially, OUT1 first and OUT3 last. Before turning on each channel, a delay period is waited (programmable by connecting a capacitor from DELAY to ground. The power-up phase for each channel ends when its output voltage exceeds a fixed percentage (VTH_PG) of the corresponding IN_ voltage. When all channels have exceeded these thresholds, PG/RST asserts high after TTIMEOUT, indicating a successful sequence.

If there is a fault condition during the initial power-up sequence, the process is aborted.

When powering down, all outputs turn off simultaneously, tracking each other. No reverse power-down sequencing occurs.

The power-supply sequencing operation should be completed within the selected fault timeout period (TFAULT) (see Figure 5). The total sequencing time is extended when the devices must vary the control slew rate to allow slow supplies to catch up. If the external FET is too small (RDS is too high for the selected load current and IN_ source current), the OUT_ voltage may never reach the control ramp voltage. For a slew rate of 935V/s, a fault is signaled if all outputs have not stabilized within 22ms. For a slew rate of 93.5V/s, a fault is signaled if sequencing takes too long (more than 219ms).

The fault time period (TFAULT) is set through the capacitor at SLEW (CSLEW). Use the following formula to estimate the fault timeout period:

\[ T_{FAULT} = 2.191 \times 10^8 \times CSLEW \]

Autoretry Function
The MAX6880/MAX6881/MAX6882 feature autoretry modes to power-on again after a fault condition has been detected (see the Typical Operating Characteristics).

When a fault is detected, for a period of TRETRY, GATE_ remains off and the 100Ω pulldowns are turned on. After the TRETRY period, the device waits TDELAY and retry sequencing if all power-up conditions are met (see Figure 5). These include all VSET_ > 0.5V, EN/UV > VEN_R, and OUT_ voltages < VTH_PL. The autoretry period TRETRY is a function of CSLEW (see Table 1).

Power-Up and Power-Down
During power-up, OUT_ is forced to follow the internal reference ramp voltage by an internal loop that controls the GATE_ of the external MOSFET. This phase must be completed within the adjustable fault timeout period (TFAULT); otherwise, the part forces a shutdown on all GATE_.

Once the power-up is completed, a power-down phase can be initiated by forcing VEN/UV below VEN_F. The reference voltage ramp ramps down at the capacitor-adjusted slew rate. The control-loop comparators monitor each OUT_ voltage with respect to the common
reference ramp voltage. During ramp down, if an OUT voltage is greater than the reference ramp voltage by more than $V_{TRK}$, the control loop dynamically stops the control ramp voltage from decreasing until the slow OUT voltage catches up. If an OUT voltage is greater or less than the reference ramp voltage by more than $V_{TRK,F}$, a fault is signaled and the fast-shutdown mode is initiated. In fast-shutdown mode, a $100\,\Omega$ pulldown resistor is connected from OUT to GND to quickly discharge capacitance at OUT, and GATE is pulled low with a strong Igds current (see Figure 3).

Figure 4 shows the aborted sequencing mode. When EN/UV goes low before $t_{TIMEOUT}$ expires, all the outputs go low, and the device goes into fast shutdown.

**Internal Pulldown**

To ensure that the OUT voltages are not held high by a large output capacitance after a fault has occurred, there is a $100\,\Omega$ internal pulldown at OUT. The pulldown ensures that all OUT voltages are below $V_{TH, PL}$ (referenced to GND) before power-up cycling is initiated. The internal pulldown also ensures a fast discharge of the output capacitor during fast shutdown and fault modes. The pulldowns are not present during normal operation.

**Stability Comment**

No external compensation is required for sequencing or slew-rate control.

**Inputs**

IN1/IN2/IN3

The highest voltage on IN1, IN2, or IN3 supplies power to the device. The undervoltage threshold for each IN supply is set with an external resistor-divider from each IN to SET to ground. To disable sequencing on any IN, connect IN to ground (or leave unconnected) and connect SET to a voltage greater than 0.5V.

**Undervoltage Lockout Threshold Inputs (SET_)**

The MAX6880/MAX6881 feature three and the MAX6882/MAX6883 feature two externally adjustable IN under-voltage lockout thresholds (SET1/SET2/SET3). The 0.5V SET threshold enables monitoring IN voltages as low as 0.5V. The undervoltage threshold for each IN supply is set with an external resistor-divider from each IN to SET to ground (see Figure 6). All SET inputs must be above the internal SET threshold (0.5V) to enable sequencing functionality. Use the following formula to set the UVLO threshold:

$$V_{IN} = V_{TH} \left( \frac{R1 + R2}{R2} \right)$$

where $V_{IN}$ is the undervoltage lockout threshold and $V_{TH}$ is the 500mV SET threshold.

**Margin Input (MARGIN) (MAX6880/MAX6882)**

MARGIN allows system-level testing while power supplies are below the normal ranges as adjusted by the SET inputs. Drive MARGIN low before varying system voltages below the adjusted thresholds to avoid signaling an error. The state of PG/RST does not change while MARGIN is low. PG/RST and all monitoring functions are disabled while MARGIN is low. MARGIN makes it possible to vary the supplies without a need to adjust the thresholds to prevent sequencer alerts. Drive MARGIN high or leave it unconnected for normal operating mode.

**Slew-Rate Control Input (SLEW)**

The reference ramp voltage slew rate during any controlled power-up/down phase can be programmed in the 90V/s to 950V/s range by connecting a capacitor ($C_{SLEW}$) from SLEW to ground. Use the following formula to calculate the typical slew rate:

$$Slew \, Rate = \frac{9.35 \times 10^{-8}}{C_{SLEW}}$$

where slew rate is in V/s and $C_{SLEW}$ is in farads.

The capacitor at $C_{SLEW}$ also sets the retry timeout period ($t_{RETRY}$), see Table 1.

For example, if $C_{SLEW} = 100\,pF$, we have $t_{RETRY} = 350ms$, $t_{FAULT} = 21.91ms$, slew rate = 935V/s. For example, if $C_{SLEW} = 1\,nF$, we have $t_{RETRY} = 3.5s$, slew rate = 93.5V/s.

$C_{SLEW}$ is the capacitor on SLEW pad, and must be large enough so the parasitic PC board capacitance is negligible. $C_{SLEW}$ should be in the range of $100\,pF < C_{SLEW} < 1\,nF$.

Figure 6. Setting the Undervoltage (UVLO) Thresholds
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

**Table 1. C_{SLEW} Timing Formulas**

<table>
<thead>
<tr>
<th>TIME PERIOD</th>
<th>FORMULAS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow Rate</td>
<td>$(9.35 \times 10^{-8})/C_{SLEW}$</td>
</tr>
<tr>
<td>t_{RETRY}</td>
<td>$3.506 \times 10^3 \times C_{SLEW}$</td>
</tr>
<tr>
<td>t_{FAULT}</td>
<td>$2.191 \times 10^3 \times C_{SLEW}$</td>
</tr>
</tbody>
</table>

**Limiting Inrush Current**

The capacitor (C_{SLEW}) at SLEW to ground, controls the OUT_ slew rate, thus controlling the inrush current required to charge the load capacitor at OUT_. Using the programmed slew rate, limit the inrush current by using the following formula:

$$I_{INRUSH} = C_{OUT} \times SR$$

where $I_{INRUSH}$ is in amperes, $C_{OUT}$ is in farads, and $SR$ is in V/s.

**Delay Time Input (DELAY)**

To adjust the desired delay period (t_{DELAY}) before sequencing is enabled, connect a capacitor (C_{DELAY}) between DELAY to ground (see Figures 2 to 5). The selected delay time is also enforced when EN/UV rises from low to high when all the input voltages are present. Use the following formula to calculate the delay time:

$$t_{DELAY} = 200\mu s + (500k\Omega \times C_{DELAY})$$

where $t_{DELAY}$ is in $\mu$s and $C_{DELAY}$ is in farads. Leave DELAY unconnected for the default 200$\mu$s delay.

**Timeout Period Input (TIMEOUT)**

These devices feature a PG/RST timeout period. Connect a capacitor (C_{TIMEOUT}) from TIMEOUT to ground to program the PG/RST timeout period. After all OUT_ outputs exceed their IN_ referenced thresholds ($V_{TH,PG}$), PG/RST remains low for the selected timeout period t_{TIMEOUT} (see Figure 3).

$$t_{TIMEOUT} = 200\mu s + (500k\Omega \times C_{TIMEOUT})$$

where $t_{TIMEOUT}$ is in $\mu$s and $C_{TIMEOUT}$ is in farads. Leave TIMEOUT unconnected for the default 200$\mu$s timeout delay.

**Logic-Enable Input (EN/UV)**

Drive logic EN/UV input above $V_{EN,R}$ to initiate voltage sequencing during power-up operation. Drive logic EN/UV below $V_{EN,F}$ to initiate tracking power-down operation. Connect EN/UV to an external resistor-divider network to set the external undervoltage lockout threshold.

**ABP Input (MAX6880/MAX6882)**

ABP powers the analog circuitry. Bypass ABP to GND with a 1$\mu$F ceramic capacitor installed as close to the device as possible. ABP takes the highest voltage of IN_. Do not use ABP to provide power to external circuitry. ABP maintains the device supply voltage during rapid power-down conditions.

**OUT1/OUT2/OUT3**

The MAX6880/MAX6881 monitor three OUT_ and the MAX6882/MAX6883 monitor two OUT_ outputs to control the sequencing performance. After the internal supply (ABP) exceeds the minimum voltage (2.7V) requirements, EN/UV > $V_{EN,R}$, and IN1/IN2/IN3 are all greater than their adjusted SET_ thresholds, OUT1/OUT2/OUT3 begin to sequence. During fault conditions, an internal pulldown resistor (100$\Omega$) on OUT_ is enabled to help discharge load capacitance (100$\Omega$ is connected for fast power-down control).

**Outputs**

**GATE_**

The MAX6880–MAX6883 feature up to three GATE_ outputs to drive up to three external n-channel FET gates. The following conditions must be met before GATE_ begins enhancing the external n-channel FET:

1) All SET_ inputs (SET1/SET2/SET3) are above their 0.5V thresholds.
2) At least one IN_ input is above the minimum operating voltage (2.7V).
3) EN/UV > 1.25V.

At power-up mode, GATE_ voltages are enhanced by control loops so all OUT_ voltages sequence at a capacitor-adjusted slew rate. Each GATE_ is internally pulled up to 5V above its relative IN_ voltage to fully enhance the external n-channel FET when power-up is complete.

**Power-Good Output (PG/RST) (MAX6880/MAX6882)**

The MAX6880/MAX6882 include a power-good (PG/RST) output. PG/RST is an open-drain output and requires an external pullup resistor. All the OUT_ outputs must exceed their IN_ referenced thresholds ($IN_ \times V_{TH,PG}$) for the selected reset timeout period t_{TIMEOUT} (see the TIMEOUT Period Input section) before PG/RST asserts high. PG/RST stays low for the selected reset timeout period (t_{TIMEOUT}) after all the OUT_ voltages exceed their IN_ referenced thresholds. PG/RST goes low when $V_{SET_} < V_{TH}$ or $V_{EN/UV} < V_{EN,R}$ (see Figure 2).
Applications Information

MOSFET Selection
The external pass MOSFET is connected in series with the sequenced power-supply source. Since the load current and the MOSFET drain-to-source impedance (R\text{ds}) determine the voltage drop, the on characteristics of the MOSFET affect the load supply accuracy. The MAX6880–MAX6883 fully enhance the external MOSFET out of its linear range to ensure the lowest drain-to-source on-impedance. For highest supply accuracy/lowest voltage drop, select a MOSFET with an appropriate drain-to-source on-impedance with a gate-to-source bias of 4.5V to 6.0V.

Layout and Bypassing
For better noise immunity, bypass each of the IN inputs to GND with 0.1\mu F capacitors installed as close to the device as possible. Bypass ABP to GND with a 1\mu F capacitor installed as close to the device as possible. ABP is an internally generated voltage and must not be used to supply power to external circuitry.

Selector Guide

<table>
<thead>
<tr>
<th>PART</th>
<th>CHANNEL</th>
<th>TIMEOUT SELECTABLE</th>
<th>PG/RST</th>
<th>MARGIN</th>
<th>PG THRESHOLD VOLTAGE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX6880</td>
<td>3</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>92.5</td>
</tr>
<tr>
<td>MAX6881</td>
<td>3</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>—</td>
</tr>
<tr>
<td>MAX6882</td>
<td>2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>92.5</td>
</tr>
<tr>
<td>MAX6883</td>
<td>2</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>—</td>
</tr>
</tbody>
</table>

Chip Information

PROCESS: BiCMOS
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

Typical Application Circuit
Pin Configurations (continued)

TOP VIEW

4mm x 4mm THIN QFN

MAX6881

SET1

GATE1

GATE2

IN1

IN2

IN3

OUT1

OUT2

OUT3

SLEW

DELAY

GND

EN/UV

MAX6882

SET1

PG/RST

GATE1

GATE2

IN1

IN2

IN3

OUT1

OUT2

OUT3

SLEW

DELAY

GND

EN/UV

MAX6883

SET1

N.C.

GATE1

GATE2

IN1

IN2

IN3

OUT1

OUT2

OUT3

SLEW

DELAY

GND

EN/UV

*EXPOSED PADDLE CONNECTED TO GND.
Dual-/Triple-Voltage, Power-Supply Sequencers/Supervisors

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)