**General Description**

The MAX5712 is a small footprint, low-power, 12-bit digital-to-analog converter (DAC) that operates from a single +2.7V to +5.5V supply. The MAX5712 on-chip precision output amplifier provides rail-to-rail output swing. Drawing only 85μA supply current at +3V, the MAX5712 is ideally suited for portable battery-operated equipment.

The MAX5712 utilizes a 3-wire serial-interface that is compatible with SPI/QSPI™/MICROWIRE® and DSP-interface standards. All logic inputs are CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers. The MAX5712 incorporates a power-on reset (POR) circuit that ensures the DAC begins in a zero-volt-state upon power-up. A power-down mode that reduces current consumption to 0.3μA may be initiated through a software command.

The MAX5712 is available in a small 6-pin SOT23 package. For dual and quad 12-bit versions, see the MAX5722 and MAX5742 data sheets. For single, dual, and quad 10-bit versions, see the MAX5711, MAX5721 and MAX5741 data sheets. The MAX5712 is specified over the automotive temperature range of -40°C to +125°C.

**Applications**

- Automatic Tuning
- Gain and Offset Adjustment
- Power Amplifier Control
- Process Control I/O Boards
- Battery-Powered Equipment
- VCO Control

**Features**

- Wide -40°C to +125°C Operating Temperature Range
- Low 85μA Supply Current
- Ultra Low 0.3μA Power-Down Supply Current
- Single +2.7V to +5.5V Supply Voltage
- Fast 20MHz 3-Wire SPI/QSPI/MICROWIRE and DSP-Compatible Serial Interface
- Schmitt-Triggered Inputs for Direct Interfacing to Optocouplers
- Rail-to-Rail Output Buffer
- Tiny 6-Pin SOT23 Package
- Power-On Reset to 0V
- Three Software-Selectable Power-Down Output Impedances (100kΩ, 1kΩ, Hi-Z)

**Ordering Information**

<table>
<thead>
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<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
<th>TOP MARK</th>
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<td>-40°C to +85°C</td>
<td>6 SOT23</td>
<td>ABCQ/ACST</td>
</tr>
<tr>
<td>MAX5712AUT+T</td>
<td>-40°C to +125°C</td>
<td>6 SOT23</td>
<td>AAUD/ACST</td>
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</tbody>
</table>

+Denotes a lead(Pb)-free/RoHS-compliant package.

*Pin Configuration appears at end of data sheet.*

**Functional Diagram**

[Diagram of MAX5712 DAC with functional blocks labeled: DAC REGISTER, REF+, REF-, 12-BIT DAC, OUTPUT BUFFER, POWER-DOWN CONTROL LOGIC, POWER-ON RESET, VCC, GND, CS, SCLK, DIN, OUT, 100kΩ, 1kΩ]
MAX5712 Low-Power, 12-Bit, Rail to Rail Voltage-Output Serial DAC in SOT23

Absolute Maximum Ratings

V_{DD} to GND ............................................................ -0.3V to +6V
OUT, SCLK, DIN, CS to GND ................... -0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin.............. ±50mA
Continuous Power Dissipation (T_{A} = +70°C)........ 727mW
Operating Temperature Range .................... -40°C to +125°C
Maximum Junction Temperature .................. +150°C
Storage Temperature Range ............... -65°C to +150°C
Lead Temperature (soldering, 10s) ............ +300°C
Soldering Temperature (reflow) ................. +260°C
Continuous Power Dissipation (TA = +70°C) ....... 727mW

Package Thermal Characteristics (Note 1)

SOT23
Junction-to-Ambient Thermal Resistance (\theta_{JA}) ... 134.40°C/W
Junction-to-Case Thermal Resistance (\theta_{JC}) .......... 39°C/W

Electrical Characteristics

(V_{DD} = +2.7V to +5.5V, GND = 0, R_{L} = 5k\Omega, C_{L} = 200pF, T_{A} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V, T_{A} = +25°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>N</td>
<td>Guaranteed monotonic (Note 2)</td>
<td>12</td>
<td>±1</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Differential Nonlinearity Error</td>
<td>DNL</td>
<td>Code = 000</td>
<td>±2</td>
<td>±16</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity Error</td>
<td>INL</td>
<td>Code = FFF hex</td>
<td>0.4</td>
<td>1.5</td>
<td>% of FS</td>
<td></td>
</tr>
<tr>
<td>Zero-Code Error</td>
<td>OE</td>
<td>Code = 000</td>
<td>0.4</td>
<td>1.5</td>
<td>% of FS</td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td>GE</td>
<td>Code = FFF hex</td>
<td>2.3</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain-Error Tempco</td>
<td>GE</td>
<td>Code = FFF hex</td>
<td>-3</td>
<td>% of FS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DAC OUTPUT

Output Voltage Range
No-load (Note 3) | 0 | V_{DD} | V

DC Output Impedance
Code = 800 hex | 0.8 | \Omega

Short Circuit Current
V_{DD} = +3V | 15 | mA
V_{DD} = +5V | 48 |

Wake-Up Time
V_{DD} = +3V | 8 | \mu s
V_{DD} = +5V | 8 |

Output Leakage Current
Power-down mode = output high-impedance | ±18 | ±33 | nA

DIGITAL INPUTS (SCLK, DIN, CS)

Input High Voltage | V_{IH} | V_{DD} = +3V, +5V | 0.7 \times V_{DD} | V
Input Low Voltage | V_{IL} | V_{DD} = +3V, +5V | 0.3 \times V_{DD} | V
Input Leakage Current | I_{IN} | Digital Inputs = 0 or V_{DD} | ±0.1 | ±1 | \mu A
Input Capacitance | C_{IN} | 5 | pF

DYNAMIC PERFORMANCE

Voltage-Output Slew Rate | SR | 0.5 | V/\mu s
Voltage-Output Settling Time
400 hex to C00 hex (Note 4) | 4 | 10 | \mu s
Digital Feedthrough
Any digital inputs from 0 to V_{DD} | 0.2 | nV-s
Digital-Analog Glitch Impulse
Major carry transition (code 7FF hex to code 800 hex) | 12 | nV-s

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
**MAX5712** Low-Power, 12-Bit, Rail to Rail Voltage-Output Serial DAC in SOT23

### Electrical Characteristics (continued)

\(V_{DD} = +2.7\text{V to} +5.5\text{V, GND} = 0, R_L = 5\text{k}\Omega, C_L = 200\text{pF, } T_A = T_{MIN} \text{ to } T_{MAX}, \text{unless otherwise noted. Typical values are at } V_{DD} = +5\text{V, } T_A = +25^\circ\text{C}}

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>POWER REQUIREMENTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage Range</td>
<td>(V_{DD})</td>
<td>All digital inputs at 0 or (V_{DD}), (V_{DD} = +3.6\text{V})</td>
<td>2.7</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Supply Current with No-Load</td>
<td>(I_{DD})</td>
<td>All digital inputs at 0 or (V_{DD}), (V_{DD} = +5.5\text{V})</td>
<td>85</td>
<td>150</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>Power-Down Supply Current</td>
<td>(I_{DDPD})</td>
<td>All digital inputs at 0 or (V_{DD}), (V_{DD} = +5.5\text{V})</td>
<td>105</td>
<td>187</td>
<td></td>
<td>(\mu\text{A})</td>
</tr>
</tbody>
</table>

### TIMING CHARACTERISTICS (FIGURE 1) (TIMING IS TESTED WITH NO-LOAD)

| SCLK Clock Frequency            | \(f_{SCLK}\) | 0    | 20   |      | MHz   |
| SCLK Pulse Width High           | \(t_{CH}\) | 20   |      |      | ns    |
| SCLK Pulse Width Low            | \(t_{CL}\) | 20   |      |      | ns    |
| \(CS\) Fall-to-SCLK Rise       | \(t_{CSS}\) | 15   |      |      | ns    |
| DIN Setup Time                  | \(t_{DS}\) | 15   |      |      | ns    |
| DIN Hold Time                   | \(t_{DH}\) | 0    |      |      | ns    |
| SCLK Falling Edge-to-CS Rising Edge | \(t_{CSH}\) | 10   |      |      | ns    |
| \(CS\) Pulse Width High        | \(t_{CSW}\) | 80   |      |      | ns    |

**Note 1:** DC Specifications are tested without output loads.
**Note 2:** Linearity guaranteed from code 115 to code 3981.
**Note 3:** Offset and gain error limit the FSR.
**Note 4:** Guaranteed by design.

### Typical Operating Characteristics

\(T_A = +25^\circ\text{C}, \text{unless otherwise noted.})
Typical Operating Characteristics (continued)
($T_A = +25^\circ C$, unless otherwise noted.)
Typical Operating Characteristics (continued)
($T_A = +25^\circ C$, unless otherwise noted.)

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**

**POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE**

**SUPPLY CURRENT vs. CS INPUT VOLTAGE**

**FULL-SCALE SETTLING TIME**
(VDD = +5V)

**FULL-SCALE SETTLING TIME**
(VDD = +5V)

**HALF-SCALE SETTLING TIME**
(VDD = +3V)

**HALF-SCALE SETTLING TIME**
(VDD = +3V)

**EXITING POWER-DOWN**
(VDD = +5V)

**DIGITAL-TO-ANALOG GLITCH IMPULSE**
(VDD = +5V)
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

**Pin Description**

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_DD</td>
<td>Power-Supply Input</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>DIN</td>
<td>Serial-Data Input</td>
</tr>
<tr>
<td>4</td>
<td>SCLK</td>
<td>Serial-Clock Input</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Active Low Chip-Select Input</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>DAC Output Voltage</td>
</tr>
</tbody>
</table>
Detailed Description
The MAX5712 voltage output, 12-bit DAC, offers a full 12-bit performance in a small 6-pin SOT23 package. The SOT23 footprint is less than 9mm². The MAX5712 has less than 1LSB differential nonlinearity error, ensuring monotonic performance. The device uses a simple 3-wire, SPI/QSPI/MICROWIRE and DSP-compatible serial interface that operates up to 20MHz. The MAX5712 incorporates three shutdown modes, making it ideal for low-power.

Analog Section
The MAX5712 consists of a resistor string, an output buffer, and a POR circuit. Monotonic digital to analog conversion is achieved using a resistor string architecture. Since VDD is the reference for the MAX5712, the accuracy of the DAC depends on the accuracy of VDD. The low bias current of the MAX5712 allows its power to be supplied by a voltage reference such as the MAX6030. The 12-bit DAC code is binary-unipolar with 1LSB = VDD/4096.

Output Buffer
The DAC output buffer has a rail-to-rail output and is capable of driving a 5kΩ resistive load in parallel with a 200pF capacitive load. With a capacitive load of 200pF, the output buffer slewes 0.5V/μs. With a 1/4FS to 3/4FS output transition, the amplifier output settles to 1/2LSB in less than 10μs when loaded with 5kΩ in parallel with 200pF. The buffer amplifier is stable with any combination of resistive loads greater than 5kΩ and capacitive loads less than 200pF.

Program the input register bits to power-down the device. The DAC registers are preserved during power-down and upon wake-up, the DAC output is restored to its pre-power-down voltage.

Power-On Reset
The MAX5712 has a POR circuit to set the DACs output to zero when VDD is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system start-up, such as after a loss of power. Upon initial power-up, an internal power-on-reset circuit ensures that all DAC registers are cleared, the DAC is powered-down, and its output is terminated to GND by a 100kΩ resistor. An 8μs recovery time after issuing a wake-up command is needed before writing to the DAC registers.

Digital Section
3-Wire Serial Interface
The MAX5712 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input (CS) frames the serial data loading at DIN. Immediately following CS high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its contents to the DAC latch. CS may then either be held low or brought high. CS must be brought high for a minimum of 80ns before the next write sequence, since a write sequence is initiated on a falling edge of CS. Not keeping CS low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions. Figure 1 shows the complete 3-wire serial interface transmission. Table 1 lists serial-interface mapping.

![Figure 1. Timing Diagram](image-url)
**Shutdown Modes**

The MAX5712 includes three software-controlled shutdown modes that reduce the supply current to below 1μA. In two of the three shutdown modes, OUT is connected to GND through a resistor. Table 1 lists the three shutdown modes of operation.

**Applications Information**

**Device Powered by an External Reference**

The MAX5712 generates an output voltage proportional to $V_{DD}$, coupling power supply noise to the output. The circuit in Figure 2 rejects this power-supply noise by powering the device directly with a precision voltage reference, improving overall system accuracy. The MAX6030 (+3V, 75ppm) or the MAX6050 (+5V, 75ppm) precision voltage references are ideal choices due to the low-power requirements of the MAX5712. This solution is also useful when the required full-scale output voltage is less than the available supply voltages.

**Table 1. Serial Interface Mapping**

<table>
<thead>
<tr>
<th>16-BIT SERIAL WORD</th>
<th>MODE</th>
<th>OUTPUT</th>
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</thead>
<tbody>
<tr>
<td>C3 C2 C1 C0 D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>12-Bit DAC Code</td>
<td>Set and update DAC</td>
</tr>
<tr>
<td>1 1 1 1 X X X X X X X X X X 0 0</td>
<td>Wake-Up</td>
<td>Current DAC setting (initially 0)</td>
</tr>
<tr>
<td>1 1 1 1 X X X X X X X X X X 0 1</td>
<td>Power-Down</td>
<td>Floating</td>
</tr>
<tr>
<td>1 1 1 1 X X X X X X X X X X 1 0</td>
<td>Power-Down</td>
<td>1kΩ to GND</td>
</tr>
<tr>
<td>1 1 1 1 X X X X X X X X X X 1 1</td>
<td>Power-Down</td>
<td>100kΩ to GND</td>
</tr>
</tbody>
</table>

**Digital Inputs and Interface Logic**

The 3-wire digital interface for the MAX5712 is compatible with SPI, QSPI, MICROWIRE, and DSP. The three digital inputs (CS, DIN, and SCLK) load the digital input serially into the DAC. All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This allows optocouplers to interface directly to the MAX5712 without additional external logic. The digital inputs are compatible with CMOS-logic levels.

**Power-Supply Bypassing and Layout**

Careful PC board layout is important for optimal system performance. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Use a ground plane to ensure that the ground return from GND to the supply ground is short and low impedance. Bypass $V_{DD}$ with a 0.1μF capacitor to ground as close as possible to the device.

**Pin Configuration**

![Figure 2. MAX5712 Powered By Reference](image)

**Chip Information**

PROCESS: BICMOS
MAX5712
Low-Power, 12-Bit, Rail to Rail Voltage-Output Serial DAC in SOT23

Package Information
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", 
"#", or "." in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing 
pertains to the package regardless of RoHS status.

<table>
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www.maximintegrated.com
Revision History

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<th>REVISION DATE</th>
<th>DESCRIPTION</th>
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<td>0</td>
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