General Description

The MAX5104 low-power, serial, voltage-output, dual 12-bit digital-to-analog converter (DAC) consumes only 500µA from a single +5V supply. This device features Rail-to-Rail® output swing and is available in a space-saving 16-pin QSOP package. To maximize the dynamic range, the DAC output amplifiers are configured with an internal gain of +2V/V.

The 3-wire serial interface is SPI™/QSPI™/MICROWIRE™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include programmable power-down (2µA), hardware power-down lockout (PDL), a separate reference voltage input for each DAC that accepts AC and DC signals, and an active-low clear input (CL) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality, and a serial-data output pin for Daisy chaining.

Applications

Industrial Process Control
Remote Industrial Controls
Digital Offset and Gain Adjustment
Microprocessor-Controlled Systems
Motion Control
Automatic Test Equipment (ATE)

Features

- 12-Bit Dual DAC with Internal Gain of +2V/V
- Rail-to-Rail Output Swing
- 12µs Settling Time
- +5V Single-Supply Operation
- Low Quiescent Current
  - 500µA (normal operation)
  - 2µA (power-down mode)
- SPI/QSPI/MICROWIRE Compatible
- Space-Saving 16-Pin QSOP Package
- Power-On Reset Clears Registers and DACs to Zero
- Adjustable Output Offset

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP. RANGE</th>
<th>PIN-PACKAGE</th>
<th>INL (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX5104CEE</td>
<td>0°C to +70°C</td>
<td>16 QSOP</td>
<td>±4</td>
</tr>
<tr>
<td>MAX5104EEE</td>
<td>-40°C to +85°C</td>
<td>16 QSOP</td>
<td>±4</td>
</tr>
</tbody>
</table>

Pin Configuration appears at end of data sheet.

Functional Diagram
Low-Power, Dual, Voltage-Output, 12-Bit DAC
with Serial Interface

MAX5104

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Condition</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to AGND</td>
<td>-0.3V to +6V</td>
<td>16-Pin QSOP (derate 8.30mW/°C above +70°C)……..667mW</td>
<td></td>
</tr>
<tr>
<td>VDD to DGND</td>
<td>-0.3V to +6V</td>
<td>Operating Temperature Ranges</td>
<td></td>
</tr>
<tr>
<td>AGND to DGND</td>
<td>-0.3V to +6V</td>
<td>MAX5104CEE……………………………………..0°C to +70°C</td>
<td></td>
</tr>
<tr>
<td>OSA, OSB to AGND</td>
<td>(VAGND - 4V) to (VDD + 0.3V)</td>
<td>MAX5104EEE………………………………..-40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>REF_, OUT_ to AGND</td>
<td>-0.3V to (VDD + 0.3V)</td>
<td>Junction Temperature …………………………..+150°C</td>
<td></td>
</tr>
<tr>
<td>Digital Inputs (SCLK, DIN, CS, CL, PDL) to DGND</td>
<td>(-0.3V to +6V)</td>
<td>Storage Temperature Range ………………-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Digital Outputs (DOUT, UPO) to DGND</td>
<td>-0.3V to (VDD + 0.3V)</td>
<td>Lead Temperature (soldering, 10sec) …………..+300°C</td>
<td></td>
</tr>
<tr>
<td>Maximum Current into Any Pin</td>
<td>±20mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VDD = +5V ±10%, VREF_ = VREF_ = +2.048V, RL = 10kΩ, CL = 100pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C (OS_ connected to AGND for a gain of +2V/V).)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>INL</td>
<td>(Note 1)</td>
<td>12</td>
<td>Bits</td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td></td>
<td></td>
<td>±4</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>DNL</td>
<td>Guaranteed monotonic</td>
<td>±1</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td>VOS</td>
<td>Code = 10</td>
<td>±10</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Offset Tempco</td>
<td>TCVOS</td>
<td>Normalized to 2.048V</td>
<td>4</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Gain Error</td>
<td></td>
<td></td>
<td>-0.2</td>
<td>±8</td>
<td>LSB</td>
</tr>
<tr>
<td>Gain - Error Tempco</td>
<td></td>
<td></td>
<td>4</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>VDD Power-Supply Rejection Ratio</td>
<td>PSRR</td>
<td>4.5V ≤ VDD ≤ 5.9V</td>
<td>20</td>
<td>600</td>
<td>µV/V</td>
</tr>
</tbody>
</table>

REFERENCE INPUT

| Reference Input Range | REF | 0 | VDD - 1.4 | V |
| Reference Input Resistance | RREF | Minimum with code 1554 hex | 14 | 20 | kΩ |

MULTIPLYING-MODE PERFORMANCE

| Reference 3dB Bandwidth | Input code = 1FFE hex, VREF_ = 0.67Vp-p at 2.5VDC | 300 | kHz |
| Reference Feedthrough | Input code = 0000 hex, VREF_ = | -82 | dB |
| Signal-to-Noise plus Distortion Ratio | SINAD | Input code = 1FFE hex, VREF_ = 1Vp-p at 1.25VDC, f = 25kHz | 75 | dB |

DIGITAL INPUTS

| Input High Voltage | VH | CL, PDL, CS, DIN, SCLK | 3 | V |
| Input Low Voltage | VL | CL, PDL, CS, DIN, SCLK | 0.8 | V |
| Input Hysteresis | VHYHS | | 200 | mV |
| Input Leakage Current | ILIN | VIN = 0 to VDD | 0.001 | ±1 | µA |
| Input Capacitance | CIN | | 8 | pF |
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

(VDD = +5V ±10%, VREFA = VREFB = +2.048V, RL = 10kΩ, CL = 100pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C (OS_ connected to AGND for a gain of +2V/V).)

### DIGITAL OUTPUTS (DOUT, UPO)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage</td>
<td>VOH</td>
<td>ISOURCE = 2mA</td>
<td>VDD - 0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>VIL</td>
<td>ISINK = 2mA</td>
<td>0.13</td>
<td>0.40</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

### DYNAMIC PERFORMANCE

- Voltage Output Slew Rate: SR
  - Typical: 0.75 V/µs
- Output Settling Time: To 1/2LSB of full-scale, VSTEP = 4V
  - Typical: 15 µs
- Output Voltage Swing: Rail-to-rail (Note 2)
  - Minimum: 0 to VDD
- OSA or OSB Input Resistance: ROS_
  - Typical: 24 34 kΩ
- Time Required to Exit Shutdown: 25 µs
- Digital Feedthrough: CS = VDD, SCLK = 100kHz, VCLK = 5Vp-p
  - Typical: 5 nVs
- Digital Crosstalk
  - Typical: 5 nVs

### POWER SUPPLIES

- Positive Supply Voltage: VDD
  - MIN: 4.5 V
  - TYP: 5.5 V
  - MAX: VDD
- Power-Supply Current: IDD
  - MIN: 0.5 mA
  - TYP: 0.65 mA
  - MAX: IDD
- Power-Supply Current in Shutdown: IDD(SHDN)
  - MIN: 2 µA
  - TYP: 10 µA
  - MAX: IDD
- Reference Current in Shutdown: 0 ±1 µA

### TIMING CHARACTERISTICS

- SCLK Clock Period: τCP
  - Note 4: 100 ns
- SCLK Pulse Width High: τCH
  - Typical: 40 ns
- SCLK Pulse Width Low: τCL
  - Typical: 40 ns
- CS Fall to SCLK Rise Setup Time: τCSS
  - Typical: 40 ns
- SCLK Rise to CS Rise Hold Time: τCSH
  - Typical: 0 ns
- SDI Setup Time: τDS
  - Typical: 40 ns
- SDI Hold Time: τDH
  - Typical: 0 ns
- SCLK Rise to DOUT Valid Propagation Delay: τD01
  - CL = 200pF
  - Typical: 80 ns
- SCLK Fall to DOUT Valid Propagation Delay: τD02
  - CL = 200pF
  - Typical: 80 ns
- SCLK Rise to CS Fall Delay: τCS0
  - Typical: 10 ns
- CS Rise to SCLK Rise Hold: τCS1
  - Typical: 40 ns
- CS Pulse Width High: τCSW
  - Typical: 100 ns

### Notes

- **Note 1:** Accuracy is specified from code 6 to code 4095.
- **Note 2:** Accuracy is better than 1LSB for VOUT greater than 6mV and less than VDD - 50mV. Guaranteed by PSRR test at the end points.
- **Note 3:** Digital inputs are set to either VDD or DGND, code = 0000 hex, RL = ∞.
- **Note 4:** SCLK inputs are set to either VDD or DGND, code = 0000 hex, RL = ∞.
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

Typical Operating Characteristics

(VDD = +5V, RL = 10kΩ, CL = 100pF, OS_ pins connected to AGND, TA = +25°C, unless otherwise noted.)

REFERENCE VOLTAGE INPUT
FREQUENCY RESPONSE

SUPPLY CURRENT vs. TEMPERATURE

TOTAL HARMONIC DISTORTION
PLUS NOISE vs. FREQUENCY

FULL-SCALE ERROR vs. RESISTIVE LOAD

REFERENCE FEEDTHROUGH AT 1kHz

SHUTDOWN CURRENT vs. TEMPERATURE

OUTPUT FFT PLOT

NOTE: RELATIVE TO FULL SCALE
Typical Operating Characteristics (continued)

(V_{DD} = +5V, R_L = 10k\Omega, C_L = 100pF, OS_ pins connected to AGND, T_A = +25°C, unless otherwise noted.)
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

**Detailed Description**

The MAX5104 dual, 12-bit, voltage-output DAC is easily configured with a 3-wire serial interface. The device includes a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input composed of an input register and a DAC register (see Functional Diagram). In addition, trimmed internal resistors produce an internal gain of +2V/V that maximizes output voltage swing. The amplifier’s offset-adjust pin allows for a DC shift in the DAC’s output.

Both DACs use an inverted R-2R ladder network that produces a weighted voltage proportional to the input voltage value. Each DAC has its own reference input to facilitate independent full-scale values. Figure 1 depicts a simplified circuit diagram of one of the two DACs.

**Reference Inputs**

The reference inputs accept both AC and DC values with a voltage range extending from 0 to (VDD - 1.4V). Determine the output voltage using the following equation (OS_ = AGND):

\[ V_{OUT} = \left( V_{REF} \cdot \frac{NB}{4096} \right) \cdot 2 \]

where NB is the numeric value of the DAC’s binary input code (0 to 4095) and VREF is the reference voltage.

The reference input impedance ranges from 14kΩ (1554 hex) to several gigohms (with an input code of 0000 hex). The reference input capacitance is code dependent and typically ranges from 15pF with an input code of all zeros to 50pF with a full-scale input code.

**Output Amplifier**

The MAX5104’s output amplifiers have internal resistors that provide for a gain of +2V/V when OS_ is connected to AGND. These resistors are trimmed to minimize gain error. The output amplifiers have a typical slew rate of 0.75V/μs and settle to 1/2LSB within 15μs, with a load of 10kΩ in parallel with 100pF. Loads less than 2kΩ degrade performance.

The OS_ pin can be used to produce an adjustable offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to the OS_ pin to produce an output range from 1V to (1V + VREF • 2). Note that the DAC’s output range is still limited by the maximum output voltage specification.

**Power-Down Mode**

The MAX5104 features a software-programmable shut-down mode that reduces the typical supply current to 2μA. The two DACs can be powered down independently, or simultaneously using the appropriate programming command. Enter power-down mode by writing the appropriate input-control word (Table 1). In power-down mode, the reference inputs and amplifier outputs become high impedance, and the serial interface remains active. Data in the input registers is saved.
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

allowing the MAX5104 to recall the output state prior to entering power-down when returning to normal mode. Exit power-down by recalling the previous condition or by updating the DAC with new information. When returning to normal operation (exiting power-down), wait 20µs for output stabilization.

### Serial Interface

The MAX5104’s 3-wire serial interface is compatible with both MICROWIRE (Figure 2) and SPI/QSPI (Figure 3) serial-interface standards. The 16-bit serial input word consists of 1 address bit, 2 control bits, 12 bits of data (MSB to LSB), and 1 sub-bit as shown in Figure 4. The address and control bits determine the MAX5104’s response, as outlined in Table 1.
The MAX5104's digital inputs are double buffered, which allows any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC registers concurrently. The address and control bits allow the DACs to act independently.

Send the 16-bit data as one 16-bit word (QSPI) or two 8-bit packets (SPI, MICROWIREF), with \( CS \) low during this period. The address and control bits determine which register will be updated, and the state of the registers when exiting power-down. The 3-bit address/control determines the following:

- Registers to be updated
- Clock edge on which data is to be clocked out via the serial-data output (DOUT)
- State of the user-programmable logic output
- Configuration of the device after power-down

The general timing diagram of Figure 5 illustrates how data is acquired. Driving \( CS \) low enables the device to receive data; otherwise, the interface control circuitry is disabled. With \( CS \) low, data at DIN is clocked into the register on the rising edge of SCLK. As \( CS \) goes high, data is latched into the input and/or DAC registers, depending on the address and control bits. The maximum clock frequency guaranteed for proper operation is 10MHz. Figure 6 shows a more detailed timing diagram of the serial interface.
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

Figure 6. Detailed Serial-Interface Timing Diagram

Figure 7. Daisy Chaining MAX5104s

Figure 8. Multiple MAX5104s Sharing a Common DIN Line
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

Serial-Data Output
The serial-data output, DOUT, is the internal shift register’s output. DOUT allows for daisy chaining of devices and data readback. The MAX5104 can be programmed to shift data out of DOUT on SCLK’s falling edge (Mode 0) or on the rising edge (Mode 1). Mode 0 provides a lag of 16 clock cycles, which maintains compatibility with SPI/QSPI and MICROWIRE interfaces. In Mode 1, the output data lags 15.5 clock cycles. On power-up, the device defaults to Mode 0.

User-Programmable Logic Output
User-programmable logic output (UPO) allows an external device to be controlled through the serial interface (Table 1), thereby reducing the number of microcontroller I/O pins required. On power-up, UPO is low.

Power-Down Lockout Input
The power-down lockout (PDL) pin disables software shutdown when low. When in power-down, transitioning PDL from high to low wakes up the part with the output set to the state prior to power-down. PDL can also be used to asynchronously wake up the device.

Daisy-Chaining Devices
Any number of MAX5104s can be daisy-chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5104’s DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. See the digital output VOH and VOL specifications in the Electrical Characteristics.

Figure 8 shows an alternate method of connecting several MAX5104s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input (CS) is required for each IC.

Applications Information

Unipolar Output
Figure 9 shows the MAX5104 configured for unipolar, rail-to-rail operation with a gain of +2V/V. The MAX5104 can produce a 0 to 4.096V output with a 2.048V reference (Figure 9). Table 2 lists the unipolar output codes. An offset to the output can be achieved by connecting a voltage to OS_, as shown in Figure 10. By applying VOS_ = -1V, the output values will range between 1V and (1V + VREF - 2).

Bipolar Output
The MAX5104 can be configured for a bipolar output (Figure 11). The output voltage is given by the equation (OS_ = AGND):

Table 2. Unipolar Code Table (Gain = +2)

<table>
<thead>
<tr>
<th>DAC CONTENTS</th>
<th>ANALOG OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 (0)</td>
<td>+VREF (4095)</td>
</tr>
<tr>
<td>1000 0000 0001 (0)</td>
<td>+VREF (2049)</td>
</tr>
<tr>
<td>1000 0000 0000 (0)</td>
<td>+VREF (2048)</td>
</tr>
<tr>
<td>0111 1111 1111 (0)</td>
<td>+VREF (2047)</td>
</tr>
<tr>
<td>0000 0000 0001 (0)</td>
<td>+VREF (1)</td>
</tr>
<tr>
<td>0000 0000 0000 (0)</td>
<td>0V</td>
</tr>
</tbody>
</table>
Low-Power, Dual, Voltage-Output, 12-Bit DAC with Serial Interface

\[ V_{OUT} = V_{REF} \left[ \left( 2 \cdot NB \right) / 4096 \right] - 1 \]

where NB represents the numeric value of the DAC’s binary input code. Table 3 shows digital codes and the corresponding output voltage for Figure 11’s circuit.

**Using an AC Reference**

In applications where the reference has an AC signal component, the MAX5104 has multiplying capabilities within the reference input voltage range specifications. Figure 12 shows a technique for applying a sinusoidal input to \( \text{REF}_- \), where the AC signal is offset before being applied to the reference input.

**Harmonic Distortion and Noise**

The total harmonic distortion plus noise (THD+N) is typically less than -78dB at full scale with a 1Vp-p input swing at 5kHz.

**Digital Calibration and Threshold Selection**

Figure 13 shows the MAX5104 in a digital calibration application. With a bright-light value applied to the photodiode (on), the DAC is digitally ramped until it trips the comparator. The microprocessor (\( \mu \)P) stores this “high” calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration.

---

**Table 3. Bipolar Code Table**

<table>
<thead>
<tr>
<th>DAC CONTENTS</th>
<th>MSB</th>
<th>LSB</th>
<th>ANALOG OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111 1111 111 (0)</td>
<td>+V_{REF} \left( \frac{2047}{2048} \right)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000 0000 000 (0)</td>
<td>+V_{REF} \left( \frac{1}{2048} \right)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0000 000 (0)</td>
<td>0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0111 1111 111 (0)</td>
<td>-V_{REF} \left( \frac{1}{2048} \right)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0000 000 (0)</td>
<td>+V_{REF} \left( \frac{2047}{2048} \right) \times 2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: () are for the sub-bit.
The µP then programs the DAC to set an output voltage at the midpoint of the two calibrated values. Applications include tachometers, motion sensing, automatic readers, and liquid-clarity analysis.

**Digital Control of Gain and Offset**

The two DACs can be used to control the offset and gain for curve-fitting nonlinear functions, such as transducer linearization or analog compression/expansion applications. The input signal is used as the reference for the gain-adjust DAC, whose output is summed with the output from the offset-adjust DAC. The relative weight of each DAC output is adjusted by R1, R2, R3, and R4 (Figure 14).

**Power-Supply Considerations**

On power-up, the input and DAC registers clear (set to zero code). For rated performance, $V_{REF}$ should be at least 1.4V below $V_{DD}$. Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize lead lengths to reduce lead inductance.

**Grounding and Layout Considerations**

Digital and AC transient signals on AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.