**General Description**

The MAX5099 offers a dual-output, high-switching-frequency DC-DC buck converter with an integrated high-side switch. The MAX5099 integrates two low-side MOSFET drivers to allow each converter to drive an external synchronous-rectifier MOSFET. Converter 1 delivers up to 2A output current, and converter 2 can deliver up to 1A of output current. The MAX5099 integrates load-dump protection circuitry that is capable of handling load-dump transients up to 80V for automotive applications. The load-dump protection circuit utilizes an internal charge pump to drive the gate of an external n-channel MOSFET. When an overvoltage or load-dump condition occurs, the series protection MOSFET absorbs the high voltage transient to prevent damage to lower voltage components.

The DC-DC converter operates over a wide 4.5V to 19V operating voltage range. The MAX5099 operates 180° out-of-phase with an adjustable switching frequency to minimize external components while allowing the ability to make trade-offs between the size, efficiency, and cost. The high switching frequency also allows these devices to operate outside the AM band for automotive applications. These regulators can be protected against high voltage transients such as a load-dump condition by using the integrated overvoltage controller.

This device utilizes voltage-mode control for stable operation and external compensation, so that the loop gain is tailored to optimize component selection and transient response. The MAX5099 has a maximum duty cycle of 92.5% and is synchronized to an external clock fed at the SYNC input.

Additional features include internal digital soft-start, individual enable for each DC-DC regulator (EN1 and EN2), open-drain power-good outputs (PGOOD1 and PGOOD2), and shutdown input (ON/OFF).

Other features of the MAX5099 include overvoltage protection and short-circuit (hiccup current limit) and thermal protection. The MAX5099 is available in a thermally enhanced, exposed pad 5mm x 5mm, 32-pin TQFN package and operates over the automotive -40°C to +125°C temperature range.

**Applications**

- Automotive AM/FM Radio Power Supply
- Automotive Instrument Cluster Display

**Features**

- Wide 4.5V to 5.5V or 5.2V to 19V Input Voltage Range with 80V Load-Dump Protection
- Dual-Output DC-DC Converter with Integrated Power MOSFETs
- Adjustable Outputs from 0.8V to 0.9VIN
- Output Current Capability Up to 2A and 1A
- Switching Frequency Programmable from 200kHz to 2.2MHz
- Synchronization Input (SYNC)
- Individual Converter Enable Input and Power-Good Output
- Low-IQ (7µA) Standby Current (ON/OFF)
- Internal Digital Soft-Start and Soft-Stop
- Short-Circuit Protection on Outputs and Maximum Duty-Cycle Limit
- Overvoltage Protection on Outputs with Auto Restart
- Thermal Shutdown
- Thermally Enhanced 32-Pin TQFN Package Dissipates Up to 2.7W at +70°C

**Ordering Information**

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX5099ATJ+</td>
<td>-40°C to +125°C</td>
<td>32 TQFN-EP*</td>
</tr>
</tbody>
</table>

*Denotes a lead-free package.

*EP = Exposed pad.

Pin Configuration appears at end of data sheet.
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to SGND</td>
<td>V+</td>
<td>-0.3V to +25V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V+ to IN_HIGH</td>
<td>V+</td>
<td>-19V to +19V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IN_HIGH to SGND</td>
<td>IN_HIGH</td>
<td>-0.3V to +19V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IN_HIGH Maximum Input Current</td>
<td>I_{IL}</td>
<td>60mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BYPASS to SGND</td>
<td>I_{VL}</td>
<td>-0.3V to +2.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GATE to V+</td>
<td>I</td>
<td>-0.3V to +12V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GATE to SGND</td>
<td>I</td>
<td>-0.3V to +36V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SGND to PGND</td>
<td>I</td>
<td>-0.3V to +0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vj</td>
<td>I</td>
<td>-0.3V to the Lower of +6V or (V+ + 0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDRV to SGND</td>
<td>I</td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BST1/VDD1, BST2/VDD2, DRAIN_</td>
<td>I</td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PGOOD_ to SGND</td>
<td>I</td>
<td>-0.3V to +30V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON/OFF to SGND</td>
<td>I</td>
<td>-0.3V to (IN_HIGH + 0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BST1/VDD1 to SOURCE1</td>
<td>I</td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BST2/VDD2 to SOURCE2</td>
<td>I</td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOURCE_ to SGND</td>
<td>I</td>
<td>-0.6V to +25V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN_ to SGND</td>
<td>I</td>
<td>-0.3V to +6V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OSC, FSEL_1, COMP_, SYNC, FB_, COMP_, V+</td>
<td>I</td>
<td>-0.3V to (VL + 0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DL_ to PGND</td>
<td>I</td>
<td>-0.3V to (VDRV + 0.3V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOURCE1, DRAIN1 Peak Current</td>
<td>I</td>
<td>5A for 1ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOURCE2, DRAIN2 Peak Current</td>
<td>I</td>
<td>3A for 1ms</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V+ to SGND short circuit</td>
<td>I</td>
<td>Continuous, Internally Limited</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Power Dissipation (TA = +70°C)</td>
<td></td>
<td>2759mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Junction-to-Ambient Thermal Resistance (θJA)</td>
<td></td>
<td>29.0°C/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Junction-to-Case Thermal Resistance (θJC)</td>
<td></td>
<td>1.7°C/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>-40°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td></td>
<td>+150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td></td>
<td>+300°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specifications. For detailed information on package thermal considerations refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(VDRV = VL, V+ = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = VL; SYNC = GND, IVL = 0mA, PGND = SGND, CBYPASS = 0.22μF (low ESR), CVL = 4.7μF (ceramic), CV+ = 1μF (low ESR), CIN_HIGH = 1μF (ceramic), R_{IN_HIGH} = 3.9kΩ, ROSC = 10kΩ, TJ = -40°C to +125°C, unless otherwise noted.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>V+</td>
<td>V+ = IN_HIGH, Figure 6 (Note 3)</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V+ Operating Supply Current</td>
<td>I_Q</td>
<td>V+ unloaded, no switching, VFB_ = 1V</td>
<td>4.2</td>
<td>6.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>V+ Standby Supply Current</td>
<td>I_{V+STBY}</td>
<td>V_{ENL} = 0V, PGOOD_ unconnected, V+ = V_{IN_HIGH} = 14V</td>
<td>0.75</td>
<td>1.1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>η</td>
<td>VOUT1 = 5V at 1.5A, VOUT2 = 3.3V at 0.75A, f_{SW} = 300kHz</td>
<td>V+ = V+ = 5.2V</td>
<td>86</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V+ = 12V</td>
<td>85</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V+ = 16V</td>
<td>85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OVERVOLTAGE PROTECTOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IN_HIGH Clamp Voltage</td>
<td>IN_HIGH</td>
<td>ISINK = 10mA</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>V</td>
</tr>
<tr>
<td>IN_HIGH Clamp Load Regulation</td>
<td></td>
<td>1mA &lt; ISINK &lt; 50mA</td>
<td>160</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IN_HIGH Supply Current</td>
<td>IN_HIGH</td>
<td>V_{ENL} = VPGOOD_ = VGATE = 0V, VIN_HIGH = VN/OFF = 14V</td>
<td>270</td>
<td>600</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>IN_HIGH Standby Supply Current</td>
<td>IN_HIGHSTBY</td>
<td>VN/OFF = 0V, VPGOOD_ = V+ = unconnected, VIN_HIGH = 14V</td>
<td>7</td>
<td>9</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V+ to IN_HIGH Overvoltage Clamp</td>
<td>V_{OV}</td>
<td>V_{OV} = V+ - VIN_HIGH, IGATE = -1mA</td>
<td>1.20</td>
<td>1.85</td>
<td>2.50</td>
<td>V</td>
</tr>
</tbody>
</table>
**MAX5099**

**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**ELECTRICAL CHARACTERISTICS (continued)**

(VDRV = VL, V+ = VL = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = VL, SYNC = GND, Ivl = 0mA, PGND = SGND, CBYPASS = 0.22μF (low ESR), CVL = 4.7μF (ceramic), CV+ = 1μF (low ESR), CIN_HIGH = 1μF (ceramic), R_IN_HIGH = 3.9kΩ, ROSC = 10kΩ, Tj = -40°C to +125°C, unless otherwise noted.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_HIGH Startup Voltage</td>
<td>IN_HIGH UVLO</td>
<td>Rising, ON/OFF = IN_HIGH, GATE rising</td>
<td>3.6</td>
<td>4.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling, ON/OFF = IN_HIGH, GATE falling</td>
<td>3.45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GATE Charge Current</td>
<td>IGATE_CH</td>
<td>V_IN HIGH = V_ON/OFF = 14V, VGATE = V+ = 0V</td>
<td>20</td>
<td>45</td>
<td>80</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIN_HIGH = V+ = VIN_ON/OFF = 4.5V, IGATE = 1μA</td>
<td>4.0</td>
<td>5.3</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V+ = VIN_HIGH = V_ON/OFF = 14V, IGATE = 1μA</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GATE Turn-Off Pulldown Current</td>
<td>IGATE_PD</td>
<td>V_IN HIGH = 14V, V_ON/OFF = 0V, V+ = 0V, VGATE = 5V</td>
<td>3.6</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**STARTUP/VL REGULATOR**

| VL Undervoltage-Lockout Trip Level | UVLO | VL falling | 3.9 | 4.1 | 4.3 | V |
| VL Undervoltage-Lockout Hysteresis | | | 180 | | | mV |
| VL Output Voltage |VL | ISOURCE_ = 0 to 40mA, 5.5V ≤ V+ ≤ 19V | 5.0 | 5.2 | 5.5 | V |
| VL LDO Short-Circuit Current |VL_SHORT | V+ = VIN_HIGH = 5.2V | 130 | | | mA |
| VL LDO Dropout Voltage |VLDO | ISOURCE_ = 40mA, V+ = VIN_HIGH = 4.5V | 300 | 550 | | mV |

**BYPASS OUTPUT**

| BYPASS Voltage | VBYPASS | | 1.98 | 2.00 | 2.02 | V |
| BYPASS Load Regulation | ΔVBYPASS | 0 < IBYPASS < 100μA (sourcing) | 2 | 5 | | mV |

**SOFT-START/SOFT-STOP**

| Digital Ramp Period Soft-Start/Soft-Stop | Internal 6-bit DAC | 2048 | | | | |
| Soft-Start/Soft-Stop Steps | | | 64 | | | Steps |

**VOLTAGE-ERROR AMPLIFIER**

| FB_ Input Bias Current | IFB_ | 250 | | | | nA |
| FB_ Input-Voltage Set Point | VFB_ | -40°C ≤ TA ≤ +85°C | 0.783 | 0.8 | 0.809 | |
| | | -40°C ≤ TA ≤ +125°C | 0.785 | 0.814 | | |
| FB_ to COMP_ Transconductance | gM | 1.4 | 2.4 | 3.4 | | mS |

**INTERNAL MOSFETs**

| On-Resistance High-Side MOSFET Converter 1 | RON1 | | 195 | | | mΩ |
| | ISWITCH = 100mA, BST1/VDD1 to VSOURCE1 = 5.2V | | 208 | 355 | | |
# Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

## ELECTRICAL CHARACTERISTICS (continued)

(VDRV = VL, V+ = VIN_HIGH = 5.2V or V+ = VIN_HIGH = 5.2V to 19V, EN_ = VL, SYNC = GND, IVL = 0mA, PGND = SGND, 
C_BYPASS = 0.22μF (low ESR), CVL = 4.7μF (ceramic), CV+ = 1μF (low ESR), C_IN_HIGH = 1μF (ceramic), R_IN_HIGH = 3.9kΩ, 
ROSC = 10kΩ, Tj = -40°C to +125°C, unless otherwise noted.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-Resistance High-Side MOSFET Converter 2</td>
<td>R_ON2</td>
<td>ISWITCH = 100mA, BST2/VDD2 to VSOURCE2 = 5.2V</td>
<td>280</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ISWITCH = 100mA, BST2/VDD2 to VSOURCE2 = 4.5V</td>
<td>300</td>
<td>520</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Converter 1 Output Current</td>
<td>I_OUT1</td>
<td>VOUT1 = 5V, V+ = 12V (Note 4)</td>
<td>2</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Minimum Converter 2 Output Current</td>
<td>I_OUT2</td>
<td>VOUT2 = 3.3V, V+ = 12V (Note 4)</td>
<td>1</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Converter 1/Converter 2 MOSFET DRAIN_ Leakage Current</td>
<td>I_LK12</td>
<td>VEN1 = VEN2 = 0V, VDS = 19V, VDRAIN_ = 19V, VSOURCE_ = 0V</td>
<td>20</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Internal Weak Low-Side Switch On-Resistance</td>
<td>R_ONLSSW_</td>
<td>I_LSSW = 30mA</td>
<td>22</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

### INTERNAL SWITCH CURRENT LIMIT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Switch Current-Limit Converter 1</td>
<td>I_CL1</td>
<td>V+ = VIN_HIGH = 5.2V, VL = VDRV = VBST_/VDD_ = 5.2V</td>
<td>2.8</td>
<td>3.45</td>
<td>4.3</td>
<td>A</td>
</tr>
<tr>
<td>Internal Switch Current-Limit Converter 2</td>
<td>I_CL2</td>
<td>V+ = VIN_HIGH = 5.2V, VL = VDRV = VBST_/VDD_ = 5.2V</td>
<td>1.75</td>
<td>2.10</td>
<td>2.60</td>
<td>A</td>
</tr>
</tbody>
</table>

### SWITCHING FREQUENCY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM Maximum Duty Cycle</td>
<td>D_MAX</td>
<td>SYNC = SGND, f_SW = 1.25MHz</td>
<td>90</td>
<td>92</td>
<td>100</td>
<td>%</td>
</tr>
<tr>
<td>Switching Frequency Range</td>
<td>f_SW</td>
<td></td>
<td>200</td>
<td>2200</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>f_SW</td>
<td>ROSC = 6.81kΩ, each converter</td>
<td>1.7</td>
<td>1.9</td>
<td>2.1</td>
<td>MHz</td>
</tr>
<tr>
<td>Switching Frequency Accuracy</td>
<td></td>
<td>5.6kΩ &lt; ROSC &lt; 10kΩ, 1%</td>
<td>5</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10kΩ &lt; ROSC &lt; 62.5kΩ, 1%</td>
<td>7</td>
<td>%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| SYNC Frequency Range | fSYNC | Each converter switching frequency is half of the SYNC input frequency, 
FSEL_1 = VL (see the Setting the Switching Frequency section) | 400 | 4400 | kHz |
| SYNC High Threshold | V_SYNCH | | 2 | V |
| SYNC Low Threshold | V_SYNCL | | 0.8 | V |
| SYNC Input Leakage | I_SYNC_LEAK | | 2 | μA |
| SYNC Input Minimum Pulse Width | T_SYNCIN | | 100 | ns |
| Sync to Source 1 Phase Delay | T_SYNC_PHASE | ROSC = 62.5kΩ | 90 | Degrees |
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**ELECTRICAL CHARACTERISTICS (continued)**

(VDRV = VL, V+ = V+ = IN_HIGH = 5.2V or V+ = IN_HIGH = 5.2V to 19V, EN_ = VL, SYNC = GND, IyL = 0mA, PGND = SGND, CBYPASS = 0.22μF (low ESR), CVL = 4.7μF (ceramic), CV+ = 1μF (low ESR), CIN_HIGH = 1μF (ceramic), RIN_HIGH = 3.9kΩ, ROSC = 10kΩ, TJ = -40°C to +125°C, unless otherwise noted.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTERNAL DL_ DRIVERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rds(on) DL_ Sink</td>
<td>RONDLN</td>
<td>ISINK = 200mA</td>
<td>1</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Rds(on) DL_ Source</td>
<td>RONDLP</td>
<td>ISOURCE = 200mA</td>
<td>1.8</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Break-Before-Make Time</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>FSEL_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSEL_1 Input High Threshold</td>
<td>VIH</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>FSEL_1 Input Low Threshold</td>
<td>VIL</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>FSEL_1 Input Leakage</td>
<td>IFSEL_1_LEAK</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>ON/OFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON/OFF Input High Threshold</td>
<td>VIH</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ON/OFF Input Low Threshold</td>
<td>VIL</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ON/OFF Input Leakage Current</td>
<td>ION/OFF_LEAK</td>
<td>VON/OFF = 5V</td>
<td>0.35</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>EN_ INPUTS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN_ Input High Threshold</td>
<td>VIH</td>
<td>EN_ rising</td>
<td>1.9</td>
<td>2.0</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>EN_ Input Hysteresis</td>
<td>VEN_HYS</td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN_ Input Leakage Current</td>
<td>IEN_LEAK</td>
<td></td>
<td>-1</td>
<td>+1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>POWER-GOOD OUTPUT (PGOOD1, PGOOD2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PGOOD_ Threshold</td>
<td>VTPGOOD_</td>
<td>Falling</td>
<td>90</td>
<td>92.5</td>
<td>95</td>
<td>% VFB</td>
</tr>
<tr>
<td>PGOOD_ Output Voltage</td>
<td>VPGOOD_</td>
<td>ISINK = 3mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>PGOOD_ Output Leakage Current</td>
<td>ILPGOOD_</td>
<td>V+ = VL = VIN_HIGH = VEN_ = 5.2V, VPGOOD_ = 23V, VFB_ = 1V</td>
<td>2</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>OUTPUT OVERVOLTAGE PROTECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB_ OVP Threshold Rising</td>
<td>VDVP_R</td>
<td></td>
<td>107</td>
<td>114</td>
<td>121</td>
<td>% VFB</td>
</tr>
<tr>
<td>FB_ OVP Threshold Falling</td>
<td>VDVP_F</td>
<td></td>
<td>112.5</td>
<td></td>
<td></td>
<td>% VFB</td>
</tr>
<tr>
<td>THERMAL PROTECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>TSHDN</td>
<td>Rising</td>
<td>+165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Hysteresis</td>
<td>THYST</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 2:** 100% tested at TA = +25°C and TA = +125°C. Specifications at TA = -40°C are guaranteed by design and not production tested.

**Note 3:** Operating supply range (V+) is guaranteed by Vl line regulation test. Connect V+ to IN_HIGH and Vl for 5V operation.

**Note 4:** Output current is limited by the power dissipation of the package; see the Power Dissipation section in the Applications Information section.
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Typical Operating Characteristics

(V+ = V_IN_HIGH = 14V, unless otherwise noted. V+ = V_IN_HIGH means that N1 is shorted externally.)

- **Output1 Efficiency vs. Load Current**
- **Output2 Efficiency vs. Load Current**
- **Output1 Voltage vs. Load Current**
- **Output2 Voltage vs. Load Current**
- **V_L Output Voltage vs. Converter Switching Frequency**
- **Each Converter Switching Frequency vs. ROSC**
- **Each Converter Switching Frequency vs. Temperature**
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Typical Operating Characteristics (continued)

(V+ = VIN_HIGH = 14V, unless otherwise noted. V+ = VIN_HIGH means that N1 is shorted externally.)
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

**Typical Operating Characteristics (continued)**

\[(V_+ = V_{\text{IN\_HIGH}} = 14V, \text{unless otherwise noted. } V_+ = V_{\text{IN\_HIGH}} \text{ means that N1 is shorted externally.})\]

**FB VOLTAGE vs. TEMPERATURE**

\[
\begin{array}{c|c|c|c|c}
\text{TEMPERATURE (°C)} & \text{78.5} & \text{80.0} & \text{80.5} & \text{81.0} \\
\text{FB VOLTAGE (V)} & 0.785 & 0.790 & 0.795 & 0.800 \\
\end{array}
\]

**BYPASS VOLTAGE vs. TEMPERATURE**

\[
\begin{array}{c|c|c|c|c|c|c}
\text{TEMPERATURE (°C)} & \text{-40} & \text{0} & \text{30} & \text{135} & \text{135} & \text{135} \\
\text{BYPASS VOLTAGE (V)} & 1.990 & 1.992 & 1.994 & 2.000 & 2.002 & 2.004 \\
\end{array}
\]

**EXTERNAL SYNCHRONIZATION**

\[\text{FSEL}_1 = \text{VL}\]

\[\text{SYNC} 5\text{V/div} \]

\[\text{SOURCE1} 10\text{V/div} \]

\[\text{SOURCE2} 10\text{V/div} \]

\[\text{GATE} 10\text{V/div} \]

\[\text{V+} 10\text{V/div} \]

\[\text{PGOOD2} 10\text{V/div} \]

**EXTERNAL SYNCHRONIZATION**

\[\text{FSEL}_1 = \text{SGND}\]

\[\text{SYNC} 5\text{V/div} \]

\[\text{SOURCE1} 10\text{V/div} \]

\[\text{SOURCE2} 10\text{V/div} \]

\[\text{GATE} 10\text{V/div} \]

\[\text{V+} 10\text{V/div} \]

**OUT-OF-PHASE OPERATION**

\[\text{FSEL}_1 = \text{SGND}\]

\[\text{SOURCE1} 10\text{V/div} \]

\[\text{SOURCE2} 10\text{V/div} \]

\[\text{DL1} 10\text{V/div} \]

\[\text{DL2} 10\text{V/div} \]

**OVP BEHAVIOR**

\[\text{VOUT1} 10\text{V/div} \]

\[\text{VOUT2} 10\text{V/div} \]

\[\text{GATE} 10\text{V/div} \]
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**Typical Operating Characteristics (continued)**

(V+ = V\text{IN\_HIGH} = 14V, unless otherwise noted. V+ = V\text{IN\_HIGH} means that N1 is shorted externally.)

- **BYPASS VOLTAGE vs. BYPASS CURRENT**
- **V+ SWITCHING SUPPLY CURRENT vs. SWITCHING FREQUENCY**
- **V+ STANDBY SUPPLY CURRENT vs. TEMPERATURE**
- **IN\_HIGH SHUTDOWN CURRENT vs. TEMPERATURE**
- **IN\_HIGH STANDBY CURRENT vs. TEMPERATURE**


**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**Typical Operating Characteristics (continued)**

(V+ = VIN_HIGH = 14V, unless otherwise noted. V+ = VIN_HIGH means that N1 is shorted externally.)

**IN_HIGH CLAMP VOLTAGEx vs. CLAMP CURRENT**

![IN_HIGH CLAMP VOLTAGE vs. CLAMP CURRENT graph](image)

**V+ TO IN_HIGH CLAMP VOLTAGEx vs. GATE SINK CURRENT**

![V+ TO IN_HIGH CLAMP VOLTAGE vs. GATE SINK CURRENT graph](image)

**IN_HIGH CLAMP VOLTAGEx vs. CLAMP CURRENT**

![IN_HIGH CLAMP VOLTAGE vs. CLAMP CURRENT graph](image)

**SYSTEM TURN-ON FROM BATTERY**

![SYSTEM TURN-ON FROM BATTERY graph](image)

**SYSTEM TURN-OFF FROM BATTERY**

![SYSTEM TURN-OFF FROM BATTERY graph](image)

**SYSTEM LOAD DUMP**

![SYSTEM LOAD DUMP graph](image)
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**Pin Description**

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 32</td>
<td>SOURCE2</td>
<td>Converter 2 Internal MOSFET Source Connection. For buck converter operation, connect SOURCE2 to the switched side of the inductor. For boost operation, connect SOURCE2 to PGND (Figure 5).</td>
</tr>
<tr>
<td>2, 3</td>
<td>DRAIN2</td>
<td>Converter 2 Internal MOSFET Drain Connection. For buck converter operation, use the MOSFET as a high-side switch and connect DRAIN2 to the DC-DC converters supply input rail. For boost converter operation, use the MOSFET as a low-side switch and connect DRAIN2 to the inductor and diode junction (Figure 5).</td>
</tr>
<tr>
<td>4</td>
<td>PGOOD2</td>
<td>Converter Open-Drain Power-Good Output. PGOOD2 goes low when converter 2's output falls below 92.5% of its set regulation voltage. Use PGOOD2 and EN1 to sequence the converters.</td>
</tr>
<tr>
<td>5</td>
<td>EN2</td>
<td>Converter 2 Active-High Enable Input. Connect to VIL for always-on operation.</td>
</tr>
<tr>
<td>6</td>
<td>FB2</td>
<td>Converter 2 Feedback Input. Connect FB2 to a resistive divider between converter 2's output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB2 to a resistive voltage-divider from BYPASS to regulator 2's output (Figure 2). See the Setting the Output Voltage section.</td>
</tr>
<tr>
<td>7</td>
<td>COMP2</td>
<td>Converter 2 Internal Transconductance Amplifier Output. See the Compensation section.</td>
</tr>
<tr>
<td>8</td>
<td>OSC</td>
<td>Oscillator Frequency Set Input. Connect a resistor from OSC to SGND (Rosc) to set the switching frequency (see the Setting the Switching Frequency section). Set Rosc for an oscillator frequency equal to the SYNC input frequency when using external synchronization. Rosc is still required when an external clock is connected to the SYNC input. See the Synchronization (SYNC) section.</td>
</tr>
<tr>
<td>9</td>
<td>SYNC</td>
<td>External Clock Synchronization Input. Connect SYNC to a 400kHz to 4400kHz clock to synchronize the switching frequency with the system clock. Each converter frequency is 1/2 of the frequency applied to SYNC (FSEL_1 = VL). For FSEL_1 = SGND, the switching frequency of converter 1 becomes 1/4 of the SYNC frequency. Connect SYNC to SGND when not used.</td>
</tr>
<tr>
<td>10</td>
<td>GATE</td>
<td>Gate Drive Output. Connect to the gate of the external n-channel load-dump protection MOSFET. GATE = IN HIGH + 9V (typ) with IN HIGH = 12V. GATE pulls to IN HIGH by an internal n-channel MOSFET when V+ raises 2V above IN HIGH. Leave GATE unconnected if the load-dump protection is not used (MOSFET not installed).</td>
</tr>
<tr>
<td>11</td>
<td>ON/OFF</td>
<td>n-Channel Switch Enable Input. Drive ON/OFF high for normal operation. Drive ON/OFF low to turn off the external n-channel load-dump protection MOSFET and reduce the supply current to 7µA (typ). When ON/OFF is driven low, both DC-DC converters are disabled and the PGOOD_ outputs are driven low. Connect to V+ if the external load-dump protection is not used (MOSFET not installed).</td>
</tr>
<tr>
<td>12</td>
<td>IN HIGH</td>
<td>Startup Input. IN HIGH is protected by internally clamping to 21V (max). Connect a resistor (4kΩ max) from IN HIGH to the drain of the protection switch. Bypass IN_HIGH with a 4.7µF electrolytic or 1µF minimum ceramic capacitor. Connect to V+ if the external load-dump protection is not used (MOSFET not installed).</td>
</tr>
<tr>
<td>13</td>
<td>V+</td>
<td>Input Supply Voltage. V+ can range from 5.2V to 19V. Connect V+, IN HIGH, and VL together for 4.5V to 5.5V input operation. Bypass V+ to SGND with a 4.7µF minimum ceramic capacitor.</td>
</tr>
<tr>
<td>14</td>
<td>VL</td>
<td>Internal Regulator Output. The VL regulator is used to supply the drive current at input VDRV. When driving VDRV, use an RC lowpass filter to decouple switching noise from VDRV to the VL regulator (see the Typical Application Circuit). Bypass VL to SGND with a 4.7µF minimum ceramic capacitor.</td>
</tr>
</tbody>
</table>
## Pin Description (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>SGND</td>
<td>Signal Ground. Connect SGND to exposed pad and to the board signal ground plane. Connect the board signal ground and power ground planes together at a single point.</td>
</tr>
<tr>
<td>16</td>
<td>BYPASS</td>
<td>Reference Output Bypass Connection. Bypass to SGND with a 0.22μF or greater ceramic capacitor.</td>
</tr>
<tr>
<td>17</td>
<td>FSEL_1</td>
<td>Converter 1 Frequency Select Input. Connect FSEL_1 to VL for normal operation. Connect FSEL_1 to SGND to reduce converter 1’s switching frequency to 1/2 of converter 2’s switching frequency (converter 1 switching frequency is 1/4 the SYNC frequency). Do not leave FSEL_1 unconnected.</td>
</tr>
<tr>
<td>18</td>
<td>COMP1</td>
<td>Converter 1 Internal Transconductance Amplifier Output. See the Compensation section.</td>
</tr>
<tr>
<td>19</td>
<td>FB1</td>
<td>Converter 1 Feedback Input. Connect FB1 to a resistive divider between converter 1’s output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage-divider from BYPASS to regulator 1’s output (Figure 2). See the Setting the Output Voltage section.</td>
</tr>
<tr>
<td>20</td>
<td>EN1</td>
<td>Converter 1 Active-High Enable Input. Connect to VL for an always-on operation.</td>
</tr>
<tr>
<td>21</td>
<td>PGOOD1</td>
<td>Converter 1 Power-Good Output. Open-drain output goes low when converter 1’s output falls below 92.5% of its set regulation voltage. Use PGOOD1 and EN2 to sequence the converters (converter 1 starts first).</td>
</tr>
<tr>
<td>22, 23</td>
<td>DRAIN1</td>
<td>Converter 1 Internal MOSFET Drain Connection. For buck converter operation, use the MOSFET as a high-side switch and connect DRAIN1 to the DC-DC converters supply input rail. For boost converter operation, use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction (Figure 5).</td>
</tr>
<tr>
<td>24, 25</td>
<td>SOURCE1</td>
<td>Converter 1 Internal MOSFET Source Connection. For buck operation, connect SOURCE1 to the switched side of the inductor. For boost operation, connect SOURCE1 to the switched side of the inductor. For boost operation, connect SOURCE1 to the switched side of the inductor. For boost operation, connect SOURCE1 to the switched side of the inductor.</td>
</tr>
<tr>
<td>26</td>
<td>BST1/VDD1</td>
<td>Converter 1 Bootstrap Flying-Capacitor Connection. For buck converter operation, connect BST1/VDD1 to a 0.1μF ceramic capacitor and diode according to the Typical Application Circuit. For boost converter operation, driver bypass capacitor connection. Connect to VDRV and bypass with a 0.1μF ceramic capacitor to PGND (Figure 5).</td>
</tr>
<tr>
<td>27</td>
<td>VDRV</td>
<td>Low-Side Driver Supply Input. Connect VDRV to VL through an RC filter to bypass switching noise to the internal VL regulator. For buck converter operation, connect anode terminals of external bootstrap diodes to VDRV. For boost converter operation, connect VDRV to BST1/VDD1 and BST2/VDD2. Bypass with a minimum 2.2μF ceramic capacitor to PGND (see the Typical Application Circuit). Do not connect to an external supply.</td>
</tr>
<tr>
<td>28</td>
<td>DL1</td>
<td>Converter 1 Low-Side Synchronous-Rectifier Gate Driver Output</td>
</tr>
<tr>
<td>29</td>
<td>PGND</td>
<td>Power Ground. Connect to the board power ground plane.</td>
</tr>
<tr>
<td>30</td>
<td>DL2</td>
<td>Converter 2 Low-Side Synchronous-Rectifier Gate Driver Output</td>
</tr>
<tr>
<td>31</td>
<td>BST2/VDD2</td>
<td>Converter 2 Bootstrap Flying-Capacitor Connection. For buck converter operation, connect BST2/VDD2 to a 0.1μF ceramic capacitor and diode according to the Typical Application Circuit. For boost converter operation, driver bypass capacitor connection. Connect to VDRV and bypass with a 0.1μF ceramic capacitor from BST2/VDD2 to PGND (Figure 5).</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>Exposed Pad. Connect EP to SGND. For enhanced thermal dissipation, connect EP to a copper area as large as possible. Do not use EP as the sole ground connection.</td>
</tr>
</tbody>
</table>
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Functional Diagram
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

**Detailed Description**

### PWM Controller

The MAX5099 dual DC-DC converters use a pulse-width-modulation (PWM) voltage-mode control scheme. On each converter the device includes one integrated n-channel MOSFET switch and requires an external low-forward-drop Schottky diode for output rectification. The controller generates the clock signal by dividing down the internal oscillator (fOSC) or the SYNC input when driven by an external clock; therefore, each controller’s switching frequency equals half the oscillator frequency (fSW = fOSC/2) or half of the SYNC input frequency (fSW = fSYNC/2). An internal transconductance error amplifier produces an integrated error voltage at COMP_, providing high DC accuracy. The voltage at COMP_ sets the duty cycle using a PWM comparator and a ramp generator. At each rising edge of the clock, converter 1’s MOSFET switch turns on and remains on until either the appropriate or maximum duty cycle is reached, or the maximum current limit for the switch is reached. Converter 2 operates 180° out-of-phase, so its MOSFET switch turns on at each falling edge of the clock.

In the case of buck operation (see the Typical Application Circuit), the internal MOSFET is used in high-side configuration. During each MOSFET’s on-time, the associated inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and forward biases the Schottky rectifier. During this time, the SOURCE_ voltage is clamped to a diode drop (VD) below ground. A low-forward-voltage-drop (0.4V) Schottky diode must be used to ensure the SOURCE_ voltage does not go below -0.6V absolute max. The inductor releases the stored energy as its current ramps down, and provides current to the output. The bootstrap capacitor is also recharged when the SOURCE_ voltage goes low during the high-side MOSFET off-time. The maximum duty-cycle limits ensure proper bootstrap charging at startup or low input voltages. The circuit goes in discontinuous conduction mode operation at light load, when the inductor current completely discharges before the next cycle commences. Under overload conditions, when the inductor current exceeds the peak current limit of the respective switch, the high-side MOSFET turns off quickly and waits until the next clock cycle.

### Synchronous-Rectifier Output

The MAX5099 is intended mostly for synchronous buck operation with an external synchronous-rectifier MOSFET. During the internal high-side MOSFET on-time, the inductor current ramps up. When the high-side MOSFET turns off, the inductor reverses polarity and forward biases the Schottky rectifier in parallel with the low-side external synchronous MOSFET. The SOURCE_ voltage is clamped to 0.5V below ground until the adaptive break-before-make time (tBBM) of 25ns is over. After tBBM, the synchronous-rectifier MOSFET turns on, thus bypassing the Schottky rectifier and reducing the conduction loss during the inductor freewheeling time. The synchronous-rectifier MOSFET keeps the circuit in continuous conduction mode operation even at light load because the inductor current is allowed to go negative.

The MAX5099, with the synchronous-rectifier driver output (DL_), has an adaptive break-before-make circuit to avoid cross-conduction between the internal power MOSFET and the external synchronous-rectifier MOSFET. When the synchronous-rectifier MOSFET is turning off, the internal high-side power MOSFET is kept off until VDL falls below 0.97V. Similarly, DL_ does not go high until the internal power MOSFET gate voltage falls below 1.24V.

### Load-Dump Protection

Most automotive applications are powered by a multi-cell, 12V lead-acid battery with a voltage from 9V to 16V (depending on load current, charging status, temperature, battery age, etc.). The battery voltage is distributed throughout the automobile and is locally regulated down to voltages required by the different system modules. Load dump occurs when the alternator is charging the battery and the battery becomes disconnected. Power in the alternator inductance flows into the distributed power system and elevates the voltage seen at each module. The voltage spikes have rise times typically greater than 5ms and decays within several hundred milliseconds but can extend out to 1s or more depending on the characteristics of the charging system. These transients are capable of destroying sensitive electronic equipment on the first fault event. During load dump, the MAX5099 provides the ability to clamp the input-voltage rail of the internal DC-DC converters to a safe level, while preventing power discontinuity at the DC-DC converters’ outputs.

The load-dump protection circuit utilizes an internal charge pump to drive the gate of an external n-channel MOSFET. This series-protection MOSFET absorbs the load-dump overvoltage transient and operates in saturation over the normal battery range to minimize power dissipation. During load dump, the gate voltage of the protection MOSFET is regulated to prevent the source terminal from exceeding 19V.

The DC-DC converters are powered from the source terminal of the load-dump protection MOSFET, so that their input voltage is limited during load dump and can operate normally.
ON/OFF
The MAX5099 provide an input (ON/OFF) to turn on and off the external load-dump protection MOSFET. Drive ON/OFF high for normal operation. Drive ON/OFF low to turn off the external n-channel load-dump protection MOSFET and reduce the supply current to 7μA (typ). When ON/OFF is driven low, both converters are also turned off, and the PGOOD_ outputs are driven, low. V+ will be self-discharged through the converters’ output currents and the IC supply current.

Internal Oscillator/
Out-of-Phase Operation
The internal oscillator generates the 180° out-of-phase clock signal required by each regulator. The switching frequency of each converter (fSW) is programmable from 200kHz to 2.2MHz using a single 1% resistor at ROSC. See the Setting the Switching Frequency section.

With dual-synchronized out-of-phase operation, the MAX5099’s internal MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced RMS ripple current and input-voltage ripple. This reduces the required input capacitor ripple current rating, allows for fewer or less expensive capacitors, and reduces shielding requirements for EMI.

Synchronization (SYNC)
The main oscillator can be synchronized to the system clock by applying an external clock (fSYNC) at SYNC. The fSYNC frequency must be twice the required operating frequency of an individual converter. Use a TTL logic signal for the external clock with at least a 100ns pulse width. ROSC is still required when using external synchronization. Program the internal oscillator frequency to have fSW = 1/2 fSYNC. The device is properly synchronized if the SYNC frequency fSYNC varies within the range ±20%.

Short SYNC to SGND if unused.

Input Voltage (V+)/
Internal Linear Regulator (VL)
All internal control circuitry operates from an internally regulated nominal voltage of 5.2V (VL). At higher input voltages (V+) of 5.2V to 19V, VL is regulated to 5.2V. At 5.2V or below, the internal linear regulator operates in dropout mode, where VL follows V+. Depending on the load on VL, the dropout voltage can be high enough to reduce VL below the undervoltage-lockout (UVLO) threshold. Do not use VL to power external circuitry.

For input voltages less than 5.5V, connect V+ and VL together. The load on VL is proportional to the switching frequency of converter 1 and converter 2. See the VL Output Voltage vs. Converter Switching Frequency graph in the Typical Operating Characteristics. For input voltage ranges higher than 5.5V, disconnect VL from V+.

Bypass V+ to SGND with a 1μF or greater ceramic capacitor placed close to the MAX5099. Bypass VL with a low-ESR 4.7μF ceramic capacitor to SGND.

Undervoltage Lockout/
Soft-Start/Soft-Stop
The MAX5099 includes an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on and monotonic rise of the output voltage. The falling UVLO threshold is internally set to 4.1V (typ) with 180mV hysteresis. Hysteresis at UVLO eliminates “chattering” during startup. When VL drops below UVLO, the internal MOSFET switches are turned off.

The MAX5099 digital soft-start reduces input inrush currents and glitches at the input during turn-on. When UVLO is cleared and EN_ is high, digital soft-start slowly ramps up the internal reference voltage in 64 steps. The total soft-start period is 4096 internal oscillator switching cycles.

Driving EN_ low initiates digital soft-stop that slowly ramps down the internal reference voltage in 64 steps. The total soft-stop period is equal to the soft-start period.

To calculate the soft-start/soft-stop period, use the following equation:

\[ t_{SS}(ms) = \frac{4096}{f_{OSC}(kHz)} \]

where fOSC is the internal oscillator and fOSC is twice each converter’s switching frequency (FSEL_1 = VL).
Enable (EN1, EN2)

The MAX5099 dual converter provides separate enable inputs, EN1 and EN2, to individually control or sequence the output voltages. These active-high enable inputs are TTL compatible. Driving EN_ high initiates soft-start of the converter, and PGOOD_ goes logic-high when the converter output voltage reaches the VTPGOOD_ threshold. Driving EN_ low initiates a soft-stop of the converter. Use EN1, EN2, and PGOOD1 for sequencing (see Figure 1). Connect PGOOD1 to EN2 to make sure converter 1’s output is within regulation before converter 2 starts. Add an RC network from VL to EN1 and EN2 to delay the individual converter. Sequencing reduces input inrush current and possible chattering. Connect EN_ to VL for always-on operation.

PGOOD

Converter 1 and converter 2 include power-good flags, PGOOD1 and PGOOD2, respectively. Since PGOOD_ is an open-drain output and can sink 3mA while providing the TTL logic-low signal, pull PGOOD_ to a logic voltage to provide a logic-level output. PGOOD1 goes low when converter 1’s feedback (FB_) drops to 92.5% (VTPGOOD_) of its nominal set point. The same is true for converter 2. Connect PGOOD_ to SGND or leave unconnected, if not used.

Current Limit

The internal high-side MOSFET switch current of each converter is monitored during its on-time. When the peak switch current crosses the current-limit threshold of 3.45A (typ) and 2.1A (typ) for converter 1 and converter 2, respectively, the on-cycle is terminated immediately and the inductor is allowed to discharge. The MOSFET switch is turned on at the next clock pulse initiating a new clock cycle.

In deep overload or short-circuit conditions when VFBI drops below 0.2V, the switching frequency is reduced to 1/4 x fSW to provide sufficient time for the inductor to discharge. During overload conditions, if the voltage across the inductor is not high enough to allow for the inductor current to properly discharge, current runaway may occur. Current runaway can destroy the device in spite of internal thermal-overload protection. Reducing the switching frequency during overload conditions prevents current runaway.

Output Overvoltage Protection

The MAX5099 outputs are protected from output voltage overshoots due to input transients and shorting the output to a high voltage. When the output voltage rises over the overvoltage threshold, 114% (typ) nominal FB, the overvoltage condition is triggered. When the overvoltage condition is triggered on either channel, both converters are immediately turned off, 20Ω pulldown switches from SOURCE_ to PGND are turned on to help the output-voltage discharge, and the gate of the load-dump protection external MOSFET is pulled low. The device restarts as soon as both converter outputs discharge, bringing both FB_ input voltages below 12.5% of their nominal set points.
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

**Thermal-Overload Protection**
During continuous short circuit or overload at the output, the power dissipation in the IC can exceed its limit. The MAX5099 provides thermal shutdown protection with temperature hysteresis. Internal thermal shutdown is provided to avoid irreversible damage to the device. When the die temperature exceeds +165°C (typ), an on-chip thermal sensor shuts down the device, forcing the internal switches to turn off, allowing the IC to cool. The thermal sensor turns the part on again with soft-start after the junction temperature cools by +20°C. During thermal shutdown, both regulators shut down, PGOOD_ goes low, and soft-start resets. The internal 20V zener clamp from IN_HIGH to SGND is not turned off during thermal shutdown because this clamping action must always be active.

**Applications Information**

**Setting the Switching Frequency**
The controller generates the clock signal by dividing down the internal oscillator fOSC or the SYNC input signal when driven by an external oscillator. The switching frequency equals half the internal oscillator frequency (fSW = fOSC/2). The internal oscillator frequency is set by a resistor (ROSC) connected from OSC to SGND. To find ROSC for each converter switching frequency fSW, use the formulas:

\[
ROSC (\text{k}\Omega) = \begin{cases} 
10.721 & \text{fSW} \geq 1.25\text{MHz} \\
12.184 & \text{fSW} < 1.25\text{MHz}
\end{cases}
\]

A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by ROSC. When an external synchronization signal is used, ROSC must be selected such that fSW = 1/2 fSYNC.

**Buck Converter**

**Effective Input Voltage Range**
Although the MAX5099 converter operates from input supplies ranging from 5.2V to 19V, the input voltage range can be effectively limited by the MAX5099 duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum on-time (tON(MIN)):

\[
V_{IN(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}
\]

where tON(MIN) is 100ns. The minimum input voltage is limited by the maximum duty cycle (D_{MAX} = 0.92):

\[
V_{IN(MIN)} = \left[ \frac{V_{OUT} + V_{DROP1}}{D_{MAX}} \right] + V_{DROP2} - V_{DROP1}
\]

where V_{DROP1} is the total parasitic voltage drops in the inductor discharge path, which includes the forward voltage drop (V_{DS}) of the low-side n-channel MOSFET, the series resistance of the inductor, and the PCB resistance. V_{DROP2} is the total resistance in the charging path that includes the on-resistance of the high-side switch, the series resistance of the inductor, and the PCB resistance.

**Setting the Output Voltage**
For 0.8V or greater output voltages, connect a voltage-divider from OUT_ to FB_ to SGND (Figure 2). Select RB (FB_ to SGND resistor) to between 1kΩ and 20kΩ. Calculate RA (OUT_ to FB_ resistor) with the following equation:

\[
R_A = R_B \left( \frac{V_{OUT}}{V_{FB_}} - 1 \right)
\]

where VFB_ = 0.8V (see the Electrical Characteristics table).

For output voltages below 0.8V, set the MAX5099 output voltage by connecting a voltage-divider from OUT_ to FB_ to BYPASS (Figure 2). Select RC (FB_ to BYPASS resistor) higher than a 50kΩ range. Calculate RA with the following equation:

\[
R_A = R_C \left( \frac{V_{FB_} - V_{OUT_}}{V_{BYPASS} - V_{FB_}} \right)
\]

where VFB_ = 0.8V, V_BYPASS = 2V (see the Electrical Characteristics table), and VOUT_ can range from 0V to VFB_.

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Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5099: inductance value (L), peak inductor current (IL), and inductor saturation current (ISAT). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔIL). A good compromise is to choose ΔIL equal to 30% of the full load current. To calculate the inductance, use the following equation:

\[
L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta L}
\]

where \(V_{IN}\) and \(V_{OUT}\) are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by ROSC (see the Setting the Switching Frequency section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worse at the maximum input voltage. See the Output Capacitor section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during output overload and continuous short circuit. Select the ISAT to be higher than the maximum peak current limits of 4.3A and 2.6A for converter 1 and converter 2.

Input Capacitor

The discontinuous input current waveform of the buck converter causes large ripple currents at the input. The switching frequency, peak inductor current, and allowable peak-to-peak voltage ripple dictate the input capacitance requirement. Note that the two converters of the MAX5099 run 180° out-of-phase, thereby effectively doubling the switching frequency at the input. The input ripple waveform would be unsymmetrical due to the difference in load current and duty cycle between converter 1 and converter 2. The worst-case mismatch is when one converter is at full load while the other is at no load or in shutdown. The input ripple is comprised of ΔVQ (caused by the capacitor discharge) and ΔVESR (caused by the ESR of the capacitor). Use ceramic capacitors with high ripple-current capability at the input connected between DRAIN_ and PGND. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

\[
ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta L}{2}}
\]

where

\[
\Delta L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}
\]

and

\[
C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_{Q} \times f_{SW}}
\]

where \(I_{OUT}\) is the maximum output current from either converter 1 or converter 2, and \(D\) is the duty cycle for that converter. \(f_{SW}\) is the frequency of each individual converter. For example, at \(V_{IN} = 12V, V_{OUT} = 3.3V\) at \(I_{OUT} = 2A\), and with \(L = 3.3\mu H\), the ESR and input capacitance are calculated for a peak-to-peak input ripple of 100mV or less, yielding an ESR and capacitance value of 20mΩ and 6.8μF for 1.25MHz frequency. At low input voltages, also add one electrolytic bulk capacitor of at least 100μF on the converters’ input voltage rail. This capacitor acts as an energy reservoir to avoid possible undershoot below the undervoltage-lockout threshold during power-on and transient loading.
Output Capacitor

The allowable output ripple voltage and the maximum deviation of the output voltage during step load currents determine the output capacitance and its ESR. The output ripple is comprised of $\Delta V_Q$ (caused by the capacitor discharge) and $\Delta V_{ESR}$ (caused by the ESR of the capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by $\Delta V_{ESR}$. Use the ESR output equation to calculate the ESR requirements and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge are equal. Calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where $I_{STEP}$ is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Boost Converter

The MAX5099 can be configured for step-up conversion since the internal MOSFET can be used as a low-side switch. Use the following equations to calculate the values for the inductor ($L_{MIN}$), input capacitor ($C_{IN}$), and output capacitor ($C_{OUT}$) when using the converter in boost operation.

Inductor

Choose the minimum inductor value so the converter remains in continuous mode operation at minimum output current ($I_{OMIN}$).

$$L_{MIN} = \frac{V_{IN}^2 \times D}{2 \times I_{SW} \times V_O \times I_{OMIN}}$$

where

$$D = \frac{V_O + V_D - V_{IN}}{V_O + V_D - V_{DS}}$$

$V_D$ is the forward voltage drop of the external Schottky diode, $D$ is the duty cycle, and $V_{DS}$ is the voltage drop across the internal MOSFET switch. Select the inductor with low DC resistance and with a saturation current ($I_{SAT}$) rating higher than the peak switch current limit of 4.3A ($I_{CL1}$) and 2.6A ($I_{CL2}$) of converter 1 and converter 2, respectively.

Input Capacitor

The input current for the boost converter is continuous, and the RMS ripple current at the input is low. Calculate the capacitor value and ESR of the input capacitor using the following equations:

$$C_{IN} = \frac{\Delta I_L}{8 \times I_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

where

\[ \Delta L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{SW}} \]

where \( V_{DS} \) is the voltage drop across the internal MOSFET switch. \( \Delta L \) is the peak-to-peak inductor ripple current as calculated above. \( \Delta V_Q \) is the portion of input ripple due to the capacitor discharge, and \( \Delta V_{ESR} \) is the contribution due to ESR of the capacitor.

**Output Capacitor**

For the boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to the ESR while supporting the load current. Use the following equation to calculate the output capacitor for a specified output ripple tolerance:

\[ ESR = \frac{\Delta V_{ESR}}{I_{PK}} \]

\[ C_{OUT} = \frac{I_O \times D_{MAX}}{\Delta V_Q \times f_{SW}} \]

where \( I_{PK} \) is the peak inductor current as defined in the following Power Dissipation section, \( I_O \) is the load current, \( \Delta V_Q \) is the portion of the ripple due to the capacitor discharge, and \( \Delta V_{ESR} \) is the contribution due to the ESR of the capacitor. \( D_{MAX} \) is the maximum duty cycle at minimum input voltage.

**Power Dissipation**

The MAX5099 includes two internal power MOSFET switches. The DC loss is a function of the RMS current in the switch while the switching loss is a function of switching frequency and instantaneous switch voltage and current. Use the following equations to calculate the RMS current, DC loss, and switching loss of each converter. The MAX5099 is available in a thermally enhanced package and can dissipate up to 2.7W at +70°C ambient temperature. The total power dissipation in the package must be limited so that the operating junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature.

For the buck converter:

\[ I_{RMS} = \sqrt{(I_{DC}^2 + I_{PK}^2 + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}} \]

\[ P_{DC} = I_{RMS}^2 \times R_{ON(MAX)} \]

where \( V_{DS} \) is the drop across the internal MOSFET and \( \eta \) is the efficiency. See the Electrical Characteristics table for the \( R_{ON(MAX)} \) value.

For the boost converter:

\[ I_{RMS} = \sqrt{(I_{DC}^2 + I_{PK}^2 + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}} \]

\[ I_{PK} = I_O + \frac{\Delta L}{2} \]

\[ P_{SW} = \frac{V_{IN} \times I_O \times (I_R + I_F) \times f_{SW}}{4} \]

where \( t_R \) and \( t_F \) are rise and fall times of the internal MOSFET. The \( t_R \) and \( t_F \) can be measured in the actual application.

The supply current in the MAX5099 is dependent on the switching frequency. See the Typical Operating Characteristics to find the supply current of the MAX5099 at a given operating frequency. The power dissipation (\( P_S \)) in the device due to supply current (\( I_{SUPPLY} \)) is calculated using following equation:

\[ P_S = V_{IN \times MAX} \times I_{SUPPLY} \]

The total power dissipation \( P_T \) in the device is:

\[ P_T = P_{DC1} + P_{DC2} + P_{SW1} + P_{SW2} + P_S \]

where \( P_{DC1} \) and \( P_{DC2} \) are DC losses in converter 1 and converter 2, respectively. \( P_{SW1} \) and \( P_{SW2} \) are switching losses in converter 1 and converter 2, respectively.
Calculate the temperature rise of the die using the following equation:

\[ T_J = T_C \times (P_T \times \theta_{JC}) \]

where \( \theta_{JC} \) is the junction-to-case thermal impedance of the package equal to +1.7°C/W. Solder the exposed pad of the package to a large copper area to minimize the case-to-ambient thermal impedance. Measure the temperature of the copper area near the device at a worst-case condition of power dissipation, and use +1.7°C/W as \( \theta_{JC} \) thermal impedance.

**Compensation**

The MAX5099 provides an internal transconductance amplifier with its inverting input and its output available for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use high-ESR aluminum electrolytic capacitors; for component size-sensitive applications, use low-ESR tantalum, polymer, or ceramic capacitors at the output. The high switching frequency of the MAX5099 allows the use of ceramic capacitors at the output.

Choose all the passive power components that meet the output ripple, component size, and component cost requirements. Choose the small-signal components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin. Use a simple pole-zero pair (Type II) compensation if the output capacitor ESR zero frequency is below the unity-gain crossover frequency \( f_C \). Type III compensation is necessary when the ESR zero frequency is higher than \( f_C \) or when compensating for a continuous-mode boost converter that has a right-half-plane zero.

Use procedure 1 to calculate the compensation network components when \( f_{\text{ZERO,ESR}} < f_C \).

**Buck Converter Compensation**

**Procedure 1 (See Figure 3)**

1) Calculate the \( f_{\text{ZERO,ESR}} \) and \( f_C \) double-pole frequencies:

\[ f_{\text{ZERO,ESR}} = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \]
\[ f_C = \frac{1}{2\pi \sqrt{L_{\text{OUT}} \times C_{\text{OUT}}}} \]

2) Select the unity-gain crossover frequency:

\[ f_C = \frac{f_{\text{SW}}}{20} \]

If the \( f_{\text{ZERO,ESR}} \) is lower than \( f_C \) and close to \( f_C \), use a Type II compensation network where \( R_{\text{CCF}} \) provides a midband zero, \( f_{\text{MID,ZERO}} \), and \( R_{\text{FCF}} \) provides a high-frequency pole.

3) Calculate modulator gain \( G_M \) at the crossover frequency.

\[ G_M = \frac{V_{IN}}{V_{OSC}} \times \frac{\text{ESR} \times 0.8}{(2\pi \times f_C \times L_{\text{OUT}}) \times \frac{V_{OUT}}{V_{OSC}}} \]

where \( V_{OSC} \) is a peak-to-peak ramp amplitude equal to 1V.

The transconductance error-amplifier gain is:

\[ G_{E/A} = g_M \times R_F \]

The total loop gain at \( f_C \) should be equal to 1:

\[ G_M \times G_{E/A} = 1 \]

or

\[ R_F = \frac{V_{OSC} \times (\text{ESR} + 2\pi \times f_C \times L_{\text{OUT}}) \times V_{OUT}}{0.8 \times V_{IN} \times g_M \times \text{ESR}} \]

4) Place a zero at or below the \( f_C \) double-pole:

\[ C_F = \frac{1}{2\pi \times R_{\text{CCF}} \times f_C} \]

5) Place a high-frequency pole at \( f_p = 0.5 \times f_{\text{SW}} \).

\[ C_{\text{CCF}} = \frac{C_F}{(2\pi \times 0.5f_{\text{SW}} \times R_F \times C_F) - 1} \]

**Figure 3. Type II Compensation Network**
Procedure 2 (See Figure 4)

If the output capacitor used is a low-ESR ceramic type, the ESR frequency is usually far away from the targeted unity crossover frequency \( f_C \). In this case, Type III compensation is recommended. Type III compensation provides two-pole zero pairs. The locations of the zero and poles should be such that the phase margin peaks around \( f_C \). It is also important to place the two zeros at or below the double pole to avoid the conditional stability issue.

1) Select a crossover frequency:
\[
f_{SW} = \frac{f_{SW}}{20}
\]

2) Calculate the LC double-pole frequency, \( f_{LC} \):
\[
f_{LC} = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}
\]

3) Place a zero \( f_{Z1} = \frac{1}{2\pi R_F \times C_F} \) at \( 0.75 \times f_{LC} \).

where
\[
C_F = \frac{1}{2\pi \times 0.75 \times f_{LC} \times R_F}
\]

and \( R_F \geq 10k\Omega \).

4) Calculate \( C_I \) for a target unity crossover frequency, \( f_C \).

\[
C_I = \frac{2\pi \times f_C \times L_{OUT} \times C_{OUT} \times V_{OSC}}{V_{IN} \times R_F}
\]

5) Place a pole \( f_{P1} = \frac{1}{2\pi \times R_I \times C_I} \) at \( f_{ZERO,ESR} \).

\[
R_I = \frac{1}{2\pi f_{ZERO,ESR} \times C_I}
\]

6) Place a second zero, \( f_{Z2} \), at \( 0.2 \times f_C \) or at \( f_{LC} \), whichever is lower.

\[
R_1 = \frac{1}{2\pi f_{Z2} \times C_I} - R_I
\]

7) Place a second pole at \( 1/2 \) the switching frequency.

\[
C_{CF} = \frac{C_F}{\left(2\pi \times 0.5 \times f_{SW} \times R_F \times C_F \right) - 1}
\]

Boost Converter Compensation

The boost converter compensation gets complicated due to the presence of a right-half-plane zero \( f_{ZERO,RHP} \). The right-half-plane zero causes a drop in phase while adding positive (+1) slope to the gain curve. It is important to drop the gain significantly below unity before the RHP frequency. Use the following procedure to calculate the compensation components:

1) Calculate the LC double-pole frequency, \( f_{LC} \), and the right-half-plane-zero frequency.

\[
f_{LC} = \frac{1-D}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}
\]

\[
f_{ZERO,RHP} = \frac{(1-D)^2 R_{(MIN)}}{2\pi \times L_{OUT}}
\]

where

\[
D = 1 - \frac{V_{IN}}{V_{OUT}} \quad \frac{V_{OUT}}{V_{OUBT}(MAX)}
\]

Target the unity-gain crossover frequency for:

\[
f_C = \frac{f_{ZERO,RHP}}{5}
\]
Choose a suitable power MOSFET that can safely operate in the saturation region. Verify its capability to support the downstream DC-DC converters’ input current during the load-dump event by checking its safe operating area (SOA) characteristics. Since the transient peak power dissipation on the MOSFET can be very high during the load-dump event, also refer to the thermal impedance graph given in the data sheet of the power MOSFET to make sure its transient power dissipation is kept within the recommended limits.

**Improving Noise Immunity**
In applications where the MAX5099 is subject to noisy environments, adjust the controller’s compensation to improve the system’s noise immunity. In particular, high-frequency noise coupled into the feedback loop causes jittery duty cycles. One solution is to lower the crossover frequency (see the Compensation section).
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters where one channel can affect the other. Refer to the MAX5098A/MAX5099 Evaluation Kit data sheet for a specific layout example. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PCB layout:

1) For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose this copper area on the top and bottom side of the PCB. Do not make a direct connection from the exposed pad copper plane to SGND underneath the IC.

2) Isolate the power components and high-current path from the sensitive analog circuitry.

3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.

4) Connect SGND and PGND together at a single point. Do not connect them together anywhere else (refer to the MAX5099 Evaluation Kit data sheet for more information).

5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.

6) Ensure that the feedback connection to COUT is short and direct.

7) Route high-speed switching nodes (BST_/VDD_, SOURCE_) away from the sensitive analog areas (BYPASS, COMP_, and FB_). Use the internal PCB layer for SGND as an EMI shield to keep radiated noise away from the IC, feedback dividers, and analog bypass capacitors.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (inductor, CIN_, and COUT_). Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).

2) Group the gate-drive components (bootstrap diodes and capacitors, and ViL bypass capacitor) together near the controller IC.

3) Make the DC-DC controller ground connections as follows:
   a) Create a signal ground plane underneath the IC.
   b) Connect this plane to SGND and use this plane for the ground connection for the reference (BYPASS), enable, compensation components, feedback dividers, and OSC resistor.
   c) Connect SGND and PGND together (this is the only connection between SGND and PGND). Refer to the MAX5098A/MAX5099 Evaluation Kit data sheet for more information.
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Figure 6. 4.5V to 5.5V Operation
Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection

Typical Application Circuit
**Dual, 2.2MHz, Automotive Synchronous Buck Converter with 80V Load-Dump Protection**

**Pin Configuration**

**Chip Information**

**PROCESS:** BiCMOS

**Package Information**

For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

<table>
<thead>
<tr>
<th>PACKAGE TYPE</th>
<th>PACKAGE CODE</th>
<th>DOCUMENT NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 TQFN</td>
<td>T3255+4</td>
<td>21-0140</td>
</tr>
</tbody>
</table>