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## MAX25608

# Twelve Switch High Brightness LED Matrix Manager for Automotive Front Lights

### General Description

The MAX25608 12-switch matrix manager IC for automotive lighting applications includes a 12-switch array for bypassing individual LEDs in a single or dual string application. It features twelve individually controlled n-channel MOSFET switches rated for 14V with an on-resistance of 0.06Ω. A single current source can be used to power all the LEDs connected in series. Individual LEDs can be dimmed by turning on and off the bypass switches across each LED. The device can also be configured in two string applications with six switches in series per string. Each switch can be connected across one, two, or three LEDs in series. It also allows for parallel connection of two switches to bypass high-current LEDs. The IC also includes an internal charge pump that provides power for the gate drive for the LED bypass switches.

The MAX25608 features a serial peripheral interface (UART) for serial communication. Each switch can be turned fully on, fully off, or dimmed with or without fade transitions through the serial interface. The IC features open-LED protection as well as open and short LED fault reporting through the serial interface. The device is available in a 28-pin TSSOP package with exposed pad.

### Applications

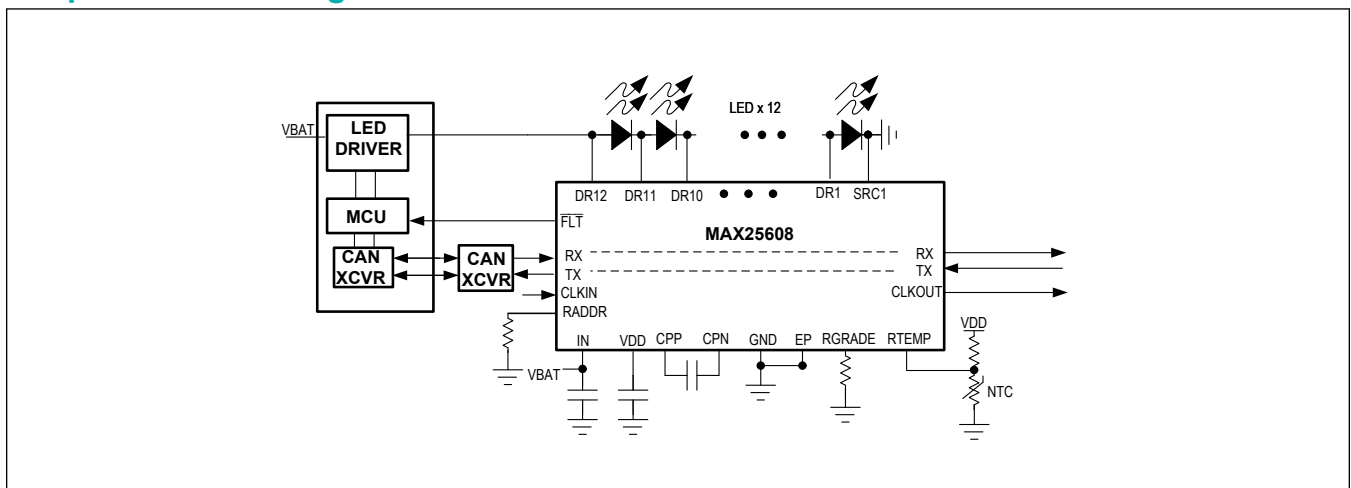
Automotive Matrix LED Systems and Adaptive Drive Beam Lights.

### Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Flexible Configuration
  - Up to Twelve Switches in Series for Single String
  - Two Sub Strings of Six Series Switches per String
- Robust Serial Interface
  - Multi-Drop UART Communication Interface
  - Up to 16 Addressable Devices
  - Compatible with CAN Physical Layer
- Optimal PWM Dimming Arrangement Provides Excellent Dimming Performance
  - Programmable 12-Bit PWM Dimming
  - Fade Transition Between PWM Dimming States
  - Internal or External Clock for PWM Dimming
  - Programmable Slew Rate for EMI Control
- Protection Features and Package Improve Reliability
  - Open-LED Protection
  - NTC Temperature Monitor
  - Programmable Open and Short-LED Threshold
  - Open and Shorted-LED Fault Reporting
  - Thermally Enhanced 28-Pin TSSOP-EP

[Ordering Information](#) appears at end of data sheet.

### Simplified Block Diagram



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## Absolute Maximum Ratings

IN to GND .....	-0.3V to +65V	RTEMP, RGRADE, CLKIN, CLKOUT, RADDR to GND ..	-0.3V to $V_{VDD} + 0.3V$
VDD to GND .....	-0.3V to +2.5V	RX, TX, $\overline{FLT}$ to GND .....	-0.3V to +6V
CPN to GND .....	-0.3V to +65V	Continuous Power Dissipation (multilayer board) ( $T_A = 70^\circ C$ , derate 40.57mW/ $^\circ C$ above $+70^\circ C$ ) .....	3245.44mW
CPP to GND .....	-0.3V to +70V	Operating Temperature Range .....	$-40^\circ C$ to $+125^\circ C$
CPP to CPN .....	-0.3V to +6V	Junction Temperature .....	$+150^\circ C$
CPP to DRx .....	-0.3V to +70V	Storage Temperature Range .....	$-40^\circ C$ to $+150^\circ C$
DR12 to GND .....	-0.3V to +65V	Soldering Temperature (reflow) .....	$+260^\circ C$
DRx to DR(x-1) .....	-0.3V to +16V		
DR6 to GND .....	-0.3V to +65V		
SRCx to GND .....	-0.3V to +65V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 28-TSSOP

Package Code	U28E+6C
Outline Number	<a href="#">21-0108</a>
Land Pattern Number	90-100175
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	24.6 $^\circ C/W$
Junction to Case ( $\theta_{JC}$ )	1.5 $^\circ C/W$

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{IN} = 5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Voltages</b>						
Supply Voltage	$V_{IN}$	Operating Voltage Range	4.0		60	V
Input Current	$I_{IN}$	$V_{IN} = 5V$		4.2	6	mA
Input POR Threshold	$V_{IN-POR}$	$V_{IN}$ Rising	3.6		3.9	V
Charge Pump DRAINn Input Current	$I_{INQP}$				6	mA
Charge-Pump Operating Voltage	$V_{CPP}$				65	V
VDD_UVLO Rising Threshold	UVLO_R_TH		1.61		1.69	V
VDD UVLO Falling Threshold	UVLO_F_TH		1.54		1.63	V
<b>LED Dimming</b>						
Internal Oscillator Frequency	$F_{OSC}$	Used for charge pump and PWM dimming of LEDs		16.384		MHz
LED PWM Dimming Frequency Range	$f_{DIM}$		100		2000	Hz
<b>LED Switches</b>						
Single Switch On Resistance	$R_{DSON}$			0.060		$\Omega$
On Resistance with series switches 6-1 on				0.36	0.75	$\Omega$
On Resistance with series switches 12-7 on				0.36	0.75	$\Omega$
Open LED Threshold (Rising)	VOTH	VOTH code = 0x0	12.0	14.0	15.0	V
		VOTH code = 0x1	8.3	9.33	10.0	
		VOTH code = 0x2	4.0	4.66	5.1	
Short LED Threshold (Rising)	VSTH	VSTH code = 000	1.26	1.40	1.54	V
		VSTH code = 001	3.24	3.6	3.96	
		VSTH code = 010	3.6	4.00	4.4	
		VSTH code = 011	4.95	5.5	6.05	
		VSTH code = 100	5.4	6.0	6.6	
		VSTH code = 101	5.94	6.6	7.26	
		VSTH code = 110	6.48	7.2	7.92	
		VSTH code = 111	6.93	7.70	8.47	
Maximum Switch Current	$I_{SW}$	Thermally Limited		1.6		A
LED Slew-Rate Setting 0	SR_LED_0	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x0		160		$\mu s$
LED Slew-Rate Setting 1	SR_LED_1	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x1		81		$\mu s$

**Electrical Characteristics (continued)**

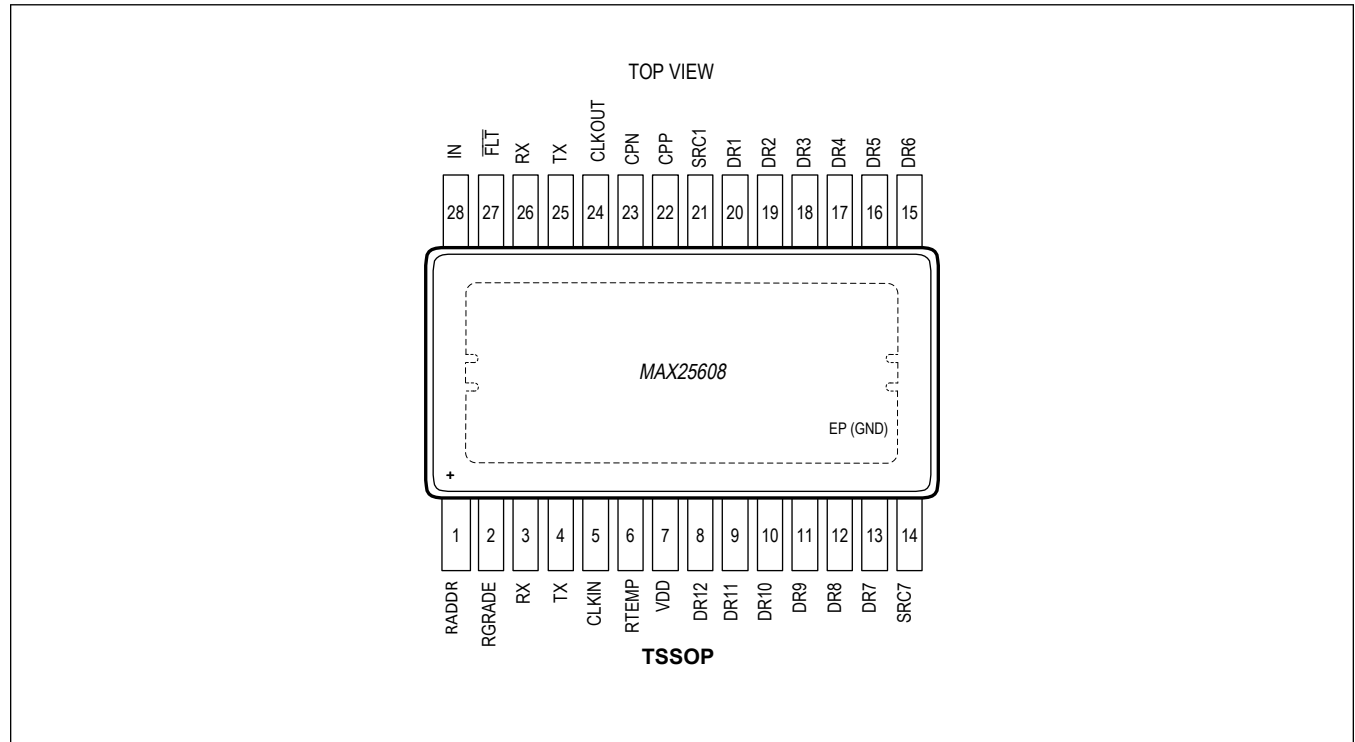
( $V_{IN} = 5V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Slew-Rate Setting 2	SR_LED_2	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x2		48		$\mu s$
LED Slew-Rate Setting 3	SR_LED_3	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x3		26		$\mu s$
LED Slew-Rate Setting 4	SR_LED_4	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x4		17		$\mu s$
LED Slew-Rate Setting 5	SR_LED_5	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x5		10		$\mu s$
LED Slew-Rate Setting 6	SR_LED_6	0–6V step, 10–90% rise/fall time, LED_SLEW[2:0] = 0x6		5.0		$\mu s$
<b>DIGITAL INPUTS - CLKIN, RX</b>						
Input High Voltage	$V_{IH}$		1.4			V
Input Low Voltage	$V_{IL}$				0.4	V
CLKIN Input Frequency	$f_{CLK}$		0.30		20.0	MHz
<b>DIGITAL OUTPUTS - TX, FLT, CLKOUT</b>						
Output Low Voltage	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
CLKOUT High Voltage	$V_{OH}$	$I_{SRC} = 2mA$	$V_{DD} - 0.4$			V
<b>THERMAL SHUTDOWN</b>						
Thermal-Warning Threshold	TH_WARN	Rising temperature		140		$^{\circ}C$
Thermal Warning Hysteresis				15		$^{\circ}C$
Thermal Shutdown	TH_SHDN	Rising temperature		165		$^{\circ}C$
Thermal-Shutdown Hysteresis	HYS_SHDN			15		$^{\circ}C$
<b>CHARGE PUMP</b>						
Charge-Pump Frequency	$f_{CPP}$			16.384		MHz
Charge-Pump Output Voltage	$V_o$	$V_{CPP} - V_{CPN}$ , $I_{CPP} = 350\mu A$	3.7		6.0	V
Charge-Pump Power-Good Threshold	$V_{CPP\_OK}$	Rising threshold		4.0		V
<b>UART Timing</b>						
UART Bit Rate	$F_{UART}$	-40 $^{\circ}C$ to 125 $^{\circ}C$ junction temperature	10		950	kbps
		0 $^{\circ}C$ to 125 $^{\circ}C$ junction temperature	10		1000	



Pin Configuration

MAX25608



## Pin Description

PIN	NAME	FUNCTION
1	RADDR	Device ID Resistor. Connect a resistor value from RADDR to GND to set the UART Device ID.
2	RGRADE	LED Binning Resistor Connection. Connect a LED binning resistor from this pin to GND.
3 , 26	RX	UART Receive Input.
4 , 25	TX	UART Transmit Output.
5	CLKIN	CLK Input. Can be optionally used to sync the MAX25608 with an external digital clock signal.
6	RTEMP	NTC Divider ADC Input. Connect to NTC resistor divider to enable remote temperature sensing.
7	VDD	LDO Output. Nominal voltage is 1.8V. Connect a bypass capacitor between VDD and GND
8	DR12	Drain of Internal Switch 12. Add a 0.1 $\mu$ F capacitor from DR12 to GND.
9	DR11	Drain of Internal Switch 11.
10	DR10	Drain of Internal Switch 10.
11	DR9	Drain of Internal Switch 9.
12	DR8	Drain of Internal Switch 8.
13	DR7	Drain of Internal Switch 7.
14	SRC7	Source of Internal Switch 7.
15	DR6	Drain of Internal Switch 6. For two string applications, connect a 0.1 $\mu$ F ceramic capacitor from DR6 to GND.
16	DR5	Drain of Internal Switch 5.
17	DR4	Drain of Internal Switch 4.
18	DR3	Drain of Internal Switch 3.
19	DR2	Drain of Internal Switch 2.
20	DR1	Drain of Internal Switch 1.
21	SRC1	Source of Internal Switch 1.
22	CPP	Charge Pump Capacitor Positive Connection. Connect a 0.1 $\mu$ F ceramic capacitor from CPP to CPN.
23	CPN	Charge Pump Capacitor Negative Connection. Connect a 0.1 $\mu$ F from CPP to CPN.
24	CLKOUT	After startup, can be optionally configured with UART to drive a clock signal to other devices, or act as a pass-through for the CLKIN input.
27	$\overline{\text{FLT}}$	Open Drain Fault Indicator. Goes low when a fault condition is present.
28	IN	Connect external bypass capacitor to GND.
-	EP/GND	Exposed Pad Ground Connection. Connect this pad to a contiguous ground plane.

## Detailed Description

### Power-On Reset and VDD UVLO

Once the IC is powered, an internal power-on reset (POR) signal sets all the registers to their default states. All twelve switches are in the on state upon a POR (all LEDs are off). The LEDs remain off until a command is received by the UART. To ensure reliable operation, the IN supply voltage ( $V_{IN}$ ) must be greater than  $V_{IN-POR}$ . If  $V_{IN}$  falls below  $V_{IN-POR}$  and the VDD regulator output falls below  $V_{DD\_UVLO}$ , the registers reset to their default state. The IN voltage must be greater than  $V_{IN-POR}$  and VDD must be above  $V_{DD\_UVLO}$  for proper operation. The bypass switches remain in their default on state until the UART is used to enable LED dimming.

### Internal Switches

Each switch connected between DRAIN $_n$  and DRAIN $_{n-1}$  has a typical on-resistance of 0.06 $\Omega$ . This measurement includes the on-resistance of the internal switch and the resistance of the bond wires to the DRAIN $_n$  and DRAIN $_{n-1}$  pads. Each bypass switch, when driven to an off state, allows the string current to flow through the corresponding parallel-connected LED, turning the LEDs on. Driving the bypass switch to an on state shunts the current through the bypass switch and turns the LEDs off. Each bypass switch can have one, two, or three LEDs in series across it.

## Programming Options

### MAX25608 Pin Resistor Decode Table

Multiple MAX25608 devices can be used in a multi-drop UART bus with an external  $\mu$ C acting as the master. The resistor on RADDR is used to program the UART Device ID of the MAX25608. For example, a resistor of 3.74k $\Omega$  sets the device ID to 0. A resistor of 115k $\Omega$  sets the device ID to 0xF.

**Table 1. Device ID Table**

DECODED VALUE OF RADDR RESISTOR	DEVICE ID
0x0	0x0
0x1	0x1
...	...
0xF	0xF

### Resistor Programming Table

A resistor connected between pins RADDR and GND is used to configure the MAX25608 device ID, and the resistor connected between pins RGRADE and GND is used for LED binning. The IC provides 16 levels of detection between 0V and 1.2V on RADDR/RGRADE pins. The pins source 400 $\mu$ A, allowing the use of an external resistor between RADDR/RGRADE and GND to set the voltage level. See [Table 1](#) for recommended resistor values.

**Table 2. RADDR/RGRADE Recommended Values**

RGRADE/RADDR[3:0] DECODE VALUE	RGRADE/RADDR RESISTOR VALUE ( $\Omega$ , 1%)
0000	95
0001	200
0010	309
0011	422
0100	536
0101	649
0110	768
0111	909
1000	1050

**Table 2. RADDR/RGRADE Recommended Values (continued)**

1001	1210
1010	1400
1011	1620
1100	1870
1101	2150
1110	2490
1111	2870

**PWM Dimming**

The IC provides 12-bit programmable dimming on each individual switch. An internal 12-bit counter (COUNT) is generated according to the clock settings. The switch turns off when COUNT is equal to the delay set by the corresponding PSFT register and stays off until the COUNT exceeds the sum of PSFT and PWM duty-control registers. In this way, the duty cycle and relative phase shift of the individual switches can be set independently (see [Figure 1](#)).

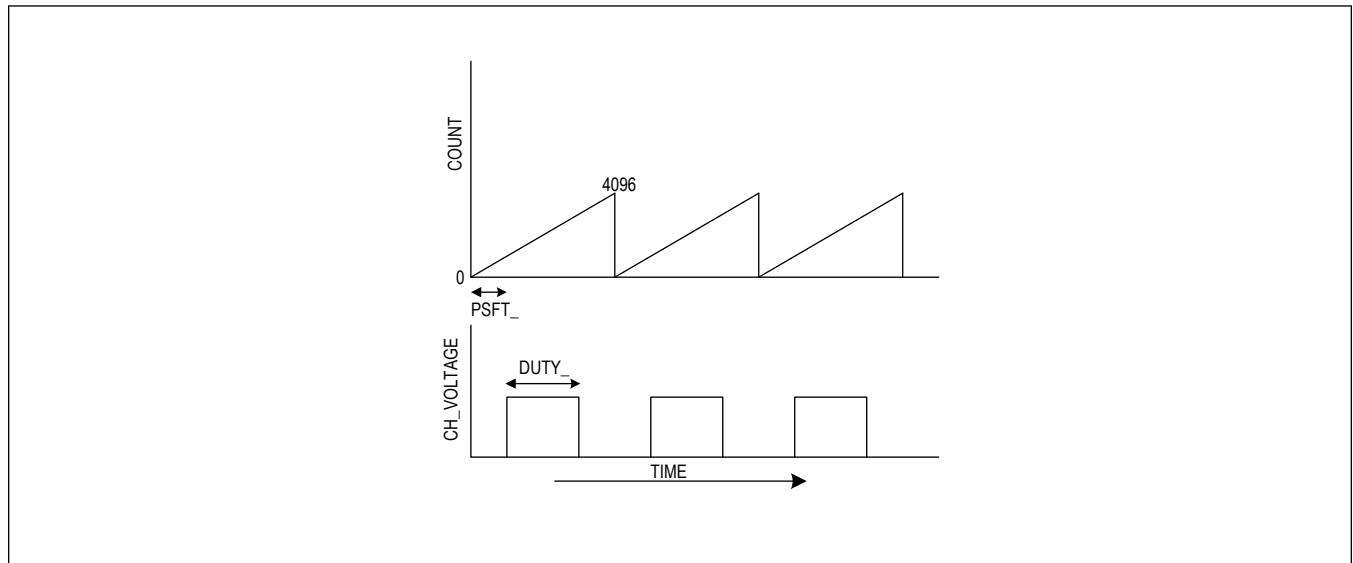


Figure 1. PWM Dimming

### PWM Clock and Synchronous Operation with Multiple Devices

The PWM clock for the IC can be selected from the internal oscillator or from an external clock source driving the CLKIN pin. The CLKOUT pin can be configured to pass either the CLKIN or the internal oscillator as an output to other devices. In this manner, a single clock signal can be used to synchronize all devices. The PWM clock source and CLKIN/CLKOUT function are configured through PWM\_CLK[1:0] in the CNFG\_GEN (0x03) register. The default value is from the internal oscillator with the CLKIN and CLKOUT disabled.

PWM dimming frequency is programmable by setting the value of the DIV[1:0] bits in the CNFG\_GEN (0x03) register, which sets the divide ratio for both the internal (8.192MHz) and external clock sources. When disabled, the CLK pin is high impedance with a 100kΩ pulldown resistor.

Synchronized operation with multiple devices is achieved through the following steps:

1. Set the SW\_GO\_EN bit to be 0.
2. Select the master device based on the resistor on RADDR pin and set the PWM\_CLK[1:0] bits in the CNFG\_GEN (0x03) register to use the internal oscillator and CLKOUT active.
3. Select the slave devices individually based on the resistor on RADDR pin and set the PWM\_CLK[1:0] bits in the CNFG\_GEN (0x03) register to keep the CLKIN and CLKOUT active.
4. Use the Global write command to set the SW\_GO\_EN bit to 1. All the PWM clocks of the devices will be synchronized now.

### Dimming With and Without Fade

Each switch of the IC can be independently programmed to perform dimming without fade transition or dimming with fade transition. For dimming without fade transition, the dimming changes from the initial value to the target value in one dimming cycle. For dimming with fade transition, the dimming changes transitionally step by step, starting from the initial value to the target value in multiple dimming cycles, following a predetermined exponential curve.

To enable dimming with fade transition, set the FADE bit to 1 and the DUTY bits to the target value for the specific switches. Each transitional step value is calculated using 12 bits according to the following formula:

$$\text{DUTY}_{\text{next}} = \text{DUTY}_{\text{now}} \times \text{CF}$$

where DUTY is the duty cycle, and CF the constant factor.

CF = 1.0625 and CF = 0.9375 for an up transition and down transition, respectively.

DUTY<sub>next</sub> continues to be updated according to the formula until DUTY<sub>next</sub> reaches the target value.

The transition period is defined by the TDIM\_ register for the switch. The number of transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 1/(8,191) to 8,191/(8,191) is 115 steps. See [Figure 2](#) for the up-transition curve.

The number of transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 8,191/(8,191) to 1/(8,191) is 111 steps. See [Figure 3](#) for the down-transition curve.

Duty-cycle steps smaller than CF update in one step.

Each step runs TDIM\_ PWM dimming cycles, and each dimming cycle consists of 8,192 clock cycles by default, therefore  $T_{\text{step}} = \text{TDIM\_} \times 8,192$ . The 8,192 clock cycles timer can also be changed to 16,384, 32,768, or 65,536 clock cycles by programming bits [3:2] in register address 0x02.

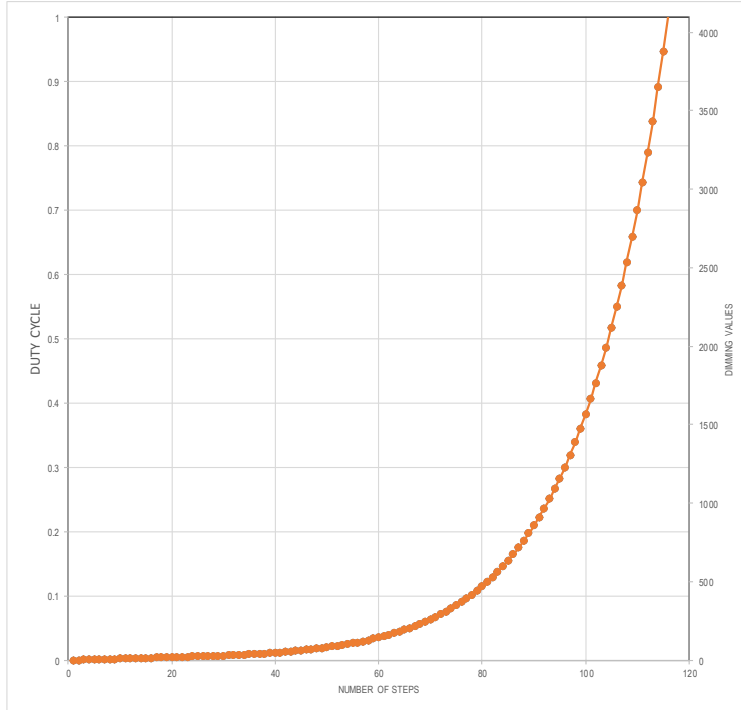


Figure 2. Up-Transition Curve

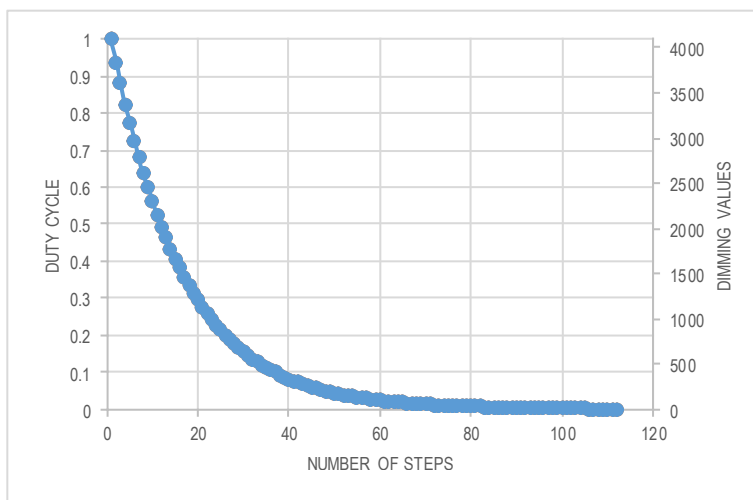


Figure 3. Down-Transition Curve

## RTEMP

The RTEMP pin is an auxiliary 8-bit ADC input that is suitable for use with an external NTC resistive divider for monitoring external temperature. In this way, a remote NTC resistor can be used to monitor the external LED temperature for current derating and system monitoring. The 8-bit code is updated with a period of 200 microseconds and can be read back using the UART RTEMP register (0x15).

## Fault Pin Behaviour

The  $\overline{\text{FLT}}$  pin will assert whenever one or more of these conditions is present:

- One or more floating domain gate drivers have detected an Open LED fault; in this case, the switch(es) with Open LED faults remain closed until the power is reset
- One or more floating domain gate drivers have detected a Short LED fault condition
- Thermal warning/shutdown

## LED Fault Detection and Protection

The IC is able to detect a shorted LED, open LED, and open trace between the device and the LED. To detect and report a LED fault, several conditions must be met. First, the LED switch must be operating, then the duty cycle must be greater than zero since both LED-open and LED-short detection require the switch to be open. Conversely, open-fault detection requires the switch to be closed, so PWM duty cycle must be less than 100%. In general, it takes up to one dimming cycle to make sure these conditions have been met after a fault condition is applied. This period depends on the PWM dimming frequency.

## LED Open-Fault Detection and Protection

An open-LED fault is triggered when the voltage between the individual LED switch DRAIN node and switch SOURCE node exceeds  $V_{\text{OTH}}$  and is reported in register OPEN\_LED\_STAT (0x13). The switch is closed when an open-LED is detected and remains closed until the next PWM dimming open-switch request occurs. By default, the open fault results in the  $\overline{\text{FLT}}$  pin being driven low; however, open faults can be masked by writing 0b1 to the MSK\_OPEN\_LED bit in the CNFG\_MSK (0x0C) register. If an open-LED fault is detected multiple times, it is recommended that the OPEN\_LED\_OVRD (0x09) register be updated to force the corresponding LED switch to remain closed continuously to provide a bypass for the faulty LED.

## LED Short Detection

A short-LED fault is triggered when the voltage between the switch DRAIN node and the switch SOURCE node is below  $V_{\text{STH}}$  for an open switch condition, and is reported in the SHRT\_LED\_STAT (0x12) register. The LED short comparator is sampled at the end of each LED pulse to avoid false detections during the beginning of the pulse. No action is taken with the switch in response to detecting a short-LED fault, thus continuing to operate as programmed. The short fault, by default, results in  $\overline{\text{FLT}}$  being driven low; however, short faults can be masked by writing 0b1 to MSK\_SHRT\_LED in the CFG\_MSK (0x0C) register.

The Low Duty Threshold Register (0x16) is used to filter out LED fault signals during short duty cycles when the voltage across the switch might not settle to a final value, causing an invalid detection of the Short LED condition. When the DUTY register of a switch is less than LOW\_DUTY\_TH, the SHORT\_LED signal is masked and SHORT\_LED\_STAT is not asserted for that switch.

## Thermal Shutdown

The IC features an on-chip temperature-protection circuit to prevent the device from overheating.

When the die temperature rises above the thermal-warning threshold (+140°C), the TH\_WARN bit is set, causing the FLT pin to be asserted but no action taken with the switches. If asserted, the FLT pin remains asserted until the die temperature drops below the thermal-warning threshold, and the TH\_WARN register bit is cleared by writing a 1. To clear the TH\_WARN bit, the die temperature must be below the thermal-warning threshold.

When the die temperature rises above the thermal-shutdown threshold (+160°C), the TH\_SHDN bit is set, causing the FLT pin to be asserted and all switches to either be closed (LEDs turned off) or opened (LEDs turned on), depending on the value of the CNFG\_MSK\_GEN (0x0C) register. Switches remain static, and the FLT pin remains asserted until the die temperature drops below the thermal-warning threshold, and both the TH\_WARN and TH\_SHDN bits are cleared in the STAT\_GEN (x10) register by writing 1 to both bits.

When the device recovers from thermal shutdown, it resumes operation from where it was before the thermal shutdown. The TH\_WARN and TH\_SHDN status bits are cleared on write.

## UART Serial Interface

### Overview

The MAX25608 includes a full-duplex UART serial interface to enable fully programmable matrix manager functionality. The system ECU/MCU acts as the UART master, driving read/write packets on the RX line and receiving packets on the TX line. The RX and TX lines can connect up to 16 MAX25608 devices on a common bus using a star topology. The device address of each MAX25608 is pin-programmable using an external resistor to ground on the RADDR pin. Devices can be addressed individually using their Device ID[3:0]. They can also be simultaneously addressed using the General Call ID or by using the programmable Cluster Call ID value.

The baud rate of incoming UART packets on RX is automatically detected by the MAX25608, from a minimum of 10kbps up to a maximum of 1,000kbps. The MAX25608 then returns frames on the TX line at the same baud rate, according to the packet format described in the [UART Frame Format](#) section.

### Device Connections

The UART interface ensures compatibility with standard microcontrollers from a variety of manufacturers. It also enables the use of CAN transceivers for applications where the matrix manager is remote from the microcontroller. The RX line should be driven by the microcontroller master. It can be connected to an individual MAX25608 or to multiple devices in a star topology. The TX line is an open-drain output. Multiple devices can share the same TX connection as well. No external timing reference is required, the MAX25608 automatically detects the bit rate on each RX packet and adjusts the bit rate of the TX response accordingly.

### UART Frame Format

Read/write packets are composed from multiple UART frames. Each frame consists of one start bit, eight data bits, one parity bit (even) and one stop bit. The parity bit shall be high if the number of ones in the data bits is odd, otherwise it will be low. If the next frame is in the same packet, there can be no more than 12-bit periods of idle (high) state between frames.



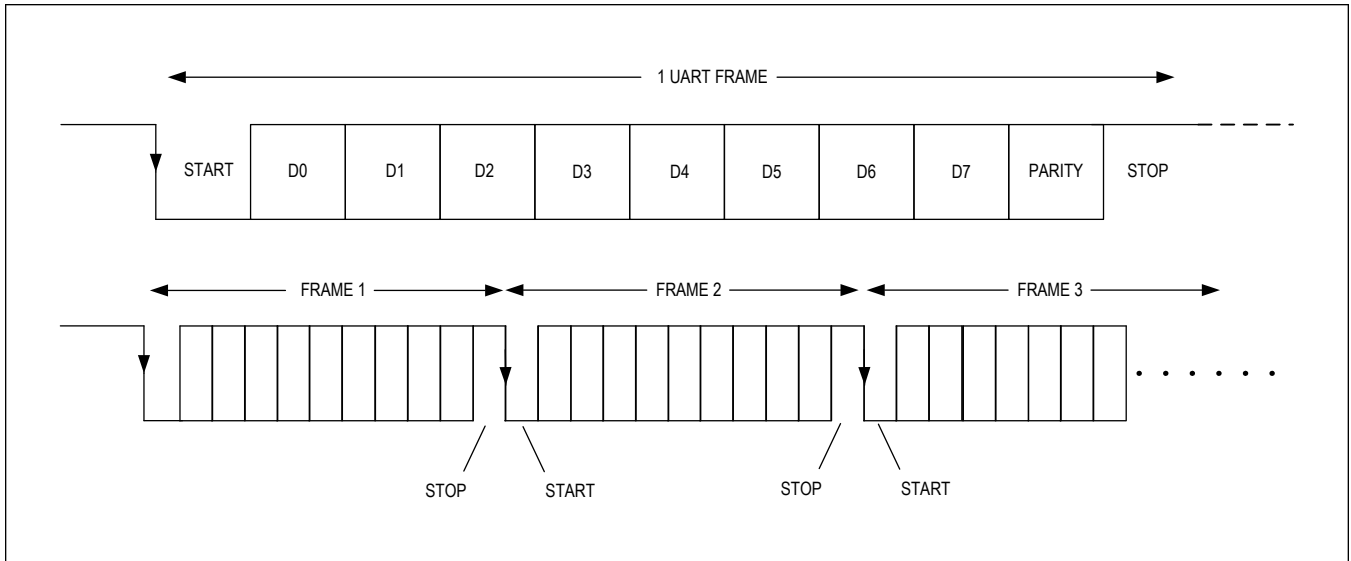


Figure 4. UART Frame Format

**Synchronization and Acknowledge Frames**

Each read/write packet must begin with a special Synchronization (SYNC) frame. This is a UART frame containing the data x79.

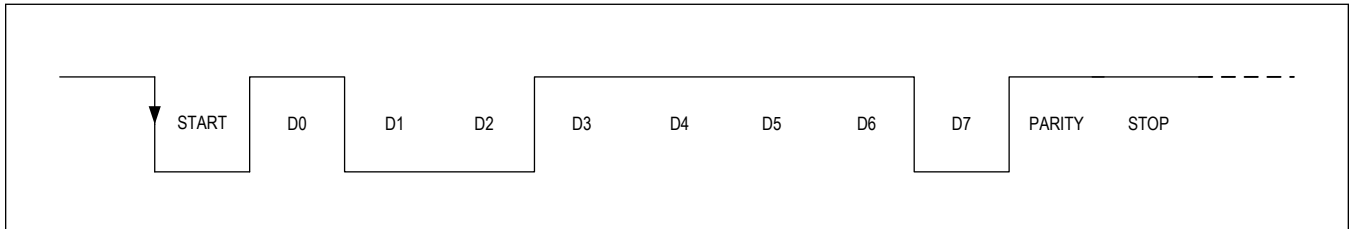


Figure 5. SYNC Frame

Each response packet always begins with a special Acknowledge (ACK) frame. This is a UART frame containing the data xC3.

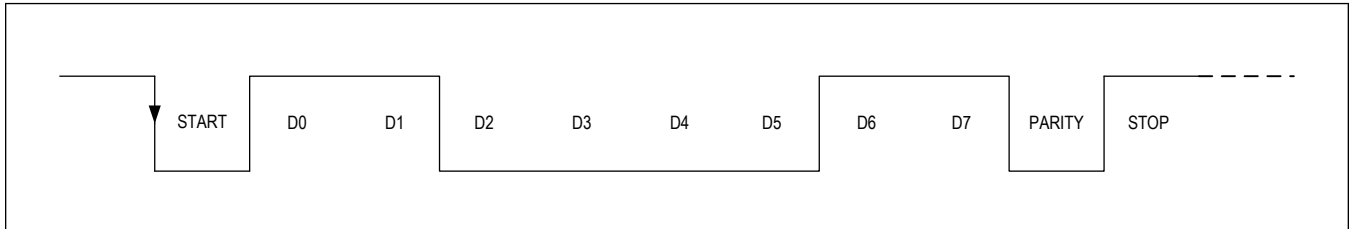


Figure 6. ACK Frame

**Device ID and Address frame format**

Each MAX25608 device in the star configuration should be assigned a unique device ID number using the resistor connected to the RADDR pin. There are 16 possible device IDs that can be assigned in this way, from x00 to x0F (see [Table 2](#)).

In addition to addressing devices individually, the MAX25608 also supports Global Call and Cluster Call write commands. A Global write command addresses all devices on the bus. A Cluster call addresses all devices with a matching cluster call ID in the CNFG\_UART register. Read commands cannot use the Global/Cluster Call option and must be addressed to a specific Device ID.

The address frame data bits are assigned as follows: the MSB is the Global/Cluster call bit, the next 6 bits are the Device ID, and the LSB is the Read/Write bit.

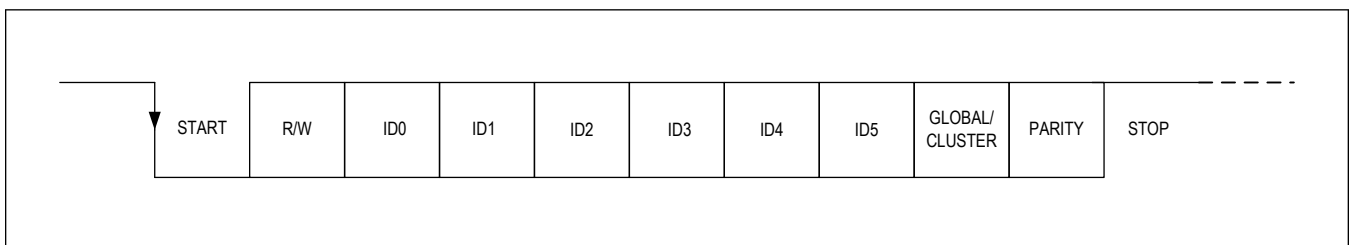


Figure 7. Device ID and Address Frame

**Write Transactions**

Each write packet consists of five UART frames on the RX pin. The first frame is the SYNC packet. The second frame consists of the Global/Cluster call flag, then the 6 bit device ID, and then the R/W bit. The R/W bit is low for a write command. The third frame is the register address being written to. The fourth frame is the lower byte of the data being written. The fifth and final frame includes the 3-bit CRC code followed by the upper five bits of the data being written. Upon receiving a valid write packet, the device responds with an ACK frame on the TX pin.

**CRC Error Checking**

Read/Write transactions are protected using a 3-bit cyclic redundancy check (CRC) on the frame. The CRC is provided by the master on last three data bits of each UART\_RX packet. The MAX25608 calculates its own CRC using the same polynomial, and the transaction is only accepted if the CRC bits match. For response frames on read packets, the MAX25608 appends its own 3-bit CRC code to the 13-bit read data.

The input to the CRC calculation consists of the data bits from the Device ID, Address, and Data frames.

The CRC calculation uses the polynomial  $x^3 + x^1 + 1$  with a starting value of 000.

## Register Map

## MAX25608

ADDRESS	NAME	MSB							LSB
<b>USER COMMANDS</b>									
0x00	<a href="#">NO_OP[15:8]</a>								REV_ID[4:0]
	<a href="#">NO_OP[7:0]</a>	-	-	-					CONSTANT_TEST[4:0]
0x01	<a href="#">SW_GO[15:8]</a>				-	-	-	-	-
	<a href="#">SW_GO[7:0]</a>	-	-	-	-	-	-	-	SW_GO_EN
0x02	<a href="#">CNFG_GEN_1[15:8]</a>				-	-	-	-	VOTH[1]
	<a href="#">CNFG_GEN_1[7:0]</a>	VOTH[0]		LED_SLEW[2:0]			DIV[1:0]		PWM_CLK_SEL[1:0]
0x04	<a href="#">CNFG_GEN_2[15:8]</a>				-		VSTH_4[2:0]		VSTH_3[2]
	<a href="#">CNFG_GEN_2[7:0]</a>	VSTH_3[1:0]		VSTH_2[2:0]			VSTH_1[2:0]		
0x05	<a href="#">CNFG_GEN_3[15:8]</a>				-		VSTH_8[2:0]		VSTH_7[2]
	<a href="#">CNFG_GEN_3[7:0]</a>	VSTH_7[1:0]		VSTH_6[2:0]			VSTH_5[2:0]		
0x06	<a href="#">CNFG_GEN_4[15:8]</a>				-		VSTH_12[2:0]		VSTH_11[2]
	<a href="#">CNFG_GEN_4[7:0]</a>	VSTH_11[1:0]		VSTH_10[2:0]			VSTH_9[2:0]		
0x07	<a href="#">CNFG_UART[15:8]</a>				-	-	-		CNFG_WATCHDOG[3:2]
	<a href="#">CNFG_UART[7:0]</a>	CNFG_WATCHDOG[1:0]					CID[5:0]		
0x08	<a href="#">CNFG_WATCHDOG[15:8]</a>				-				WD_LED_STATE[11:8]
	<a href="#">CNFG_WATCHDOG[7:0]</a>								WD_LED_STATE[7:0]
0x09	<a href="#">CNFG_OPEN_OVRD[15:8]</a>				-				OPEN_LED_OVR[11:8]
	<a href="#">CNFG_OPEN_OVRD[7:0]</a>								OPEN_LED_OVR[7:0]
0x0A	<a href="#">CNFG_GROUPA[15:8]</a>				-				GROUPA_SEL[11:8]
	<a href="#">CNFG_GROUPA[7:0]</a>								GROUPA_SEL[7:0]
0x0B	<a href="#">CNFG_GROUPB[15:8]</a>				-				GROUPB_SEL[11:8]
	<a href="#">CNFG_GROUPB[7:0]</a>								GROUPB_SEL[7:0]
0x0C	<a href="#">CNFG_MSK_GEN[15:8]</a>				TH_SHDN_ACT	-	-	-	-
	<a href="#">CNFG_MSK_GEN[7:0]</a>	-	MSK_UART_ERR	-	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CPRDY_N	MSK_RADC_ERR	MSK_TH_WARN
0x0D	<a href="#">CNFG_MSK_LED[15:8]</a>				-				CNFG_MSK_LED[11:8]
	<a href="#">CNFG_MSK_LED[7:0]</a>								CNFG_MSK_LED[7:0]
0x0E	<a href="#">STAT_RADC[15:8]</a>				-	-	-	-	-

ADDRESS	NAME	MSB							LSB
	<a href="#">STAT_RADC[7:0]</a>	-	-	-	RADC_D ONE	RADDR_ OVER_ RANGE	RGRAD E_ OVER_ RANGE	RADDR_ UNDER_ RANGE	RGRAD E_ UNDE R_ RANG E
0x0F	<a href="#">STAT_RES_CODE[15:8]</a> ↓				-	-	-	-	-
	<a href="#">STAT_RES_CODE[7:0]</a>	DEV_ID[3:0]			RGRADE[3:0]				
0x10	<a href="#">STAT_GEN[15:8]</a>				-	-	OTP_CR C_ERR	CONFIG _NOT_ D ONE	RADC_E RR
	<a href="#">STAT_GEN[7:0]</a>	EXT_CL K_ERR	UART_E RR	-	OPEN_L ED	SHORT_ LED	CP_RDY _N	TH_SHD N	TH_WA RN
0x11	<a href="#">STAT_UART[15:8]</a>				-	-	-	-	UART_ WATCH DOG
	<a href="#">STAT_UART[7:0]</a>	RX_TIM EOUT_ ERR	RX_CRC _ERR	RX_SYN C_ PERR	RX_PL_ PERR	RX_SYN C_ STOP _ERR	RX_PL_ STOP_ ERR	RX_PL_ START_ ERR	-
0x12	<a href="#">STAT_SHORT_LED[15:8]</a>				-	SHORT_LED_STAT[11:8]			
	<a href="#">STAT_SHORT_LED[7:0]</a> ↓	SHORT_LED_STAT[7:0]							
0x13	<a href="#">STAT_OPEN_LED[15:8]</a> ↓				-	OPEN_LED_STAT[11:8]			
	<a href="#">STAT_OPEN_LED[7:0]</a>	OPEN_LED_STAT[7:0]							
0x15	<a href="#">RTEMP[15:8]</a>				-	-	-	-	-
	<a href="#">RTEMP[7:0]</a>	RTEMP[7:0]							
0x16	<a href="#">LOW_DUTY_TH[15:8]</a>				-	LOW_DUTY_TH[11:8]			
	<a href="#">LOW_DUTY_TH[7:0]</a>	LOW_DUTY_TH[7:0]							
0x20	<a href="#">PSFT_GRP[15:8]</a>				-	-	-	PSFT_GROUP[1:0]	
	<a href="#">PSFT_GRP[7:0]</a>	PSFT[7:0]							
0x21	<a href="#">PSFT_1[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_1[7:0]</a>	PSFT_1[7:0]							
0x22	<a href="#">PSFT_2[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_2[7:0]</a>	PSFT_2[7:0]							
0x23	<a href="#">PSFT_3[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_3[7:0]</a>	PSFT_3[7:0]							
0x24	<a href="#">PSFT_4[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_4[7:0]</a>	PSFT_4[7:0]							
0x25	<a href="#">PSFT_5[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_5[7:0]</a>	PSFT_5[7:0]							
0x26	<a href="#">PSFT_6[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_6[7:0]</a>	PSFT_6[7:0]							
0x27	<a href="#">PSFT_7[15:8]</a>				-	-	-	-	-
	<a href="#">PSFT_7[7:0]</a>	PSFT_7[7:0]							
0x28	<a href="#">PSFT_8[15:8]</a>				-	-	-	-	-

ADDRESS	NAME	MSB					LSB
	<a href="#">PSFT_8[7:0]</a>						PSFT_8[7:0]
0x29	<a href="#">PSFT_9[15:8]</a>				-	-	-
	<a href="#">PSFT_9[7:0]</a>						PSFT_9[7:0]
0x2A	<a href="#">PSFT_10[15:8]</a>				-	-	-
	<a href="#">PSFT_10[7:0]</a>						PSFT_10[7:0]
0x2B	<a href="#">PSFT_11[15:8]</a>				-	-	-
	<a href="#">PSFT_11[7:0]</a>						PSFT_11[7:0]
0x2C	<a href="#">PSFT_12[15:8]</a>				-	-	-
	<a href="#">PSFT_12[7:0]</a>						PSFT_12[7:0]
0x30	<a href="#">TDIM_GRP[15:8]</a>				-	-	-
	<a href="#">TDIM_GRP[7:0]</a>	-	-	TDIM_GROUP[1:0]			TDIM[2:0]
0x31	<a href="#">TDIM_3_2_1[15:8]</a>				-	-	TDIM_3[2:0]
	<a href="#">TDIM_3_2_1[7:0]</a>	-		TDIM_2[2:0]			TDIM_1[2:0]
0x32	<a href="#">TDIM_6_5_4[15:8]</a>				-	-	TDIM_6[2:0]
	<a href="#">TDIM_6_5_4[7:0]</a>	-		TDIM_5[2:0]			TDIM_4[2:0]
0x33	<a href="#">TDIM_9_8_7[15:8]</a>				-	-	TDIM_9[2:0]
	<a href="#">TDIM_9_8_7[7:0]</a>	-		TDIM_8[2:0]			TDIM_7[2:0]
0x34	<a href="#">TDIM_12_11_10[15:8]</a>				-	-	TDIM_12[2:0]
	<a href="#">TDIM_12_11_10[7:0]</a>	-		TDIM_11[2:0]			TDIM_10[2:0]
0x40	<a href="#">PWM_GRP_A_DUTY[15:8]</a>				FADE_A		DUTY_A[11:8]
	<a href="#">PWM_GRP_A_DUTY[7:0]</a>						DUTY_A[7:0]
0x41	<a href="#">PWM_GRP_B_DUTY[15:8]</a>				FADE_B		DUTY_B[11:8]
	<a href="#">PWM_GRP_B_DUTY[7:0]</a>						DUTY_B[7:0]
0x42	<a href="#">PWM1[15:8]</a>				FADE_1		DUTY_1[11:8]
	<a href="#">PWM1[7:0]</a>						DUTY_1[7:0]
0x43	<a href="#">PWM2[15:8]</a>				FADE_2		DUTY_2[11:8]
	<a href="#">PWM2[7:0]</a>						DUTY_2[7:0]
0x44	<a href="#">PWM3[15:8]</a>				FADE_3		DUTY_3[11:8]
	<a href="#">PWM3[7:0]</a>						DUTY_3[7:0]
0x45	<a href="#">PWM4[15:8]</a>				FADE_4		DUTY_4[11:8]
	<a href="#">PWM4[7:0]</a>						DUTY_4[7:0]
0x46	<a href="#">PWM5[15:8]</a>				FADE_5		DUTY_5[11:8]
	<a href="#">PWM5[7:0]</a>						DUTY_5[7:0]
0x47	<a href="#">PWM6[15:8]</a>				FADE_6		DUTY_6[11:8]
	<a href="#">PWM6[7:0]</a>						DUTY_6[7:0]
0x48	<a href="#">PWM7[15:8]</a>				FADE_7		DUTY_7[11:8]
	<a href="#">PWM7[7:0]</a>						DUTY_7[7:0]
0x49	<a href="#">PWM8[15:8]</a>				FADE_8		DUTY_8[11:8]
	<a href="#">PWM8[7:0]</a>						DUTY_8[7:0]
0x4A	<a href="#">PWM9[15:8]</a>				FADE_9		DUTY_9[11:8]

ADDRESS	NAME	MSB					LSB
	<a href="#">PWM9[7:0]</a>					DUTY_9[7:0]	
0x4B	<a href="#">PWM10[15:8]</a>			FADE_1 0		DUTY_10[11:8]	
	<a href="#">PWM10[7:0]</a>					DUTY_10[7:0]	
0x4C	<a href="#">PWM11[15:8]</a>			FADE_1 1		DUTY_11[11:8]	
	<a href="#">PWM11[7:0]</a>					DUTY_11[7:0]	
0x4D	<a href="#">PWM12[15:8]</a>			FADE_1 2		DUTY_12[11:8]	
	<a href="#">PWM12[7:0]</a>					DUTY_12[7:0]	

**Register Details**

**NO\_OP (0x00)**

NO\_OP is a read-only register that reads the content of RGRADE, revision ID, and test pattern.

BIT		12	11	10	9	8		
Field				REV_ID[4:0]				
Reset				0x1				
Access Type				Read Only				
BIT	7	6	5	4	3	2	1	0
Field	-	-	-	CONSTANT_TEST[4:0]				
Reset	-	-	-	0b10001				
Access Type	-	-	-	Read Only				
BITFIELD	BITS		DESCRIPTION					
REV_ID	12:8		Revision Information: Reads back 5-bit hardware revision ID.					
CONSTANT_TEST	4:0		Test Pattern: 0x11 is always returned in this location for interface checking.					

**SW\_GO (0x01)**

SW\_GO us a read/write register that enables the PWN signals.

BIT		12	11	10	9	8		
Field		-	-	-	-	-		
Reset		-	-	-	-	-		
Access Type		-	-	-	-	-		
BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	SW_GO_EN
Reset	-	-	-	-	-	-	-	0b0
Access Type	-	-	-	-	-	-	-	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_GO_EN	0	<p>Switching Enable signal. Enables LED dimming operation and starts dimming counters. If SW_GO_EN = 0, all LED switches are closed and all PWM counters in the LED Controller are reset to 0. If SW_GO_EN = 1, all LED switches operate according to their programmed values and all PWM counters start counting from 0.</p> <p>SW_GO_EN must be low in order to change any of the CNFG_GEN_1/2/3/4 registers. If SW_GO_EN is high, the configuration change does not complete.</p> <p>The SW_GO_EN command should be issued after CP_RDY_N transitions low on STAT_GEN, ensuring CLK is present and CPP voltage is valid.</p>	<p>0x0: All LED switches are closed, and all PWM counters are reset to 0. 0x1: All LED switches operate according to their programmed values, and all PWM counters start counting from 0.</p>

**CNFG\_GEN\_1 (0x02)**

CNFG\_GEN\_1 is a read/write access register that controls the dimming clock divider ratio, the slew rate of the LED switches, the threshold used for the Open LED fault-detection function, and the functionality of the CLK pin.

SW\_GO\_EN should be set low before changing any configuration registers.

BIT			12	11	10	9	8	
Field			-	-	-	-	VOTH[1]	
Reset			-	-	-	-		
Access Type			-	-	-	-	Write, Read	
BIT	7	6	5	4	3	2	1	0
Field	VOTH[0]	LED_SLEW[2:0]			DIV[1:0]		PWM_CLK_SEL[1:0]	
Reset		0x7			0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VOTH	8:7	Sets the Open LED Threshold	<p>0x0: 14V 0x1: 9.33V 0x2: 4.66V 0x3: reserved</p>
LED_SLEW	6:4	Slew Control for the Internal LED Gate Driver. This register should only be written when SW_GO_EN = 0.	

BITFIELD	BITS	DESCRIPTION	DECODE
DIV	3:2	PWM Dimming-Frequency Select	0x0: f <sub>OSC</sub> /8,192 Nominal 2 kHz 0x0: External clock frequency divided by 8,192 0x1: f <sub>OSC</sub> /16,384 Nominal 1 kHz 0x1: External clock frequency divided by 16,384. 0x2: f <sub>OSC</sub> /32,768 Nominal 500 Hz 0x2: External clock frequency divided by 32,768. 0x3: f <sub>OSC</sub> /65,536 Nominal 250 Hz 0x3: External clock frequency divided by 65,536
PWM_CLK_SEL	1:0	Determines internal/external PWM clock and direction of CLK pin.	

**CNFG\_GEN\_2 (0x04)**

CNFG\_GEN\_2 controls the Short LED threshold (VSTH) of swithes 1, 2, 3, and 4.

SW\_GO\_EN should be set low before changing any configuration registers.

BIT			12	11	10	9	8
Field			-	VSTH_4[2:0]			VSTH_3[2]
Reset			-				
Access Type			-	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_3[1:0]		VSTH_2[2:0]			VSTH_1[2:0]		
Reset								
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_4	11:9	Sets the Short LED Threshold value for Switch 4	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_3	8:6	Sets the Short LED Threshold value for Switch 3	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V



BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_2	5:3	Sets the Short LED Threshold value for Switch 2	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_1	2:0	Sets the Short LED Threshold value for Switch 1	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

**CNFG\_GEN\_3 (0x05)**

CNFG\_GEN\_3 controls the Short LED threshold (VSTH) of switches 5, 6, 7, and 8.

SW\_GO\_EN should be set low before changing any configuration registers.

BIT	12	11	10	9	8
Field	-	VSTH_8[2:0]			VSTH_7[2]
Reset	-				
Access Type	-	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_7[1:0]		VSTH_6[2:0]			VSTH_5[2:0]		
Reset								
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_8	11:9	Sets the Short LED Threshold value for Switch 8	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_7	8:6	Sets the Short LED Threshold value for Switch 7	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_6	5:3	Sets the Short LED Threshold value for Switch 6	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_5	2:0	Sets the Short LED Threshold value for Switch 5	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

**CNFG\_GEN\_4 (0x06)**

CNFG\_GEN\_4 controls the Short LED threshold (VSTH) of switches 9, 10, 11, and 12.

SW\_GO\_EN should be set low before changing any configuration registers.

BIT	12	11	10	9	8
Field	-	VSTH_12[2:0]			VSTH_11[2]
Reset	-				
Access Type	-	Write, Read			Write, Read

BIT	7	6	5	4	3	2	1	0
Field	VSTH_11[1:0]		VSTH_10[2:0]			VSTH_9[2:0]		
Reset								
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_12	11:9	Sets the Short LED Threshold value for Switch 12	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_11	8:6	Sets the Short LED Threshold value for Switch 11	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_10	5:3	Sets the Short LED Threshold value for Switch 10	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_9	2:0	Sets the Short LED Threshold value for Switch 9	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

**CNFG\_UART (0x07)**

CNFG\_UART is a read/write access register that controls how the UART is configured, namely the cluster ID assignment and the operation of the UART Watchdog Timer.

BIT		12	11	10	9	8		
Field		-	-	-	CNFG_WATCHDOG[3:2]			
Reset		-	-	-				
Access Type		-	-	-	Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	CNFG_WATCHDOG[1:0]		CID[5:0]					
Reset			0b000001					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
CNFG_WAT CHDOG	9:6	This field controls the duration of the UART Watchdog Timer. When CNFG_WATCHDOG is set to a non-zero value, and no valid UART commands are received for a duration set by the CNFG_WATCHDOG field, the UART_Watchdog status bit is set. When the UART_Watchdog status bit is set: (1) The FAULTB pin is asserted. (2) The state of the switches is set according to the WD_LED_STATE register.	0x0: disabled 0x1: 200us 0x2: 500us 0x3: 1ms 0x4: 2ms 0x5: 5ms 0x6: 10ms 0x7: 20ms 0x8: 50ms 0x9: 100ms 0xA: 200ms 0xB: 500ms 0xC: 1s 0xD: 2s 0xE: 5s 0xF: 5s
CID	5:0	Cluster Identification: During a cluster call write transaction, the UART accepts the transaction if the received CID[5:0] matches the contents of this register.	

**CNFG\_WATCHDOG (0x08)**

BIT		12	11	10	9	8		
Field		–	WD_LED_STATE[11:8]					
Reset		–						
Access Type		–	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	WD_LED_STATE[7:0]							
Reset								
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
WD_LED_ST ATE	11:0	Sets the state of LEDs when UART timeout condition is detected.			0x0: Switch Open 0x1: Switch Closed			

**CNFG\_OPEN\_OVRD (0x09)**

OPEN\_OVRD is a read/write register that overrides the LED switching control signals. When this feature is disabled, the LED switch operates normally. When this feature is enabled, the LED switch is always forced to a closed position (i.e., the LED duty cycle is zero, regardless of the DUTY or TDIM settings).

The intent is to allow the  $\mu$ P to manually force the switch to stay closed after it has determined the particular LED is permanently opened. This further suppresses FAULTB signals from the switch(es) since LED faults are only detected when the switch opens.

BIT		12	11	10	9	8		
Field		–	OPEN_LED_OVR[11:8]					
Reset		–	0x000					
Access Type		–	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	OPEN_LED_OVR[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
OPEN_LED_ OVR	11:0	Open-LED Override: Program these bits to force the corresponding switch(es) to always be closed. This overrides the state of the corresponding DUTY registers.			0x0: Normal 0x1: LED switch is always closed.			

**CNFG\_GRP A (0x0A)**

CNFG\_GRP A is a read/write register that allows the user to assign particular LED drivers to this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT\_GRP (if PSFT\_GROUP==0001)
- TDIM\_GROUP (if TDIM\_GROUP=0001)
- PWM\_GRP A\_DUTY

BIT		12	11	10	9	8		
Field		–	GROUPA_SEL[11:8]					
Reset		–	0x000					
Access Type		–	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	GROUPA_SEL[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
GROUPA_SEL	11:0	Set high if assigning a register to GroupA.				0x0: Not assigned 0x1: Assigned		

**CNFG\_GRPB (0x0B)**

CNFG\_GRPB is a read/write register that allows the user to assign particular LED drivers to this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT\_GRP (if PSFT\_GROUP==00010)
- TDIM\_GROUP (if TDIM\_GROUP=0010)
- PWM\_GRPB\_DUTY

BIT		12	11	10	9	8		
Field		–	GROUPB_SEL[11:8]					
Reset		–	0x000					
Access Type		–	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	GROUPB_SEL[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
GROUPB_SEL	11:0	Set high if assigning a register to GroupB.				0x0: Not assigned 0x1: Assigned		

**CNFG\_MSK\_GEN (0x0C)**

CNFG\_MSK is a read/write access register that controls the masking of fault conditions from the FAULTB pin.

BIT		12	11	10	9	8
Field		TH_SHDN_ACT	–	–	–	–
Reset		0b0	–	–	–	–
Access Type		Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	MSK_UART_ERR	–	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CP_RDY_N	MSK_RADC_ERR	MSK_TH_WARN
Reset	–	0b0	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TH_SHDN_ACT	12	Thermal-Shutdown Action: This bit selects whether to open or close the LED switches when a TH_SHDN is high.	0x0: Closes all LED switches. 0x1: Opens all LED switches.
MSK_UART_ERR	6	Masks SPI_ERR to FAULTB.	0x0: UART_ERR being set high asserts the FAULTB pin. 0x1: UART_ERR bit does not assert the FAULTB pin.
MSK_OPEN_LED	4	Masks all open-LED detections to FAULTB.	0x0: Any OPEN_LED__ detections assert the FAULTB pin. 0x1: Any OPEN_LED__ detections do not assert the FAULTB pin.
MSK_SHORT_LED	3	Masks all STAT_SHORT_LED detections to FAULTB.	0x0: Any STAT_SHORT_LED bits set high assert the FAULTB pin. 0x1: Any STAT_SHORT_LED bits set high do not assert the FAULTB pin.
MSK_CP_RDY_N	2	Mask CP_RDY_N to FAULTB.	0x0: CP_RDY_N asserts the FAULTB pin. 0x1: CP_RDY_N does not assert the FAULTB pin.
MSK_RADC_ERR	1	Masks SPI_ERR to FAULTB.	0x0: No masking of RADC_ERR. 0x1: Mask RADC_ERR from generating fault.
MSK_TH_WARN	0	Mask-Thermal Warning to FAULTB.	0x0: TH_WARN asserts the FAULTB pin. 0x1: TH_WARN does not assert the FAULTB pin.

### CNFG\_MSK\_LED (0x0D)

CNFG\_MSK\_LED prevents LED faults from asserting the FAULTB pin. This allows the µP to instruct the part to ignore faults from a particular LED when that LED is deliberately not populated in the application.

BIT	12	11	10	9	8
Field	–	CNFG_MSK_LED[11:8]			
Reset	–	0x000			
Access Type	–	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	CNFG_MSK_LED[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CNFG_MSK_LED	11:0	Set bit(s) high to mask OPEN_LED and SHORT_LED from those LEDs asserting FAULTB.

**STAT\_RADC (0x0E)**

Status indicators for RGRADE and RADDR decoding

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RADC_DONE	RADDR_OVER_RANGE	RGRADE_OVER_RANGE	RADDR_UNDER_RANGE	RGRADE_UNDER_RANGE
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RADC_DONE	4	Status Indicator for RADDR/RGRADE decoding	0x0: RADC measurement incomplete 0x1: RADC measurement is complete
RADDR_OVER_RANGE	3	Indicates that the RADDR resistor value is above the supported range.	0x0: Normal operation 0x1: RADDR Over Range, or an open is detected.
RGRADE_OVER_RANGE	2	Indicates that the RGRADE resistor value is above the supported range.	0x0: Normal operation 0x1: RGRADE Over Range, or an open is detected.
RADDR_UNDER_RANGE	1	Indicates that the RADDR resistor value is below the supported range.	0x0: Normal operation 0x1: RADDR Under Range, or a short detected.
RGRADE_UNDER_RANGE	0	Indicates that the RGRADE resistor value is below the supported range.	0x0: Normal operation 0x1: RGRADE under range, or a short detected.

**STAT\_RES\_CODE (0x0F)**

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[3:0]				RGRADE[3:0]			
Reset								
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
DEV_ID	7:4	Decoded value of the RADDR external resistor. This value is used to set the UART Device ID.
RGRADE	3:0	Decoded value of the external RGRADE resistor.

**STAT\_GEN (0x10)**

STAT\_GEN is a read-only access register that provides general operations and warnings. FAULTB is asserted whenever any of these bits is high, unless the corresponding MASK bit is set.

BIT	12	11	10	9	8
Field	–	–	OTP_CRC_ERR	CONFIG_N OT_DONE	RADC_ERR
Reset	–	–		0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	EXT_CLK_ERR	UART_ERR	–	OPEN_LED	SHORT_LED	CP_RDY_N	TH_SHDN	TH_WARN
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OTP_CRC_ERR	10	OTP CRC Error Bit. Indicates that a CRC error has been detected when reading back the internal OTP memory. Status bit only, does not assert FAULTB.	
CONFIG_NOT_DONE	9	This bit indicates that the UART interface has not completed programming the LED switch configuration, triggered by writing CNFG_GEN. The master should ensure this bit is low before attempting to program CNFG_GEN. This bit does not assert the FAULTB pin.	0x0: Configuration complete; ready for new CNFG_GEN command. 0x1: Configuration not complete.
RADC_ERR	8	This signal indicates that the RGRADE read operation is not complete. When the signal goes low, the read is complete and RGRADE[2:0] in register 0x0 is valid. This signal does not assert the FAULTB pin.	0x0: RADC completes. 0x1: RADC error.
EXT_CLK_ERR	7	EXT_CLK_ERR is asserted when the part is configured to use the CLKIN pin as the reference clock (PWM_CLK_SEL = x2 or x3) and the external clock is slower than the minimum operating frequency.	0x0: CLKIN operating in spec. 0x1: External Clock Error.
UART_ERR	6	SPI_ERR is asserted if any of the error bits in SNFG_SPI are set.	0x0: UART is operating normally. 0x1: At least 1 of UART errors has been asserted.
OPEN_LED	4	OPEN_LED is asserted if any OPEN_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has open detected.
SHORT_LED	3	SHORT_LED is asserted if any SHORT_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has short detected.
CP_RDY_N	2	CP_RDY_N is a read-only bit that indicates that the charge-pump voltage is below the operating threshold.	0x0: CP operating normally. 0x1: CP is below V_CPP_OK threshold.
TH_SHDN	1	Thermal Shutdown. Latched, write 1 clears.	
TH_WARN	0	Thermal Warning. Latched, write 1 to clear.	0x0: Normal operation. 0x1: Device has exceeded the thermal-warning threshold.



STAT\_UART (0x11)

BIT			12	11	10	9	8	
Field			–	–	–	–	UART_WAT CHDOG	
Reset			–	–	–	–		
Access Type			–	–	–	–	Write 1 to Clear, Read	
BIT	7	6	5	4	3	2	1	0
Field	RX_TIMEO UT_ERR	RX_CRC_E RR	RX_SYNC_ PERR	RX_PL_PE RR	RX_SYNC_ STOP_ERR	RX_PL_ST OP_ERR	RX_PL_ST ART_ERR	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
UART_WAT CHDOG	8	The UART Watchdog Timer will assert whenever there has been no activity on the UART_RX pin for at least four seconds.	
RX_TIMEOU T_ERR	7	This bit shall be asserted if there are no UART_RX transitions for more than 16 bit lengths during a UART packet. The bit length shall be determined by the SYNC frame of each packet.	0x0: Normal operation. 0x1: UART Rx times out.
RX_CRC_ER R	6	CRC Error Indicator (SPI_ERR Term: Read only, clear-on-read)	0x0: Normal operation. 0x1: CRC Error: At least one UART transaction rejected due to a failed CRC check.
RX_SYNC_P ERR	5	Parity Error in RX Sync Frame detected	0x0: Normal operation. 0x1: Rx Sync Frame parity error detected.
RX_PL_PER R	4	UART Error: Parity Error detected on RX Payload data	0x0: Normal operation. 0x1: UART Rx payload parity error detected.
RX_SYNC_S TOP_ERR	3	RX Sync Frame Stop Bit Error detected	0x0: Normal operation. 0x1: Rx Sync Frame STOP bit error detected
RX_PL_STO P_ERR	2	UART Parity Error detected in RX Data Frames	0x0: Normal operation. 0x1: Rx Payload Frame STOP bit error.
RX_PL_STA RT_ERR	1	UART Start Bit Error on RX Data Frame	0x0: Normal operation. 0x1: Rx Payload Frame START bit error.

STAT\_SHORT\_LED (0x12)

STAT\_SHORT\_LED is a read-only access register that provides short-detect information on the 12 LED output drivers.

BIT			12	11	10	9	8	
Field			–	SHORT_LED_STAT[11:8]				
Reset			–	0x000				
Access Type			–	Write 1 to Clear, Read				

BIT	7	6	5	4	3	2	1	0
Field	SHORT_LED_STAT[7:0]							
Reset	0x000							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION
SHORT_LED_STAT	11:0	Indicates that a LED short has been detected.

**STAT\_OPEN\_LED (0x13)**

STAT\_OPEN is a read-only access register that provides open-detect information on the twelve LED output drivers.

BIT	12	11	10	9	8
Field	OPEN_LED_STAT[11:8]				
Reset	0x000				
Access Type	Write 1 to Clear, Read				

BIT	7	6	5	4	3	2	1	0
Field	OPEN_LED_STAT[7:0]							
Reset	0x000							
Access Type	Write 1 to Clear, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_LED_STAT	11:0	Indicates that an open-LED condition has been detected.	0x0: Normal 0x1: Open LED

**RTEMP (0x15)**

BIT	12	11	10	9	8
Field	–	–	–	–	–
Reset	–	–	–	–	–
Access Type	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	RTEMP[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RTEMP	7:0	Raw 8-bit ADC value representing the ratio of the voltage at the RTEMP pin relative to the voltage at the VDD pin. This value can be used in conjunction with an external NTC resistor network to provide remote temperature sensing functionality.

LOW\_DUTY\_TH (0x16)

<b>BIT</b>				<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>				–	LOW_DUTY_TH[11:8]			
<b>Reset</b>				–	0x10			
<b>Access Type</b>				–	Write, Read			
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	LOW_DUTY_TH[7:0]							
<b>Reset</b>	0x10							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>			<b>DESCRIPTION</b>				
LOW_DUTY_TH	11:0			The Low Duty Threshold is used to filter out LED fault signals during short duty cycles when the voltage across the switch might not settle to a final value, causing invalid detection of the Short LED condition. When the DUTY register of a switch is less than LOW_DUTY_TH, the SHORT_LED signal is masked and SHORT_LED_STAT is not asserted for that switch.				

PSFT\_GRP (0x20)

PSFT\_GRP is a read/write register that allows the user to assign the same phase shift to one or more LED drivers. The contents of PSFT are written to the desired group specified by PSFT\_GROUP.

**Example:**

If PSFT\_GROUP == Group A, PSFT == 0001, and LED11, LED9, and LED6 are assigned to Group A (through CNFG\_GRP\_A), then PSFT\_11, PSFT\_9, and PSFT\_6 contain 0001 after the transaction is executed.

<b>BIT</b>				<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>				–	–	–	PSFT_GROUP[1:0]	
<b>Reset</b>				–	–	–	0x1	
<b>Access Type</b>				–	–	–	Write, Read	
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	PSFT[7:0]							
<b>Reset</b>	0x0							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>			<b>DESCRIPTION</b>				
PSFT_GROUP	9:8			Group Select: bit 0: Group A selected bit 1: Group B selected  Multiple groups can be selected at a time. <b>Note:</b> 00 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.				
PSFT	7:0			Phase select.				

**PSFT\_1 (0x21)**

PSFT\_1 is a read/write register that controls the phase shift for LED1.

BIT		12	11	10	9	8		
Field		–	–	–	–	–		
Reset		–	–	–	–	–		
Access Type		–	–	–	–	–		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_1	7:0	LED 1 Phase Select.

**PSFT\_2 (0x22)**

PSFT\_2 is a read/write register that controls the phase shift for LED2.

BIT		12	11	10	9	8		
Field		–	–	–	–	–		
Reset		–	–	–	–	–		
Access Type		–	–	–	–	–		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_2[7:0]							
Reset	0x21							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_2	7:0	LED 2 Phase Select.

**PSFT\_3 (0x23)**

PSFT\_3 is a read/write register that controls the phase shift for LED3.

BIT		12	11	10	9	8		
Field		–	–	–	–	–		
Reset		–	–	–	–	–		
Access Type		–	–	–	–	–		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_3[7:0]							
Reset	0x42							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_3	7:0	LED 3 Phase Select.

**PSFT\_4 (0x24)**

PSFT\_4 is a read/write register that controls the phase shift for LED4.

BIT		12	11	10	9	8		
Field		-	-	-	-	-		
Reset		-	-	-	-	-		
Access Type		-	-	-	-	-		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_4[7:0]							
Reset	0x64							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION						
PSFT_4	7:0	LED 4 Phase Select.						

**PSFT\_5 (0x25)**

PSFT\_5 is a read/write register that controls the phase shift for LED5.

BIT		12	11	10	9	8		
Field		-	-	-	-	-		
Reset		-	-	-	-	-		
Access Type		-	-	-	-	-		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_5[7:0]							
Reset	0x85							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION						
PSFT_5	7:0	LED 5 Phase Select.						

**PSFT\_6 (0x26)**

PSFT\_6 is a read/write register that controls the phase shift for LED6.

BIT		12	11	10	9	8
Field		-	-	-	-	-
Reset		-	-	-	-	-
Access Type		-	-	-	-	-

BIT	7	6	5	4	3	2	1	0
Field	PSFT_6[7:0]							
Reset	0x106							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_6	7:0	LED 6 Phase Select.

**PSFT\_7 (0x27)**

PSFT\_7 is a read/write register that controls the phase shift for LED7.

BIT	12	11	10	9	8
Field	-	-	-	-	-
Reset	-	-	-	-	-
Access Type	-	-	-	-	-

BIT	7	6	5	4	3	2	1	0
Field	PSFT_7[7:0]							
Reset	0x128							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_7	7:0	LED 7 Phase Select.

**PSFT\_8 (0x28)**

PSFT\_8 is a read/write register that controls the phase shift for LED8.

BIT	12	11	10	9	8
Field	-	-	-	-	-
Reset	-	-	-	-	-
Access Type	-	-	-	-	-

BIT	7	6	5	4	3	2	1	0
Field	PSFT_8[7:0]							
Reset	0x149							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_8	7:0	LED 8 Phase Select.

**PSFT\_9 (0x29)**

PSFT\_9 is a read/write register that controls the phase shift for LED9.

<b>BIT</b>				<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>				–	–	–	–	–
<b>Reset</b>				–	–	–	–	–
<b>Access Type</b>				–	–	–	–	–
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	PSFT_9[7:0]							
<b>Reset</b>	0x170							
<b>Access Type</b>	Write, Read							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>
PSFT_9	7:0	LED 9 Phase Select.

**PSFT\_10 (0x2A)**

PSFT\_10 is a read/write register that controls the phase shift for LED10.

<b>BIT</b>				<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>				–	–	–	–	–
<b>Reset</b>				–	–	–	–	–
<b>Access Type</b>				–	–	–	–	–
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	PSFT_10[7:0]							
<b>Reset</b>	0x192							
<b>Access Type</b>	Write, Read							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>
PSFT_10	7:0	LED 10 Phase Select.

**PSFT\_11 (0x2B)**

PSFT\_11 is a read/write register that controls the phase shift for LED11.

<b>BIT</b>				<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>				–	–	–	–	–
<b>Reset</b>				–	–	–	–	–
<b>Access Type</b>				–	–	–	–	–
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	PSFT_11[7:0]							
<b>Reset</b>	0x213							
<b>Access Type</b>	Write, Read							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>
PSFT_11	7:0	LED 11 Phase Select.

PSFT\_12 (0x2C)

PSFT\_12 is a read/write register that controls the phase shift for LED12.

BIT		12	11	10	9	8		
Field		–	–	–	–	–		
Reset		–	–	–	–	–		
Access Type		–	–	–	–	–		
BIT	7	6	5	4	3	2	1	0
Field	PSFT_12[7:0]							
Reset	0x234							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_12	7:0	LED 12 Phase Select.

TDIM\_GRP (0x30)

TDIM\_GRP is a read/write register that allows the user to assign the same dimming period to one or more LED drivers. The contents of TDIM are written to the desired group specified by TDIM\_GROUP.

**Example:**

If TDIM\_GROUP == Group A, PSFT == 001, and LED12, LED9, and LED6 are assigned to Group A (through CNFG\_GRP\_A), then TDIM\_12, TDIM\_9, and TDIM\_6 contain 001 after the transaction is executed.

BIT		12	11	10	9	8		
Field		–	–	–	–	–		
Reset		–	–	–	–	–		
Access Type		–	–	–	–	–		
BIT	7	6	5	4	3	2	1	0
Field	–	–	TDIM_GROUP[1:0]		–	TDIM[2:0]		
Reset	–	–	0x1		–	0b000		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_GRP	5:4	Group Select: Bit 0: Group A selected Bit 1: Group B selected  Multiple groups can be selected at a time. <b>Note:</b> 0000 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.	



BITFIELD	BITS	DESCRIPTION	DECODE
TDIM	2:0	Dimming Period Select	0x0: update PWM duty cycle every 1 PWM period 0x1: update PWM duty cycle every 2 PWM periods 0x2: update PWM duty cycle every 4 PWM periods 0x3: update PWM duty cycle every 8 PWM periods 0x4: update PWM duty cycle every 16 PWM periods 0x5: update PWM duty cycle every 32 PWM periods 0x6: update PWM duty cycle every 32 PWM periods 0x7: update PWM duty cycle every 32 PWM periods 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

**TDIM\_3\_2\_1 (0x31)**

TDIM\_3\_2\_1 is a read/write register that controls the dimming period for LED drivers 3, 2, and 1.

BIT				12	11	10	9	8
Field				-	-	TDIM_3[2:0]		
Reset				-	-	0b000		
Access Type				-	-	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	-	TDIM_2[2:0]			-	TDIM_1[2:0]		
Reset	-	0b000			-	0b000		
Access Type	-	Write, Read			-	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_3	10:8	LED 3 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_2	6:4	LED 2 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_1	2:0	LED 1 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

**TDIM\_6\_5\_4 (0x32)**

TDIM\_6\_5\_4 is a read/write register that controls the dimming period for LED drivers 6, 5, and 4.

BIT				12	11	10	9	8
Field				-	-	TDIM_6[2:0]		
Reset				-	-	0b000		
Access Type				-	-	Write, Read		
BIT	7	6	5	4	3	2	1	0
Field	-	TDIM_5[2:0]			-	TDIM_4[2:0]		
Reset	-	0b000			-	0b000		
Access Type	-	Write, Read			-	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_6	10:8	LED 6 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_5	6:4	LED 5 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_4	2:0	LED 4 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

**TDIM\_9\_8\_7 (0x33)**

TDIM\_9\_8\_7 is a read/write register that controls the dimming period for LED drivers 9, 8, and 7.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		–	–	TDIM_9[2:0]				
<b>Reset</b>		–	–	0b000				
<b>Access Type</b>		–	–	Write, Read				
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	–	TDIM_8[2:0]			–	TDIM_7[2:0]		
<b>Reset</b>	–	0b000			–	0b000		
<b>Access Type</b>	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_9	10:8	LED 9 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_8	6:4	LED 8 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_7	2:0	LED 7 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

**TDIM\_12\_11\_10 (0x34)**

TDIM\_12\_11\_10 is a read/write register that controls the dimming period for LED drivers 12, 11, and 10.

BIT		12	11	10	9	8		
Field		-	-	TDIM_12[2:0]				
Reset		-	-	0b000				
Access Type		-	-	Write, Read				
BIT	7	6	5	4	3	2	1	0
Field	-	TDIM_11[2:0]			-	TDIM_10[2:0]		
Reset	-	0b000			-	0b000		
Access Type	-	Write, Read			-	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_12	10:8	LED 12 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_11	6:4	LED 11 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_10	2:0	LED 10 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8,192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

**PWM\_GRP\_A\_DUTY (0x40)**

PWM\_GRP\_A\_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM dimming to one or more LED drivers.

The contents of DUTY\_A are written to LEDs assigned to Group A.

**Example:**

If DUTY\_A == 0x0AA and LED11, LED8, and LED5 are assigned to Group A (through CNFG\_GRP\_A), then DUTY\_11, DUTY\_8, and DUTY\_5 contain 0x0AA after the transaction is executed.

BIT		12	11	10	9	8
Field		FADE_A	DUTY_A[11:8]			
Reset		0b0	0x000			
Access Type		Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_A	12	Group A PWM Dimming Enable	0x0: Disabled 0x1: Enabled
DUTY_A	11:0	Group A Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xff = 100% duty cycle	

### PWM\_GRPB\_DUTY (0x41)

PWM\_GRPB\_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM dimming to one or more LED drivers.

The contents of DUTY\_B are written to LEDs assigned to Group B.

#### Example:

If DUTY\_B == 0x0AA and LED11, LED9, and LED6 are assigned to Group B (through CNFG\_GRPB), then DUTY\_11, DUTY\_9, and DUTY\_6 contain 0x0AA after the transaction is executed.

BIT	12	11	10	9	8
Field	FADE_B	DUTY_B[11:8]			
Reset	0b0	0x000			
Access Type	Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FADE_B	12	Group B PWM Dimming Enable	0x0: Enabled 0x1: Disabled
DUTY_B	11:0	Group B Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xff = 100% duty cycle	

### PWM1 (0x42)

PWM1 is a read/write register that configures the LED1 duty cycle and enables/disables PWM dimming.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_1	DUTY_1[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_1[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_1	12	LED1 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_1	11:0	LED1 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM2 (0x43)**

PWM2 is a read/write register that configures the LED2 duty cycle and enables/disables PWM dimming.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_2	DUTY_2[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_2[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_2	12	LED2 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_2	11:0	LED2 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM3 (0x44)**

PWM3 is a read/write register that configures the LED3 duty cycle and enables/disables PWM dimming.



<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_3	DUTY_3[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_3[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_3	12	LED3 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_3	11:0	LED3 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle						

**PWM4 (0x45)**

PWM4 is a read/write register that configures the LED4 duty cycle and enables/disables PWM dimming.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_4	DUTY_4[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_4[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_4	12	LED4 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_4	11:0	LED4 Duty-Cycle Selection: 0x000= off 0x001 = 1/4,095 duty cycle ... 0xfff = 100% duty cycle						

**PWM5 (0x46)**

PWM5 is a read/write register that configures the LED5 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_5	DUTY_5[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_5[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FADE_5	12	LED5 PWM Dimming Enable			0x0: Enabled 0x1: Disabled			
DUTY_5	11:0	LED5 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM6 (0x47)**

PWM6 is a read/write register that configures the LED6 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_6	DUTY_6[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_6[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FADE_6	12	LED6 PWM Dimming Enable			0x0: Enabled 0x1: Disabled			
DUTY_6	11:0	LED6 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM7 (0x48)**

PWM7 is a read/write register that configures the LED7 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_7	DUTY_7[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_7[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FADE_7	12	LED7 PWM Dimming Enable			0x0: Enabled 0x1: Disabled			
DUTY_7	11:0	LED7 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM8 (0x49)**

PWM8 is a read/write register that configures the LED8 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_8	DUTY_8[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_8[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION			DECODE			
FADE_8	12	LED8 PWM Dimming Enable			0x0: Enabled 0x1: Disabled			
DUTY_8	11:0	LED8 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM9 (0x4A)**

PWM9 is a read/write register that configures the LED9 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_9	DUTY_9[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_9[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
FADE_9	12	LED9 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_9	11:0	LED9 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM10 (0x4B)**

PWM10 is a read/write register that configures the LED10 duty cycle and enables/disables PWM dimming.

BIT		12	11	10	9	8		
Field		FADE_10	DUTY_10[11:8]					
Reset		0b0	0x000					
Access Type		Write, Read	Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	DUTY_10[7:0]							
Reset	0x000							
Access Type	Write, Read							
BITFIELD	BITS	DESCRIPTION				DECODE		
FADE_10	12	LED10 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_10	11:0	LED10 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

**PWM11 (0x4C)**

PWM11 is a read/write register that configures the LED11 duty cycle and enables/disables PWM dimming.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_11	DUTY_11[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_11[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_11	12	LED11 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_11	11:0	LED11 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

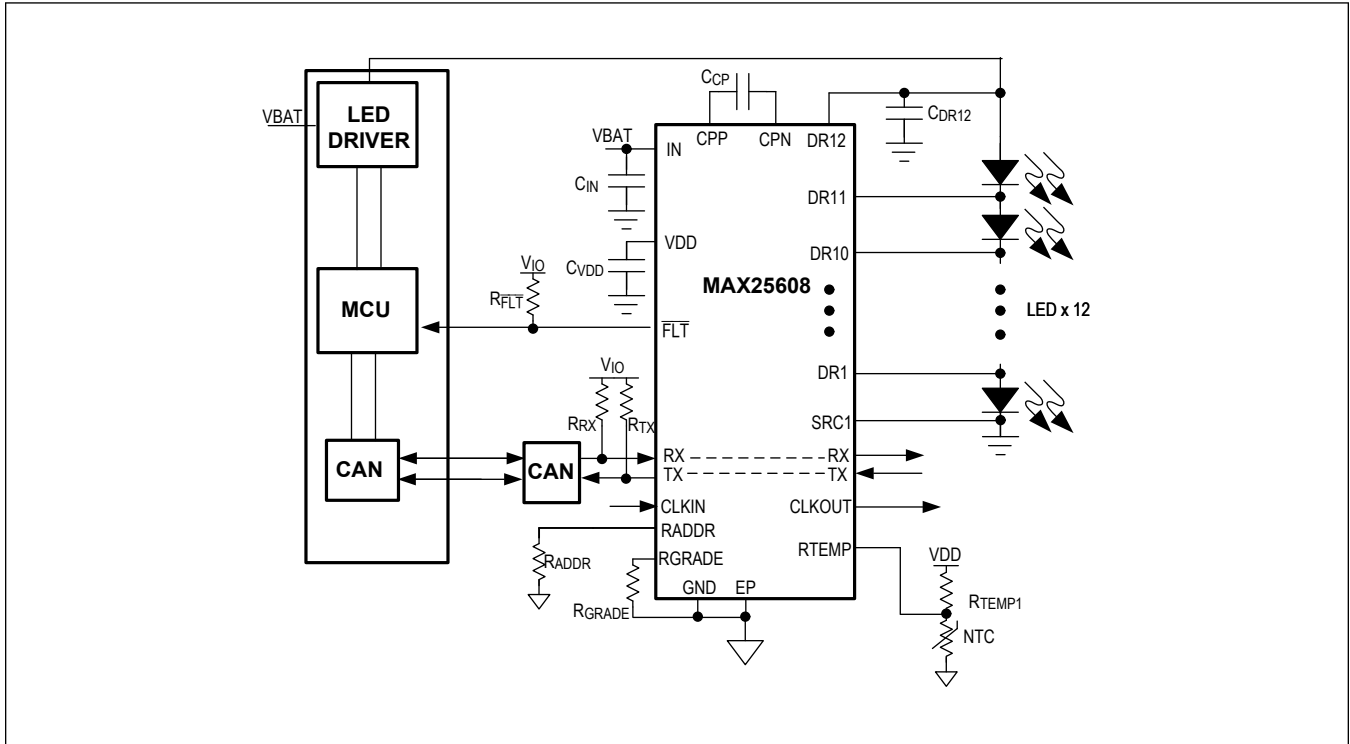
**PWM12 (0x4D)**

PWM12 is a read/write register that configures the LED12 duty cycle and enables/disables PWM dimming.

<b>BIT</b>		<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>		
<b>Field</b>		FADE_12	DUTY_12[11:8]					
<b>Reset</b>		0b0	0x000					
<b>Access Type</b>		Write, Read	Write, Read					
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DUTY_12[7:0]							
<b>Reset</b>	0x000							
<b>Access Type</b>	Write, Read							
<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>				<b>DECODE</b>		
FADE_12	12	LED12 PWM Dimming Enable				0x0: Enabled 0x1: Disabled		
DUTY_12	11:0	LED12 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4,095 duty cycle ... 0xffff = 100% duty cycle						

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX25608AUI/V+	-40°C to +125°C	28-TSSOP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

\*EP = Exposed pad.

MAX25608

## Twelve Switch High Brightness LED Matrix Manager for Automotive Front Lights

### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Release for Market Intro	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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