General Description

The MAX2242 low-voltage linear power amplifier (PA) is designed for 2.4GHz ISM-band wireless LAN applications. It delivers +22.5dBm of linear output power with an adjacent-channel power ratio (ACPR) of <-33dBc 1st-side lobe and <-55dBc 2nd-side lobe, compliant with the IEEE 802.11b 11MB/s WLAN standard with at least 3dB margin. The PA is packaged in the tiny 3x4 chip-scale package (UCSP™), measuring only 1.5mm x 2.0mm, ideal for radios built in small PC card and compact flash card form factors.

The MAX2242 PA consists of a three-stage PA, power detector, and power management circuitry. The power detector provides over 20dB of dynamic range with ±0.8dB accuracy at the highest output power level. An accurate automatic level control (ALC) function can be easily implemented using this detector circuit.

The PA also features an external bias control pin. Through the use of an external DAC, the current can be throttled back at lower output power levels while maintaining sufficient ACPR performance. As a result, the highest possible efficiency is maintained at all power levels. The device operates over a single +2.7V to +3.6V power-supply range. An on-chip shutdown feature reduces operating current to 0.5µA, eliminating the need for an external supply switch.

Applications

- IEEE 802.11b DSSS Radios
- Wireless LANs
- HomeRF
- 2.4GHz Cordless Phones
- 2.4GHz ISM Radios

Features

- 2.4GHz to 2.5GHz Operating Range
- +22.5dBm Linear Output Power (ACPR of <-33dBc 1st-Side Lobe and <-55dBc 2nd-Side Lobe)
- 28.5dB Power Gain
- On-Chip Power Detector
- External Bias Control for Current Throttleback
- +2.7V to +3.6V Single-Supply Operation
- 0.5µA Shutdown Mode
- Tiny Chip-Scale Package (1.5mm × 2.0mm)

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
<th>TOP MARK</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX2242EBC-T</td>
<td>-40°C to +85°C</td>
<td>3 x 4 UCSP</td>
<td>AAE</td>
</tr>
</tbody>
</table>

Pin Configuration

Typical Application Circuit appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.
**2.4GHz to 2.5GHz Linear Power Amplifier**

**ABSOLUTE MAXIMUM RATINGS**

VCC1, VCC2 to GND (no RF signal applied) ........0.3V to +5.5V
RF Input Power ......................................................+10dBm
SHDN, BIAS, PD_OUT, RF_OUT .........................-0.3V to (VCC + 0.3V)
DC Input Current at RF_IN Port ....................-1mA to +1mA
Maximum VSWR Without Damage ......................10:1
Continuous Power Dissipation (TA = +85°C) 3×4 UCSP (derate 80mW/°C above +85°C) ..........1.6W
Operating Temperature Range .....................-40°C to +85°C
Thermal Resistance .............................................25°C/W
Junction Temperature .........................................+150°C
Storage Temperature Range .......................-65°C to +125°C
Lead Temperature (soldering, 10s) ...................+260°C
Continuous Operating Lifetime .................10yrs × 0.92^(TA - 60°C)
(For Operating Temperature, TA ≥ +60°C)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION! ESD SENSITIVE DEVICE**

**DC ELECTRICAL CHARACTERISTICS**

(VCC = +2.7V to +3.6V, fIN = 2.4GHz to 2.5GHz, V SHDN = VCC, RF_IN = RF_OUT = connected to 50Ω load, TA = -40°C to +85°C. Typical values are measured at VCC = +3.3V, fIN = 2.45GHz, TA = +25°C, unless otherwise noted.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.7 V</td>
<td>3.6 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>POUT = +22dBm, VCC = +3.3V, idle current = 280mA</td>
<td></td>
<td></td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>POUT = +13dBm, idle current = 55mA</td>
<td></td>
<td></td>
<td>90</td>
<td></td>
</tr>
<tr>
<td></td>
<td>POUT = +5dBm, idle current = 25mA</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>V SHDN = 0, no RF input</td>
<td>0.5</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Logic Input Voltage High</td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Voltage Low</td>
<td></td>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Logic Input Current High</td>
<td></td>
<td></td>
<td>-1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Logic Input Current Low</td>
<td></td>
<td></td>
<td>-1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
# AC ELECTRICAL CHARACTERISTICS

(MAX2242 Evaluation Kit, V\textsubscript{CC} = +3.3V, V\textsubscript{SHDN} = V\textsubscript{CC}, 50\Omega source and load impedance, f\textsubscript{IN} = 2.45GHz, T\textsubscript{A} = +25°C, unless otherwise noted.) (Note 6)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range (Notes 3, 4)</td>
<td>T\textsubscript{A} = +25°C</td>
<td>2.4</td>
<td>2.5</td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td></td>
<td>T\textsubscript{A} = -40°C to +85°C</td>
<td>26.5</td>
<td>28.5</td>
<td>25.5</td>
<td>dB</td>
</tr>
<tr>
<td>Power Gain (Notes 1, 3)</td>
<td>TA = 25°C</td>
<td>25.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature (Note 3)</td>
<td>T\textsubscript{A} = -40°C to +85°C</td>
<td>±1.2</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over VCC (±10%) (Note 3)</td>
<td>V\textsubscript{CC} = +3.0V to +3.6V</td>
<td>±0.3</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Power (Notes 3, 5, 8)</td>
<td>ACPR, &lt; -55dBc</td>
<td>21.5</td>
<td>22.5</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>PIN = +5dBm</td>
<td>26.5</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Harmonic Output (2f, 3f, 4f)</td>
<td></td>
<td>-40</td>
<td></td>
<td></td>
<td>dBC</td>
</tr>
<tr>
<td>Input VSWR</td>
<td>Over full PIN range</td>
<td></td>
<td>1.5:1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output VSWR</td>
<td>Over full P\textsubscript{OUT} range</td>
<td></td>
<td>2.5:1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Ramp Turn-On Time (Note 7)</td>
<td>SHDN from low to high</td>
<td>1</td>
<td>1.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Power Ramp Turn-Off Time (Note 7)</td>
<td>SHDN from high to low</td>
<td>1</td>
<td>1.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>RF Output Detector Response Time</td>
<td></td>
<td>2.5</td>
<td>5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>RF Output Detector Voltage</td>
<td>PIN = +22dBm (Note 9)</td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>PIN = +13dBm (Note 9)</td>
<td>0.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PIN = +5dBm (Note 9)</td>
<td>0.55</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Specifications over T\textsubscript{A} = -40°C to +85°C are guaranteed by design. Production tests are performed at T\textsubscript{A} = +25°C.

**Note 2:** Idle current is controlled by external DAC for best efficiency over the entire output power range.

**Note 3:** Parameter measured with RF modulation based on IEEE 802.11b standard.

**Note 4:** Power gain is guaranteed over this frequency range. Operation outside this range is possible, but is not guaranteed.

**Note 5:** Output two-tone third-order intercept point (OIP3) is production tested at T\textsubscript{A} = +25°C. The OIP3 is tested with two signals at f\textsubscript{1} = 2.450GHz and f\textsubscript{2} = 2.451GHz with fixed PIN.

**Note 6:** Min/max limits are guaranteed by design and characterization.

**Note 7:** The total turn-on and turn-off times required for PA output power to settle to within 0.5dB of the final value.

**Note 8:** Excludes PC board loss of approximately 0.15dB.

**Note 9:** See Typical Operating Characteristics for statistical variation.
2.4GHz to 2.5GHz
Linear Power Amplifier

Typical Operating Characteristics
(VCC = +3.3V, fIN = 2.45MHz, RF modulation = IEEE 802.11b, VSHDN = VCC, TA = +25°C, unless otherwise noted.)

- **GAIN vs. SUPPLY VOLTAGE**
  - P0 = +22dBm
  - TA = 40°C
  - TA = 25°C
  - TA = 85°C

- **ICC vs. SUPPLY VOLTAGE**
  - P0 = +22dBm
  - TA = 40°C
  - TA = 25°C
  - TA = 85°C
  - Idle current set to 280mA at VCC = +3.3V, TA = +25°C

- **OUTPUT POWER vs. INPUT POWER**

- **ACPR vs. OUTPUT POWER**
  - POUT = +22 dBm

- **ACPR vs. FREQUENCY**
  - POUT = +22 dBm

- **ICC vs. FREQUENCY**

- **POWER DETECTOR VOLTAGE vs. OUTPUT POWER**
  - VCC = +2.7V, TA = +25°C
  - VCC = +3.0V, TA = +25°C
  - VCC = +3.1V, TA = +85°C
  - VCC = +3.3V, TA = +85°C
  - VCC = +3.6V, TA = +40°C
  - VCC = +3.9V, TA = +85°C

- **OUTPUT POWER HISTOGRAM AT FIXED 1.6V POWER DETECTOR VOLTAGE**
  - SIGMA = 0.14dBm
  - Based on 100 parts
MAX2242

2.4GHz to 2.5GHz Linear Power Amplifier

Typical Operating Characteristics (continued)

\( V_{CC} = +3.3V \), \( f_{IN} = 2.45MHz \), RF modulation = IEEE 802.11b, \( V_{SHDN} = V_{CC} \), \( T_A = +25^\circ C \), unless otherwise noted.

**Output Power Histogram at Fixed 0.8V Power Detector Voltage**

\( \sigma = 0.25 \) dBm

Based on 100 Parts

**Output Power Histogram at Fixed 0.5V Power Detector Voltage**

\( \sigma = 0.75 \) dBm

Based on 100 Parts

**S11, S22, vs. Frequency**

\( P_{IN} = -15dBm \)

**S21 vs. Frequency**

\( P_{IN} = -15dBm \)
**Detailed Description**

The MAX2242 is a linear PA intended for 2.4GHz ISM-band wireless LAN applications. The PA is fully characterized in the 2.4GHz to 2.5GHz ISM band. The PA consists of two driver stages and an output stage. The MAX2242 also features an integrated power detector and power shutdown control mode.

**Dynamic Power Control**

The MAX2242 is designed to provide optimum power-added efficiency (PAE) in both high and low power applications. For a +3.3V supply at high output power level, the output power is typically +22.5dBm with an idle current of 280mA. At low output-power levels, the DC current can be reduced by an external DAC to increase PAE while still maintaining sufficient ACPR performance. This is achieved by using external resistors connected to the BIAS pin to set the bias currents of the driver and output stages. The resistors are typically 8kΩ. Typically, a DAC voltage of 1.0V will give a 280mA bias current. Increasing the DAC voltage will decrease the idle current. Similarly, decreasing the DAC voltage will increase the idle current.

The BIAS pin is maintained at a constant voltage of 1.0V, allowing the user to set the desired idle current using only two off-chip 1% resistors: a shunt resistor, R2, from BIAS to ground; and a series resistor, R1, to the DAC voltage, as shown in the *Typical Application Circuit*. Resistor values R1 and R2 are determined as follows:

\[
V_{\text{MAX}} = 1.0 + (1.0 \times R_1) / R_2; \\
(I_{\text{CC}} = 0, V_{\text{DAC}} = V_{\text{MAX}}) \quad (1)
\]

\[
I_{\text{MAX}} = (1.0 \times 1867) \times (R_1 + R_2) / (R_1 \times R_2); \\
(I_{\text{CC}} = I_{\text{MAX}} = \text{max value, } V_{\text{DAC}} = 0) \quad (2)
\]

\[
I_{\text{DAC}} = (V_{\text{DAC}} - 1.0) / R_1 \quad (3)
\]

\[
I_{\text{MID}} = (1.0 \times 1867) / R_2; \\
(V_{\text{DAC}} = 1.0V \text{ or floating}) \quad (4)
\]

\[
I_{\text{CC}} = 1867 \times I_{\text{BIAS}} \quad (5)
\]

where

- \(V_{\text{MAX}}\) is the maximum DAC voltage
- \(I_{\text{MAX}}\) is the maximum idle current
- \(I_{\text{MID}}\) is the idle current with \(V_{\text{DAC}} = 1.0V\) or not connected
- \(V_{\text{DAC}}\) is the DAC voltage
- \(I_{\text{DAC}}\) is the DAC current

If no DAC is used and a constant idle current is desired, use equation 4 to determine the resistor values for a given total bias current. Only R2 is required.

---

**Pin Description**

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>GND</td>
<td>3rd Stage Ground. Refer to Application Information section for detailed PC-board layout information.</td>
</tr>
<tr>
<td>A2</td>
<td>VCC2</td>
<td>2nd Stage Supply Voltage. Bypass to ground using configuration in the typical operating circuit.</td>
</tr>
<tr>
<td>A3</td>
<td>GND</td>
<td>3rd Stage Ground. Refer to Application Information section for detailed PC-board layout information.</td>
</tr>
<tr>
<td>A4</td>
<td>VCC1</td>
<td>1st Stage Supply Voltage. Bypass to ground using configuration in the typical operating circuit.</td>
</tr>
<tr>
<td>B1</td>
<td>RF_OUT</td>
<td>RF Output. Requires external matching.</td>
</tr>
<tr>
<td>B2</td>
<td>PD_OUT</td>
<td>Power Detector Output. This output is a DC voltage indicating the PA output power. Connect a 47kΩ resistor to GND.</td>
</tr>
<tr>
<td>B4</td>
<td>GND</td>
<td>1st Stage and Bias Control Circuit Ground</td>
</tr>
<tr>
<td>C1</td>
<td>BIAS</td>
<td>Bias Control. Connect one 8kΩ resistor from BIAS to GND and one 8kΩ resistor from BIAS to DAC block to set the idle current.</td>
</tr>
<tr>
<td>C2</td>
<td>SHDN</td>
<td>Shutdown Input. Drive logic low to place the device in shutdown mode. Drive logic high for normal operation.</td>
</tr>
<tr>
<td>C3</td>
<td>VCCB</td>
<td>Bias Circuit DC Supply Voltage. Bypass to ground using configuration in the typical operating circuit.</td>
</tr>
<tr>
<td>C4</td>
<td>RF_IN</td>
<td>RF Input. Requires external matching.</td>
</tr>
</tbody>
</table>
For a DAC capable of both sourcing and sinking currents, the full voltage range of the DAC (typically from 0 to +3V) can be used. By substituting the desired values of $V_{\text{MAX}}$ and $I_{\text{MAX}}$ into equations 1 and 2, $R_1$ and $R_2$ can be easily calculated.

For a DAC capable of sourcing current only, use equation 4 to determine the value of resistor $R_2$ for the desired maximum current. Use equation 1 to determine the value of resistor $R_1$ for the desired minimum current.

For a DAC capable of sinking current only, set resistors $R_1$ and $R_2$ to 0 and connect the DAC directly to the BIAS pin. Use equation 5 to determine the DAC current required for a given $I_{\text{CC}}$.

**Shutdown Mode**

Apply logic low to $\text{SHDN}$ (pin C2) to place the MAX2242 into shutdown mode. In this mode, all gain stages are disabled and supply current typically drops to 0.5µA. Note that the shutdown current is lowest when $V_{\text{SHDN}} = 0$.

**Power Detector**

The power detector generates a voltage proportional to the output power by monitoring the output power using an internal coupler. It is fully temperature compensated and allows the user to set the bandwidth with an external capacitor. For maximum bandwidth, connect a 47kΩ resistor from PD_OUT to GND and do not use any external capacitor.

Applications Information

**Interstage Matching and Bypassing**

$V_{\text{CC1}}$ and $V_{\text{CC2}}$ provide bias to the first and second stage amplifiers, and are also part of the interstage matching networks required to optimize performance between the three amplifier stages. See the Typical Application Circuit for the lumped and discrete component values used on the MAX2242 EV kit for optimum interstage matching and RF bypassing. In addition to RF bypass capacitors on each bias line, a global bypass capacitor of 22µF is necessary to filter any noise on the supply line. Route separate $V_{\text{CC}}$ bias paths from the global bypass capacitor (star topology) to avoid coupling between PA stages. Use the MAX2242 EV kit PC board layout as a guide.

**External Matching**

The RFIN port requires a matching network. The RFIN port impedance is 16–j30 at 2.45GHz. See the Typical Application Circuit for recommended component values.

The RFOUT port is an open-collector output that must be pulled to $V_{\text{CC}}$ through a 10nH RF choke for proper biasing. A shunt 33pF capacitor to ground is required at the supply side of the inductor. In addition, a matching network is required for optimum gain, efficiency, ACPR, and output power. The load impedance seen at the RFOUT port of the MAX2242 on the EV kit is approximately 8 + j5Ω. This should serve as a good starting point for your layout. However, optimum performance is layout dependent and some component optimization may be required. See the Typical Application Circuit for the lumped and discrete component values used on the MAX2242 EV kit to achieve this impedance.

**Ground Vias**

Placement and type of ground vias are important to achieve optimum gain and output power and ACPR performance. Each ground pin requires its own through-hole via (via diameter = 10mils) placed as near as possible to the device pin as possible to reduce ground inductance and feedback between stages. Use the MAX2242 EV kit PC board layout as a guide.

**Layout and Thermal Management Issues**

The MAX2242 EV kit serves as a layout guide. Use controlled-impedance lines on all high-frequency inputs and outputs. The GND pins also serve as heat sinks. Connect all GND pins directly to the topside RF ground. On boards where the ground plane is not on the component side, connect all GND pins to the ground plane with plated multiple throughholes close to the package. PC board traces connecting the GND pins also serve as heat sinks. Make sure that the traces are sufficiently wide.

**UCSP Reliability**

UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user’s assembly methods, circuit-board material, and usage environment. The user should closely review these areas when considering use of a UCSP. Performance through the operating-life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSPs are attached through direct solder contact to the user’s PC board, foregoing the inherent stress relief of a packaged-product lead frame. Solder joint contact integrity must be considered. Testing done to characterize the
UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Users should also be aware that as with any interconnect system there are electromigration-based current limits that, in this case, apply to the maximum allowable current in the bumps. Reliability is a function of this current, the duty cycle, lifetime, and bump temperature. See the Absolute Maximum Ratings section for any specific limitations listed under Continuous Operating Lifetime. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

Chip Information

TRANSISTOR COUNT: 486
2.4GHz to 2.5GHz
Linear Power Amplifier

Package Information
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

Note: MAX2242 does not use bump B3.