General Description
The MAX22245/MAX22246 are a family of 2-channel reinforced, fast, low-power digital galvanic isolators using Maxim’s proprietary process technology. These devices transfer digital signals between circuits with different power domains, using as little as 0.76mW per-channel at 1Mbps (1.8V supply). All of the devices in the family feature reinforced isolation for a withstand voltage rating of 5kVRMS for 60 seconds.

The MAX22245 features two channels transferring data in the same direction. The two channels of the MAX22246 transfer data in opposite directions, and this makes the MAX22246 ideal for isolating the Tx and Rx lines of a transceiver.

Devices are available with a maximum data rate of 25Mbps or 200Mbps, and with outputs that are either default high or default low. The default is the state the output assumes when the input is either not powered or is open circuit. See the Ordering Information and Product Selector Guide for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX22245/MAX22246 family is available in an 8-pin wide-body SOIC package with 8mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400, which gives it a group II rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Applications
• Isolated RS232, RS485/RS-422, CAN
• General Isolation Applications
• Fieldbus Communications for Industrial Automation
• Medical Systems
• Motor Drive

Benefits and Features
• Reinforced Galvanic Isolation for Fast Digital Signals
  • Wide-Body 8-Pin SOIC with 8mm of Creepage and Clearance
  • Up to 200Mbps Maximum Data Rate
  • Withstands 5kVRMS for 60s (VISO)
  • Continuously Withstands 1500VRMS (VIOWM)
  • Withstands ±10kV Surge Between GNDA and GNDB with 1.2/50μs Waveform
  • High CMTI (50kV/μs, typ)
• Low Power Consumption
  • 0.76mW per Channel at 1Mbps with VDD = 1.8V
  • 1.42mW per Channel at 1Mbps with VDD = 3.3V
  • 3.2mW per Channel at 100Mbps with VDD = 1.8V
• Options to Support a Broad Range of Applications
  • 2 Maximum Data Rates (200Mbps, 25Mbps)
  • 2 Channel Direction Configurations
  • 2 Output Default States (High or Low)

Safety Regulatory Approvals
• UL According to UL1577
• cUL According to CSA Bulletin 5A
• VDE 0884-11 Reinforced Insulation (Pending)

MAX22245/MAX22246

Reinforced, Fast, Low-Power,
Two-Channel Digital Isolators

Functional Diagram

![Functional Diagram of MAX22245 and MAX22246](image-url)
Absolute Maximum Ratings

V_{DDA} to GNDA ........................................... -0.3V to +6V
V_{DDB} to GNDB ........................................... -0.3V to +6V
IN_ on Side A to GNDA ................................... -0.3V to +6V
IN_ on Side B to GNDB ................................... -0.3V to +6V
OUT_ on Side A to GNDA .................. -0.3V to (V_{DDA} + 0.3V)
OUT_ on Side B to GNDB .................. -0.3V to (V_{DDB} + 0.3V)

Short-Circuit Continuous Current
OUT_ on Side A to GNDA .............. ±30mA
OUT_ on Side B to GNDB .............. ±30mA

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 11.35mW/°C above +70°C) ... 908.1mW

Temperature Ratings
Operating Temperature Range .................. -40°C to +125°C
Maximum Junction Temperature .................. +150°C
Storage Temperature Range .................. -60°C to +150°C
Lead Temperature (soldering, 10s) .............. +300°C
Soldering Temperature (reflow) .............. +260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Wide SOIC

<table>
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<tr>
<th>Package Code</th>
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<tr>
<td>Outline Number</td>
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</tr>
<tr>
<td>Land Pattern Number</td>
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THERMAL RESISTANCE, FOUR-LAYER BOARD

| Junction-to-Ambient (θ_{JA}) | 88.1°C/W       |
| Junction-to-Case Thermal Resistance (θ_{JC}) | 42.4°C/W       |

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.
### MAX22245/MAX22246 Reinforced, Fast, Low-Power, Two-Channel Digital Isolators

**Electrical Characteristics**

(V<sub>DDA</sub> - V<sub>GNDA</sub> = 1.71V to 5.5V, V<sub>DDB</sub> - V<sub>GNDB</sub> = 1.71V to 5.5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>DDA</sub> - V<sub>GNDA</sub> = 3.3V, V<sub>DDB</sub> - V<sub>GNDB</sub> = 3.3V, V<sub>GNDA</sub> = V<sub>GNDB</sub>, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 3)

<table>
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<tr>
<th>PARAMETER</th>
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<th>CONDITIONS</th>
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<th>TYP</th>
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<th>UNITS</th>
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<td>5.5</td>
<td></td>
<td>V</td>
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<tr>
<td>V&lt;sub&gt;DDB&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DDB&lt;/sub&gt;</td>
<td>Relative to GNDB</td>
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<td>V&lt;sub&gt;UVLO&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; _rising</td>
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<td>1.6</td>
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**MAX22245 SUPPLY CURRENT (Note 2)**

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<th>TYP</th>
<th>MAX</th>
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<td>mA</td>
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<tr>
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**MAX22246 SUPPLY CURRENT (Note 2)**

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<th>UNITS</th>
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<td>Side A Supply Current</td>
<td>I&lt;sub&gt;DDA&lt;/sub&gt;</td>
<td>500kHz square wave, C&lt;sub&gt;L&lt;/sub&gt; = 0pF</td>
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<td>mA</td>
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<tr>
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<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 5V</td>
<td>0.46</td>
<td>0.84</td>
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<td>50MHz square wave, C&lt;sub&gt;L&lt;/sub&gt; = 0pF</td>
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<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 2.5V</td>
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<td>0.74</td>
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</table>
**MAX22245/MAX22246**

**Reinforced, Fast, Low-Power, Two-Channel Digital Isolators**

$(V_{DDA} - V_{GND_A} = 1.71\text{V to } 5.5\text{V}, V_{DDB} - V_{GND_B} = 1.71\text{V to } 5.5\text{V}, C_L = 15pF, T_A = -40^\circ\text{C to } +125^\circ\text{C}, \text{unless otherwise noted. Typical values are at } V_{DDA} - V_{GND_A} = 3.3\text{V, } V_{DDB} - V_{GND_B} = 3.3\text{V, } V_{GND_A} = V_{GND_B}, T_A = +25^\circ\text{C, unless otherwise noted.}) (Notes 1, 3)\)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
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**LOGIC INTERFACE (IN_, OUT_)**

| Input High Voltage | $V_{IH}$ | $2.25V \leq V_{DD_} \leq 5.5V$ | 0.7 x $V_{DBD}$ | V |
|                   |         | $1.71V \leq V_{DD_} < 2.25V$    | 0.75 x $V_{DBD}$ |   |
| Input Low Voltage | $V_{IL}$ | $2.25V \leq V_{DD_} \leq 5.5V$ | 0.8             | V |
|                   |         | $1.71V \leq V_{DD_} < 2.25V$    | 0.7             |   |
| Input Hysteresis  | $V_{HYS}$ | MAX2224_B/E                      | 410            | mV |
|                   |         | MAX2224_C/F                      | 80             |   |
| Input Pullup Current | $I_{PU}$ | MAX2224_B/C                      | -10            | µA |
|                   |         | MAX2224_E/F                      | 1.5            |     |
| Input Pulldown Current | $I_{PD}$ |         | 5              | µA |
|                   |         | 10                          | 2              | pF |
| Output Voltage High | $V_{OH}$ | $I_{OUT} = -4mA$ source         | $V_{DD} - 0.4$ | V |
| Output Voltage Low  | $V_{OL}$ | $I_{OUT} = 4mA$ sink            | 0.4            | V |

**Dynamic Characteristics MAX2224_B/E**

$(V_{DDA} - V_{GND_A} = 1.71\text{V to } 5.5\text{V}, V_{DDB} - V_{GND_B} = 1.71\text{V to } 5.5\text{V}, C_L = 15pF, T_A = -40^\circ\text{C to } +125^\circ\text{C}, \text{unless otherwise noted. Typical values are at } V_{DDA} - V_{GND_A} = 3.3\text{V, } V_{DDB} - V_{GND_B} = 3.3\text{V, } V_{GND_A} = V_{GND_B}, T_A = +25^\circ\text{C, unless otherwise noted.}) (Notes 2, 4)\)**

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<td>Common-Mode Transient Immunity</td>
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<tr>
<td>Pulse Width Distortion</td>
<td>$PWD$</td>
<td>$I_{PLH} \cdot I_{PHL}$</td>
<td>4.5V</td>
<td>5.5V</td>
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</table>

(Needed image)
Maxim Integrated | 6

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Maxim, Incorporated

MAX22245/MAX22246

Reinforced, Fast, Low-Power, Two-Channel Digital Isolators

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>Propagation Delay Skew Part-to-Part (Same Channel)</td>
<td>t_{SPHL}</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>14.0</td>
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<tr>
<td>Propagation Delay Skew Channel-to-Channel (Same Direction) (Figure 1)</td>
<td>t_{SCSLH}</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
<td>4</td>
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<tr>
<td>Propagation Delay Skew Channel-to-Channel (Opposite Direction)</td>
<td>t_{SCOHL}</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
<td>1.71V ≤ V_{DD} ≤ 5.5V</td>
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<tr>
<td>Peak Eye Diagram Jitter</td>
<td>t_{JIT(PK)}</td>
<td>25Mbps</td>
<td>250</td>
<td>ps</td>
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<tbody>
<tr>
<td>Rise Time (Figure 1)</td>
<td>t_R</td>
<td>C_L = 5pF</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
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<tr>
<td>Fall Time (Figure 1)</td>
<td>t_F</td>
<td>C_L = 5pF</td>
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<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
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Dynamic Characteristics MAX2224_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

<table>
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<tr>
<td>Common-Mode Transient Immunity</td>
<td>CMTI</td>
<td>(Note 5)</td>
<td>50</td>
<td>kV/µs</td>
<td></td>
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<tr>
<td>Maximum Data Rate</td>
<td>D_{RMAX}</td>
<td>2.25V ≤ V_{DD} ≤ 5.5V</td>
<td>200</td>
<td>Mbps</td>
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<tr>
<td>Minimum Pulse Width</td>
<td>P_{WMIN}</td>
<td>2.25V ≤ V_{DD} ≤ 5.5V</td>
<td>5</td>
<td>ns</td>
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www.maximintegrated.com
(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}; T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

<table>
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<tr>
<th>PARAMETER</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Propagation Delay</td>
<td>t_{PLH}</td>
<td>IN_ to OUT_, C_L = 15pF</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>4.4</td>
<td>6.2</td>
<td>9.5</td>
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<td></td>
<td></td>
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<td>3.0V ≤ V_{DD} ≤ 3.6V</td>
<td>4.8</td>
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<td>11.2</td>
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<td></td>
<td></td>
<td></td>
<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
<td>5.3</td>
<td>8.3</td>
<td>14.7</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
<td>7.1</td>
<td>12.3</td>
<td>22.1</td>
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<td>Pulse Width Distortion</td>
<td>PWE</td>
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<td></td>
<td></td>
<td></td>
<td>3.0V ≤ V_{DD} ≤ 3.6V</td>
<td>0.4</td>
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<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
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<td>2</td>
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<td></td>
<td></td>
<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
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<td>2</td>
<td></td>
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<td>t_{SPLH}</td>
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<tr>
<td>Skew Part-to-Part</td>
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<td>3.0V ≤ V_{DD} ≤ 3.6V</td>
<td>4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Same Channel)</td>
<td></td>
<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
<td>6.9</td>
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<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
<td>12.1</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>t_{SPHL}</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>4.0</td>
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<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
<td>7.0</td>
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<tr>
<td></td>
<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
<td>11.8</td>
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<tr>
<td>Propagation Delay</td>
<td>t_{SCSLH}</td>
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<tr>
<td>Skew Channel-to-Channel</td>
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<tr>
<td>(Same Direction)</td>
<td>t_{SCSHL}</td>
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<td></td>
<td>t_{SCOLH}</td>
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<tr>
<td></td>
<td>t_{SCOHL}</td>
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<tr>
<td>Peak Eye Diagram Jitter</td>
<td>t_{JIT(PK)}</td>
<td>200Mbps</td>
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<td>100</td>
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<tr>
<td>Clock Jitter RMS</td>
<td>t_{CLK(RMS)}</td>
<td>500kHz clock input, rising/falling edges</td>
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<td>7.5</td>
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<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>t_{R}</td>
<td>C_L = 5pF</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
<td>0.8</td>
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<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>3.0V ≤ V_{DD} ≤ 3.6V</td>
<td>1.1</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
<td>1.5</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
<td>2.4</td>
<td></td>
<td></td>
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<tr>
<td>Fall Time</td>
<td>t_{F}</td>
<td>C_L = 5pF</td>
<td>4.5V ≤ V_{DD} ≤ 5.5V</td>
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</tbody>
</table>
Maxim Integrated | 8

MAX22245/MAX22246

Reinforced, Fast, Low-Power, Two-Channel Digital Isolators

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
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<td></td>
<td></td>
<td>3.0V ≤ V_{DD} ≤ 3.6V</td>
<td>1.4</td>
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<td>2.25V ≤ V_{DD} ≤ 2.75V</td>
<td>1.9</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>1.71V ≤ V_{DD} ≤ 1.89V</td>
<td>3</td>
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</tr>
</tbody>
</table>

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

Test Circuit and Timing Diagram

![Test Circuit](image)

Figure 1. Test Circuit (A) and Timing Diagram (B)
## Table 1. Insulation Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
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<th>VALUE</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Partial Discharge Test Voltage</td>
<td>$V_{PR}$</td>
<td>Method B1 = $V_{IORM} \times 1.875$ (t = 1s, partial discharge &lt; 5pC)</td>
<td>3977</td>
<td>$V_P$</td>
</tr>
<tr>
<td>Maximum Repetitive Peak Isolation</td>
<td>$V_{IORM}$</td>
<td>(Note 6)</td>
<td>2121</td>
<td>$V_P$</td>
</tr>
<tr>
<td>Maximum Working Isolation Voltage</td>
<td>$V_{IOWM}$</td>
<td>Continuous RMS voltage (Note 6)</td>
<td>1500</td>
<td>$V_{RMS}$</td>
</tr>
<tr>
<td>Maximum Transient Isolation Voltage</td>
<td>$V_{IOTM}$</td>
<td>$t = 1s$ (Note 6)</td>
<td>8000</td>
<td>$V_P$</td>
</tr>
<tr>
<td>Maximum Withstanding Isolation Voltage</td>
<td>$V_{ISO}$</td>
<td>$f_{SW} = 60Hz$, duration = 60s (Notes 6, 7)</td>
<td>5000</td>
<td>$V_{RMS}$</td>
</tr>
<tr>
<td>Maximum Surge Isolation Voltage</td>
<td>$V_{IOSM}$</td>
<td>Reinforced Insulation, test method per IEC 60065, $V_{TEST} = 1.6 \times V_{IOSM} = 10000V_{PEAK}$ (Note 9)</td>
<td>6250</td>
<td>$V_P$</td>
</tr>
<tr>
<td>Isolation Resistance</td>
<td>$R_{IO}$</td>
<td>$V_{IO} = 500V$, $T_A = 25^\circ C$</td>
<td>$&gt; 10^{12}$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} = 500V$, $100^\circ C \leq T_A \leq 125^\circ C$</td>
<td>$&gt; 10^{11}$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IO} = 500V$, $T_S = 150^\circ C$</td>
<td>$&gt; 10^9$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>Barrier Capacitance Side A to Side B</td>
<td>$C_{IO}$</td>
<td>$f_{SW} = 1MHz$ (Note 8)</td>
<td>1.5</td>
<td>$pF$</td>
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<tr>
<td>Minimum Creepage Distance</td>
<td>CPG</td>
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<td>8</td>
<td>mm</td>
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<tr>
<td>Minimum Clearance Distance</td>
<td>CLR</td>
<td></td>
<td>8</td>
<td>mm</td>
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<td>Internal Clearance</td>
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<td>Distance through insulation</td>
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<td>CTI</td>
<td>Material Group II (IEC 60112)</td>
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<td>Climate Category</td>
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<td>40/125/21</td>
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<td>Pollution Degree (DIN VDE 0110, Table 1)</td>
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</table>

**Note 6:** $V_{ISO}$, $V_{IOTM}$, $V_{IOWM}$, and $V_{IORM}$ are defined by the IEC 60747-5-5 standard.

**Note 7:** Product is qualified at $V_{ISO}$ for 60s and 100% production tested at 120% of $V_{ISO}$ for 1s.

**Note 8:** Capacitance is measured with all pins on field-side and logic-side tied together.

**Note 9:** Devices are immersed in oil during surge characterization.
**Safety Regulatory Approvals**

**UL**
The MAX22245/MAX22246 are certified under UL1577. For more details, refer to File E351759.

Rated up to \(5000V_{\text{RMS}}\) isolation voltage for single protection.

**cUL (Equivalent to CSA notice 5A)**
The MAX22245/MAX22246 are certified up to \(5000V_{\text{RMS}}\) for single protection. For more details, refer to File E351759.

**VDE (Pending)**
The MAX22245/MAX22246 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 8000\(V_{\text{PK}}\), Maximum Repetitive Peak Isolation Voltage 2121\(V_{\text{PK}}\).

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

**Typical Operating Characteristics**

\((V_{\text{DDA}} \cdot V_{\text{GNDA}} = +3.3\text{V}, V_{\text{DDB}} \cdot V_{\text{GNDB}} = +3.3\text{V}, V_{\text{GNDA}} = V_{\text{GNDB}}, T_{A} = +25^\circ\text{C}, \text{unless otherwise noted.})\)

---

**SIDE A SUPPLY CURRENT vs. DATA RATE**

<table>
<thead>
<tr>
<th>DATA RATE (Mbps)</th>
<th>SUPPLY CURRENT (mA)</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0.7</td>
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<tr>
<td>5</td>
<td>0.6</td>
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<tr>
<td>10</td>
<td>0.5</td>
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<tr>
<td>15</td>
<td>0.4</td>
</tr>
<tr>
<td>20</td>
<td>0.3</td>
</tr>
<tr>
<td>25</td>
<td>0.2</td>
</tr>
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</table>

\(V_{\text{DDA}} = 1.8\text{V}, 2.5\text{V}, 3.3\text{V}, 5.0\text{V}\)

**SIDE B SUPPLY CURRENT vs. DATA RATE**

<table>
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<tr>
<th>DATA RATE (Mbps)</th>
<th>SUPPLY CURRENT (mA)</th>
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<tbody>
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<td>0</td>
<td>0.6</td>
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<tr>
<td>5</td>
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<td>10</td>
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<td>15</td>
<td>0.1</td>
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<td>20</td>
<td>0.06</td>
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\(V_{\text{DDA}} = 1.8\text{V}, 2.5\text{V}, 3.3\text{V}, 5.0\text{V}\)
### MAX22245/MAX22246

**Pin Configurations**

**TOP VIEW**

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<thead>
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<th>Pin</th>
<th>VDDA</th>
<th>IN1</th>
<th>OUT1</th>
<th>IN2</th>
<th>OUT2</th>
<th>GNDA</th>
<th>VDDB</th>
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<td>7</td>
<td>3</td>
<td>6</td>
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<tr>
<td>MAX22246</td>
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<td>3</td>
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<td>4</td>
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</table>

**WIDE SOIC**

### Pin Descriptions

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<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
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<td>MAX22246</td>
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</tr>
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<td>1</td>
<td>VDDA</td>
<td>Power Supply Input for Side A. Bypass VDDA to GNDA with a 0.1µF ceramic capacitor as close as possible to the pin.</td>
</tr>
<tr>
<td>2</td>
<td>IN1</td>
<td>Logic Input 1 on Side A</td>
</tr>
<tr>
<td>—</td>
<td>OUT1</td>
<td>Logic Output 1 on Side A</td>
</tr>
<tr>
<td>3</td>
<td>IN2</td>
<td>Logic Input 2 on Side A</td>
</tr>
<tr>
<td>4</td>
<td>GNDA</td>
<td>Ground Reference for Side A</td>
</tr>
<tr>
<td>5</td>
<td>GNDB</td>
<td>Ground Reference for Side B</td>
</tr>
<tr>
<td>6</td>
<td>OUT2</td>
<td>Logic Output 2 on Side B</td>
</tr>
<tr>
<td>7</td>
<td>—</td>
<td>OUT1</td>
</tr>
<tr>
<td>—</td>
<td>IN1</td>
<td>Logic Input 1 on Side B</td>
</tr>
<tr>
<td>8</td>
<td>VDDB</td>
<td>Power Supply Input for Side B. Bypass VDDB to GNDB with a 0.1µF ceramic capacitor as close as possible to the pin.</td>
</tr>
</tbody>
</table>
Detailed Description
The MAX22245/MAX22246 are a family of 2-channel reinforced digital isolators. The MAX22245/MAX22246 have an isolation rating of 5kV_{RMS}. The MAX22245/MAX22246 family offers two unidirectional channel configurations to accommodate any 2-channel design.

The MAX22245 features two channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX22246 has one channel to transmit data in one direction and the other channel to transmit in the opposite direction, making it ideal for applications such as isolated RS232 or RS485 communication.

Devices are available in an 8-pin wide-body SOIC package with 8mm creepage and clearance and are rated up to 5kV_{RMS}. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with a maximum data rate of either 25Mbps (B/E versions) or 200Mbps (C/F versions). The MAX22245_B/C feature default-high outputs. The MAX2224_E/F feature default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open circuit. The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX22245/MAX22246 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation
The MAX22245/MAX22246 provide reinforced galvanic isolation for digital signals that are transmitted between two ground domains. The devices withstand differences of up to 5kV_{RMS} for up to 60 seconds, and up to 2121V_{PEAK} of continuous isolation.

Level Shifting
The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX22245/MAX22246 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels
Each channel of the MAX22245/MAX22246 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features two unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E versions), or from DC to 200Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout
The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs as seen in Table 2. Figure 2 through Figure 5 show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Condition

<table>
<thead>
<tr>
<th>V_{IN}</th>
<th>V_{DDA}</th>
<th>V_{DDB}</th>
<th>V_{OUTA}</th>
<th>V_{OUTB}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Powered</td>
<td>Powered</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>0</td>
<td>Powered</td>
<td>Powered</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>X</td>
<td>Undervoltage</td>
<td>Powered</td>
<td>Default</td>
<td>Default</td>
</tr>
<tr>
<td>X</td>
<td>Powered</td>
<td>Undervoltage</td>
<td>Default</td>
<td>Default</td>
</tr>
</tbody>
</table>
Safety Limits
Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22245/MAX22246 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and...
result in damage to the isolation barrier, potentially causing downstream issues. Table 3 shows the safety limits for the MAX22245/MAX22246.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the Absolute Maximum Ratings. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_JA) determine the junction temperature. Thermal impedance values (θ_JA and θ_JC) are available in the Package Information section and power dissipation calculations are discussed in the Calculating Power Dissipation section. Calculate the junction temperature (T_J) as:

\[ T_J = T_A + (P_D \times \theta_{JA}) \]

Figure 6 and Figure 7 show the thermal derating curve for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

### Table 3. Safety Limiting Values for the MAX22245/MAX22246

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Safety Current on Any Pin (No Damage to Isolation Barrier)</td>
<td>I_S</td>
<td>T_J = 150°C, T_A = 25°C</td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td>Total Safety Power Dissipation</td>
<td>P_S</td>
<td>T_J = 150°C, T_A = 25°C</td>
<td>1418</td>
<td>mW</td>
</tr>
<tr>
<td>Maximum Safety Temperature</td>
<td>T_S</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>
Applications Information

Power-Supply Sequencing
The MAX22245/MAX22246 do not require special power-supply sequencing. The logic levels are set independently on either side by $V_{DDA}$ and $V_{DDB}$. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling
To reduce ripple and the chance of introducing data errors, bypass $V_{DDA}$ and $V_{DDB}$ with $0.1\mu F$ low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Layout Considerations
The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX22245/MAX22246 free from ground and signal planes. Any galvanic or metallic connection between the Side A and Side B defeats the isolation.

Calculating Power Dissipation
The required current for a given supply ($V_{DDA}$ or $V_{DDB}$) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel’s data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 8 and Figure 9. Note that the data in Figure 8 and Figure 9 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in Figure 8 and Figure 9), which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_D$$

where:

$C_L$ is the load capacitance on the isolator’s output pin.
$f_{SW}$ is the switching frequency (bits per second/2).
$V_D$ is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_D / R_L$$

where:

$I_{RL}$ is the current required to drive the resistive load.
$V_D$ is the supply voltage on the output side of the isolator.
$R_L$ is the load resistance on the isolator’s output pin.

Example (shown in Figure 10): A MAX22246 is operating with $V_{DDA} = 2.5V$, $V_{DDB} = 3.3V$, channel 1 operating at 100Mbps with a 15pF capacitive load, and channel 2 operating at 20Mbps with a 10kΩ resistive load and 50% duty cycle. See Table 4 and Table 5 for $V_{DDA}$ and $V_{DDB}$ supply-current calculation worksheets.

$V_{DDA}$ must supply:

- Channel 1 is an output channel operating at 2.5V and 100Mbps, consuming 0.84mA, estimated from Figure 9.
- Channel 2 is an input channel operating at 2.5V and 20Mbps, consuming 0.35mA, estimated from Figure 8.
- $I_{CL}$ on Channel 1 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.
- Total current for side A = 0.84mA + 0.35mA + 1.875mA = 3.065mA (typ)

**V_{DDA} must supply:**

- Channel 1 is an input channel operating at 3.3V and 100Mbps, consuming 1.16mA, estimated from Figure 8.
- Channel 2 is an output channel operating at 3.3V and 20Mbps, consuming 0.41mA, estimated from Figure 9.
- $I_{RL}$ on Channel 2 for 10kΩ resistor held at 3.3V is 0.165mA.
- Total current for side B = 1.16mA + 0.41mA + 0.165mA = 1.735mA (typ)

---

*Figure 8. Supply Current per Input Channel (Estimated)*

*Figure 9. Supply Current per Output Channel (Estimated)*
Table 4. Side A Supply Current Calculation Worksheet

<table>
<thead>
<tr>
<th>CHANNEL</th>
<th>IN/OUT</th>
<th>DATA RATE (Mbps)</th>
<th>LOAD TYPE</th>
<th>LOAD (pF)</th>
<th>NO LOAD CURRENT (mA)</th>
<th>LOAD CURRENT (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT</td>
<td>100</td>
<td>Capacitive</td>
<td>15</td>
<td>0.84</td>
<td>2.5V x 50MHz x 15pF = 1.875mA</td>
</tr>
<tr>
<td>2</td>
<td>IN</td>
<td>20</td>
<td></td>
<td></td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Total: 3.065mA</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. Side B Supply Current Calculation Worksheet

<table>
<thead>
<tr>
<th>CHANNEL</th>
<th>IN/OUT</th>
<th>DATA RATE (Mbps)</th>
<th>LOAD TYPE</th>
<th>LOAD (kΩ)</th>
<th>NO LOAD CURRENT (mA)</th>
<th>LOAD CURRENT (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN</td>
<td>100</td>
<td>Resistive</td>
<td>10kΩ</td>
<td>1.16</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>OUT</td>
<td>20</td>
<td></td>
<td></td>
<td>0.41</td>
<td>3.3V / 10kΩ x 0.5 = 0.165mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Total: 1.735mA</td>
<td></td>
</tr>
</tbody>
</table>
Typical Application Circuit

Product Selector Guide

MAX2224  5  B  A  W  A  +

- CHANNEL CONFIGURATION
  5: 2/0
  6: 1/1

- MAXIMUM DATA RATE
- DEFAULT OUTPUT
  (SEE TABLE)

- TEMP RANGE: -40°C TO +125°C

- PACKAGE: W SOIC

- PINS: 8

- LEAD-FREE/ROHS COMPLIANT

DEVICE CONFIGURATION | MAX DATA RATE
----------------------|---------------
                      | 25Mbps | 200Mbps
DEFAULT-HIGH OUTPUT  | B       | C       
DEFAULT-LOW OUTPUT   | E       | F       

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### Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CHANNEL CONFIGURATION</th>
<th>DATA RATE (Mbps)</th>
<th>DEFAULT OUTPUT</th>
<th>ISOLATION VOLTAGE (kVRMS)</th>
<th>TEMPERATURE RANGE (°C)</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX22245BAWA+*</td>
<td>2/0</td>
<td>25</td>
<td>High</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
<tr>
<td>MAX22245CAWA+*</td>
<td>2/0</td>
<td>200</td>
<td>High</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
<tr>
<td>MAX22245EAWA+*</td>
<td>2/0</td>
<td>25</td>
<td>Low</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
<tr>
<td>MAX22245FAWA+*</td>
<td>2/0</td>
<td>200</td>
<td>Low</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
<tr>
<td>MAX22246BAWA+*</td>
<td>1/1</td>
<td>25</td>
<td>High</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
<tr>
<td>MAX22246CAWA+*</td>
<td>1/1</td>
<td>200</td>
<td>High</td>
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<td>-40 to +125</td>
<td>8 Wide SOIC</td>
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<tr>
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<td>200</td>
<td>Low</td>
<td>5</td>
<td>-40 to +125</td>
<td>8 Wide SOIC</td>
</tr>
</tbody>
</table>

*Future product—contact Maxim for availability.
+Denotes a lead(Pb)-free/RoHS-compliant package.
Reinforced, Fast, Low-Power, Two-Channel Digital Isolators

Revision History

<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>05/20</td>
<td>Initial release</td>
<td>—</td>
</tr>
<tr>
<td>1</td>
<td>09/20</td>
<td>Updated Dynamic Characteristics MAX2224_B/E, removed pending on UL certification</td>
<td>1, 5, 10</td>
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For pricing, delivery, and ordering information, please visit Maxim Integrated’s online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

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