Absolute Maximum Ratings

SUP, SUPSW1, FB2, EN1, EN2 to AGND ..... -0.3V to 40V
OUT1 to AGND ..... -0.4V to 15V
BIAS, FSYNC, PGOOD1, FB1 to AGND ..... -0.3V to 6V
EXTVCC, COMP, CSP to AGND ..... -0.3V to (BIAS + 0.3V)
DL to PGND2 ..... -0.3V to (BIAS + 0.3V)
LX1 to PGND1 ..... -0.3V to (SUPSW1 + 0.3V)
BST1 to LX1 (Note 1) ..... -0.3V to 6V
PGND1, PGND2 to AGND ..... -0.3V to 0.3V

Continuous Power Dissipation (TQFN (T_A = +70°C, derate 28.6mW/°C above +70°C)) 2286mW
Operating Temperature Range ..... -40°C to 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature(soldering,10s) ..... 300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 28 PIN TQFN	
Package Code	T2855Y+5C
Outline Number	**21-100130**
Land Pattern Number	**90-0027**
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Note 2: Package thermal resistances were obtained using the Evaluation Kit. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{SUP} = V_{SUPSW1} = 14V, $V_{EN\_}$ = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C) (Notes 3 and 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS STEP-DOWN CONVERTERS						
Supply Voltage Range	V_{SUP}	Normal Operation	3.5		36	V
		With preboost after initial start-up condition is satisfied	2.05		36	
Supply Current	I_{IN}	V_{EN1} = V_{EN2} = 0V		1	5	µA
		V_{EN1} = V_{SUP}, V_{OUT1} = 5V, V_{EN2} = 0V, V_{EXTVCC} = 5V, No Switching		10	18	
		V_{EN1} = V_{SUP}, V_{OUT1} = 5V, V_{EN2} = V_{SUP}, V_{EXTVCC} = 5V, V_{FB2} > 1V, No Switching		30		
Buck1 Fixed Output Voltage	V_{OUT1}	V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, PWM mode	4.9	5	5.1	V
		V_{FB1} = V_{BIAS}, V_{OUT1} = 5V, skip mode	4.85	5	5.15	
		V_{FB1} = V_{BIAS}, V_{OUT1} = 3.3V, PWM mode	3.234	3.3	3.366	V
		V_{FB1} = V_{BIAS}, V_{OUT1} = 3.3V, skip mode	3.2	3.3	3.4	
Output Voltage Adjustable Range		Buck1 (Note 5)	1		14	V
Regulated Feedback Voltage	V_{FB1}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB1}	T_A = +25°C		0.01	1	µA
Feedback Line Regulation Error		V_{SUP} = 3.5V to 36V, V_{FB1} = 1V		0.01		%/V
Dead time		Buck1 (Note 5)		3		ns
Maximum Duty Cycle		Buck1	95			%
Minimum On-Time	t_{ON_MIN}	Buck1 (Note 5)		20		ns
PWM Switching Frequency Range	f_{SW}	OTP Option of 400kHz (see the *Ordering Information* for exact part number)		2.1		MHz
Switching Frequency Accuracy			1.9	2.1	2.32	MHz
Current-Limit			4.5	6	7.5	A
Soft-Start Ramp Time		Buck1 fixed soft-start time regardless of frequency.	3	5.5	7	ms
LX1 Leakage Current		V_{SUPSW1} = 6V, V_{LX1} = V_{PGND1} or V_{SUPSW1}, T_A = +25°C		0.001	5	µA
High-Side Switch On Resistance	$R_{ON\_H\_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		50		mΩ
Low-Side Switch On Resistance	$R_{ON\_L\_BUCK1}$	I_{LX1} = 1A, V_{BIAS} = 5V		45		mΩ
PGOOD1 Threshold	V_{PGOOD_H}	% of $V_{OUT\_}$, rising	93	95	97	%
	V_{PGOOD_F}	% of $V_{OUT\_}$, falling	91.5	93.5	95.5	
PGOOD1 Leakage Current		V_{PGOOD1} = 5V, T_A = +25°C		0.01	1	µA
PGOOD1 Output Low Voltage		I_{SINK} = 1mA			0.2	V
PGOOD1, Debounce Time		Fault Detection, Rising and Falling		20		µs
PGOOD1 Assertion Time		PGOOD1 Low to High (Note 5)		0		ms

Electrical Characteristics (continued)

(V_{SUP} = V_{SUPSW1} = 14V, $V_{EN\_}$ = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C) (Notes 3 and 4)

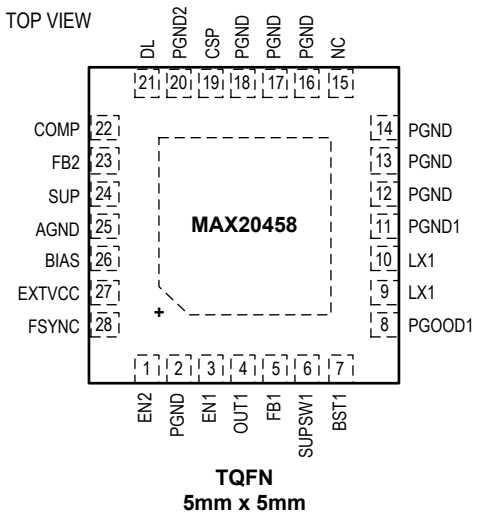
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP CONTROLLER						
Minimum On Time	t_{ONBST}	(Note 5)		60		ns
Minimum Off Time	t_{OFFBST}			60		ns
Current Limit	V_{LIMBST}	V_{CS} - V_{PGND2}	40	50	60	mV
Undervoltage Lockout	UVLO	Input Voltage Rising		4.5		V
DL Pullup Resistance		V_{BIAS} = 5V, I_{DL} = -100mA		3	6	Ω
DL Pulldown Resistance		V_{BIAS} = 5V, I_{DL} = 100mA		1	2	Ω
Boost Feedback Voltage	V_{FB2}	Pre-Boost Feedback Voltage, No Load on Boost Output	0.985	1.005	1.025	V
Transconductance (from FB2 to COMP)	g_{M_BOOST}	V_{FB2} = 1.005V, V_{BIAS} = 5V	130	230	330	µS
Boost Fixed Output Voltage	V_{OUT2}	Contact factory for other available options	9.75	10	10.2	V
Boost Load Regulation Error		PWM Mode, Load from 1mA to 4A		0.05		%/A
FB3 Leakage Current	I_{FB2}	T_A = +25°C		0.01	1	µA
FSYNC INPUT						
FSYNC frequency Range		Minimum sync pulse of 100ns, f_{OSC} = 2.1MHz	1.8		2.6	MHz
		Minimum sync pulse of 1.5µs, f_{OSC} = 400kHz	250		550	kHz
FSYNC Switching Thresholds		High Threshold	1.4			V
		Low Threshold			0.4	
INTERNAL LDO BIAS AND EXTVCC						
Internal BIAS Voltage		V_{SUPSW1} > 6V		5		V
BIAS UVLO Threshold		V_{BIAS} rising		3.1	3.3	V
		V_{BIAS} falling	2.4	2.6		
EXTVCC Operating Range			3.25		5.5	V
EXTVCC Threshold	V_{TH_EXTVCC}	EXTVCC rising, hysteresis = 110mV		3	3.25	V
THERMAL OVERLOAD						
Thermal Shutdown Temperature		(Note 5)		170		°C
Thermal Shutdown Hysteresis		(Note 5)		20		°C
EN Logic Input						
High Threshold		EN_	1.8			V
Low Threshold		EN_			0.8	V
EN Input Bias Current		EN_ Logic Inputs Only, T_A = +25°C		0.01	1	µA
SPREAD SPECTRUM						
Spread Spectrum		Spread spectrum enabled		f_{OSC} ±6%		

Note 3: Limits are 100% tested at +25°C. Limits over operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at +25°C.

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours

Note 5: Guaranteed by design, not production tested.

Pin Configuration



TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION
1	EN2	High-Voltage Tolerant, Active-High Digital Enable Input for Boost Controller. Drive EN2 high to enable boost controller.
2	PGND	Power Ground
3	EN1	High-Voltage Tolerant, Active High Digital Enable Input for Buck 1. Drive EN1 high to enable Buck 1.
4	OUT1	Output Sense Input for Buck 1. When using the internal preset 5V feedback divider, FB1 is connected to BIAS, and Buck 1 uses OUT1 to sense the output voltage.
5	FB1	Feedback Input for Buck 1. Connect FB1 to BIAS for fixed output or to a resistor divider between OUT1 and AGND to adjust the output voltage between 1V and 14V. FB1 is regulated to 1V (typ) in adjustable version.
6	SUPSW1	Buck 1 Internal High-Side Switch Supply Input and BIAS LDO Input. Bypass SUPSW1 to PGND1 with a 4.7µF ceramic capacitor.
7	BST1	Boost Flying Capacitor Connection for High-Side Gate Voltage of Buck 1. Connect a ceramic capacitor between BST1 and LX1.
8	PGOOD1	Open Drain Power-Good Output for Buck 1. PGOOD1 is low if OUT1 falls below 93.5% (typ) of output regulation voltage. PGOOD1 becomes high impedance when OUT1 rises above 95% (typ) of its regulation voltage. PGOOD1 asserts low during soft-start and in shutdown. To obtain a logic signal, pull up PGOOD1 with an external resistor connected to a positive voltage lower than 5.5V.
9, 10	LX1	Buck 1 Inductor Connection. Connect an inductor from LX1 to the Buck 1 output.

Pin Description (continued)

PIN	NAME	FUNCTION
11	PGND1	Power Ground for Buck 1
12,13, 14	PGND	Power Ground
15	N.C.	Not Connected
16,17,18	PGND	Power Ground
19	CSP	Positive Current-Sense Input for Boost Controller. Connect CSP to the positive terminal of the current sense resistor.
20	PGND2	Power Ground for Boost Controller. All the high current paths for the boost controller terminates to PGND2.
21	DL	Boost Controller N-Channel MOSFET Low Side Gate Driver Output
22	COMP	Boost Error Amplifier Output. Connect COMP with an RC compensation network.
23	FB2	Boost Controller Feedback Input. Connect an external resistive divider from boost output to FB2, and FB2 to AGND to set the output voltage for the boost adjustable output option. Connect FB2 to boost output for the fixed boost output option.
24	SUP	Boost Controller Input Sense
25	AGND	Quiet Analog Ground for the IC
26	BIAS	5V Internal Linear Regulator Output. Bypass BIAS to ground with a low ESR minimum 2.2µF ceramic capacitor. BIAS provides the power to the internal gate drive circuitry.
27	EXTVCC	Switchover Comparator Input. Connect a voltage between 3.25V and 5.5V to EXTVCC to power the IC and bypass the internal bias LDO. Connect EXTVCC to ground if EXTVCC is not used.
28	FSYNC	External Clock Synchronization Input. Synchronization operating frequency ratio is 1.
—	EP	Exposed Pad. Connect EP to ground. Connecting EP to ground does not remove the requirement for proper ground connections to PGND and AGND. EP is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Inductor Selection

Duty cycle and frequency are important to calculate the inductor size, as the inductor current ramps up during the on-time of the switch and ramps down during its off-time. The duty cycle is calculated by the formula:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D}$$

Choose 0.3 as the ratio of the inductor peak-to-peak AC current to DC average current, LIR. The inductor value can be calculated as follows:

$$L\ [\mu H] = \frac{V_{IN} \times D}{f_{SW}\ [MHz] \times 0.3 \times I_{OUT}}$$

With a higher switching frequency, a lower inductance value can be selected to minimize the component size and improve transient response at the expense of reduced efficiency. With a lower switching frequency, a higher inductance value can be selected to reduce the inductor ripple current and achieve better efficiency.

Select the inductor with low DC resistance and with a saturation current rating higher than the boost peak switch current limit.

$$I_{L\_SAT} > I_{L\_MAX} + \frac{\triangle I_{L\_PK}}{2}$$

Input Capacitor

The input current of the boost converter is continuous and its RMS ripple current at the input capacitor is low. Calculate the minimum input capacitor value and the maximum ESR using the following equations:

$$C_{IN} = \frac{\triangle I_L \times D}{4 \times f_{SW} \times \triangle V_Q}$$

$$ESR = \frac{\triangle V_{ESR}}{\triangle I_L}$$

where:

$$\triangle I_L = \frac{(V_{IN} - V_{DS}) \times D}{f_{SW} \times L}$$

and,

V_{DS} = Total voltage drop across the external MOSFET plus the voltage drop across the inductor ESR,

ΔI_L = Peak-to-peak inductor ripple current,

ΔV_Q = Portion of input ripple due to the capacitor discharge,

ΔV_{ESR} = Contribution due to ESR of the capacitor.

Assume the input capacitor ripple contribution due to ESR (ΔV_{ESR}) and capacitor discharge (ΔV_Q) are equal when using a combination of ceramic and aluminium capacitors. During the converter turn-on, a large current is drawn from the input source.

Output Capacitor

In a boost converter, the output capacitor supplies the load current when the main switch is on. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop while supporting the load current. Use the following equations to calculate the output capacitor for a specified output ripple. All ripple values are peak-to-peak:

$$ESR = \frac{\triangle V_{ESR}}{I_{OUT}}$$

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{\triangle V_Q \times f_{SW}}$$

where D_{MAX} is the maximum duty cycle at the minimum input voltage. Use a combination of low-ESR ceramic and high-value, low-cost aluminum capacitors for lower output ripple and noise.

Current Sense Resistor Selection

The current sense resistor R_{CS} connected between CSP and PGND2, sets the boost input current limit. The CSP input has 50mV (typ) voltage trip level. Set the current limit threshold above the peak switch current at the rated output power and minimum input voltage. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{IN(MAX)}}$$

where $I_{IN(MAX)}$ is the peak current that flows through the MOSFET at full load and minimum V_{IN}.

$$I_{IN(MAX)} = \frac{I_{LOAD(MAX)}}{1 - D_{MAX}}$$

When the voltage across the current sense resistor by this current exceeds the current limit comparator threshold, the MOSFET driver (DL) quickly terminates the on-cycle.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses, low EMI, and clean, stable operation. If possible, mount all power components on the top side of the board, and minimize the high frequency current loop as small as possible. Refer to the MAX20458 EV kit for an example layout. Follow these guidelines for good PCB layout.

For buck converter, place the input bypass capacitors as close to SUPSW1 as possible. The buck input capacitors deliver high di/dt current pulses when its high-side MOSFET turns on. Minimize the parasitic inductance in the power input traces to improve efficiency and reliability.

Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal for each buck regulator. This minimizes the area of current loop when the high-side MOSFET is conducting.

Keep buck high-current paths, and power traces wide and short. Minimize the traces from each buck LX node to each inductor and from each inductor to the output capacitors. This minimizes the buck current loop area and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency. Using thick copper PCBs (2 ounces vs. 1 ounce) can improve full load efficiency by 1% or more.

The boost controller loop, including the N-channel MOSFET, diode, and output capacitor has high di/dt current pulses. Keep this loop as small as possible.

The trace from the boost controller gate driver output DL to the gate of the low-side N-channel MOSFET should be wide and short. The gate driver has a high di/dt when switching. Minimized gate driver traces can reduce rising and falling time to further reduce the switching loss.

Connect the ground terminal of the current sense resistor, boost output capacitors, and PGND2 as close as possible.

Connect current sense resistor to CSP by Kelvin sensing connection to minimize current sensing error.

Keep all sensitive analog signals (FB1, FB2, and COMP) away from noisy switching nodes (LX1, BST1, and DL) and high current loops.

Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the device.

Ground is the return path for the full load currents flowing into and out of the MAX20458. It is also the common reference voltage for all the analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage reference and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Connect all the analog ground (AGND) and power grounds (PGND1, and PGND2) together at a single point in a star ground connection. The IC exposed pad can be the point for ground connection.

The exposed pad under the bottom of the package is attached with epoxy to the substrate of the IC, making it an excellent path to remove heat from the IC. Connect the exposed pad to large ground plane areas through external or internal layers. Place multiple small vias under the exposed pad to effectively transfer heat down to the internal ground plane and the back side of the PCB to further improve the thermal resistance from the IC package to the ambient.

Typical Application Circuits

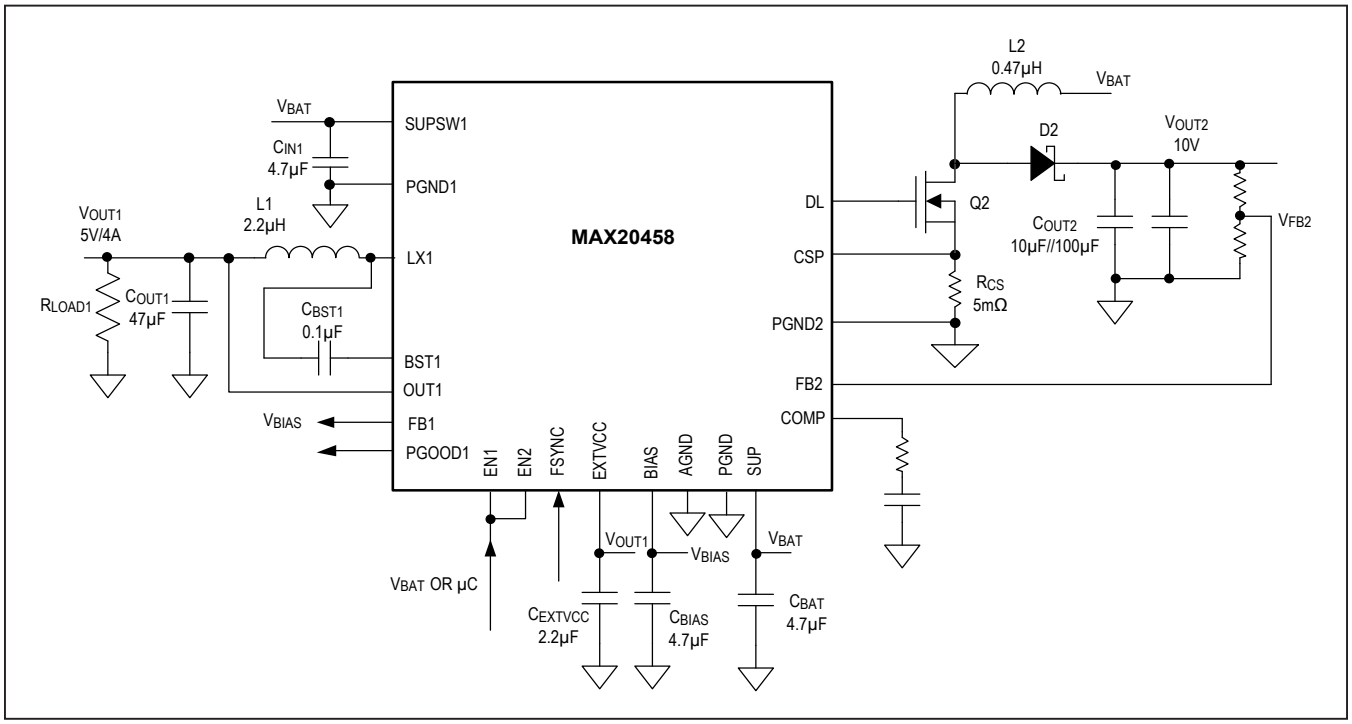


Figure 3. MAX20458ATIE/VY+ Configuration: 2.1MHz, 5V/ADJ Outputs

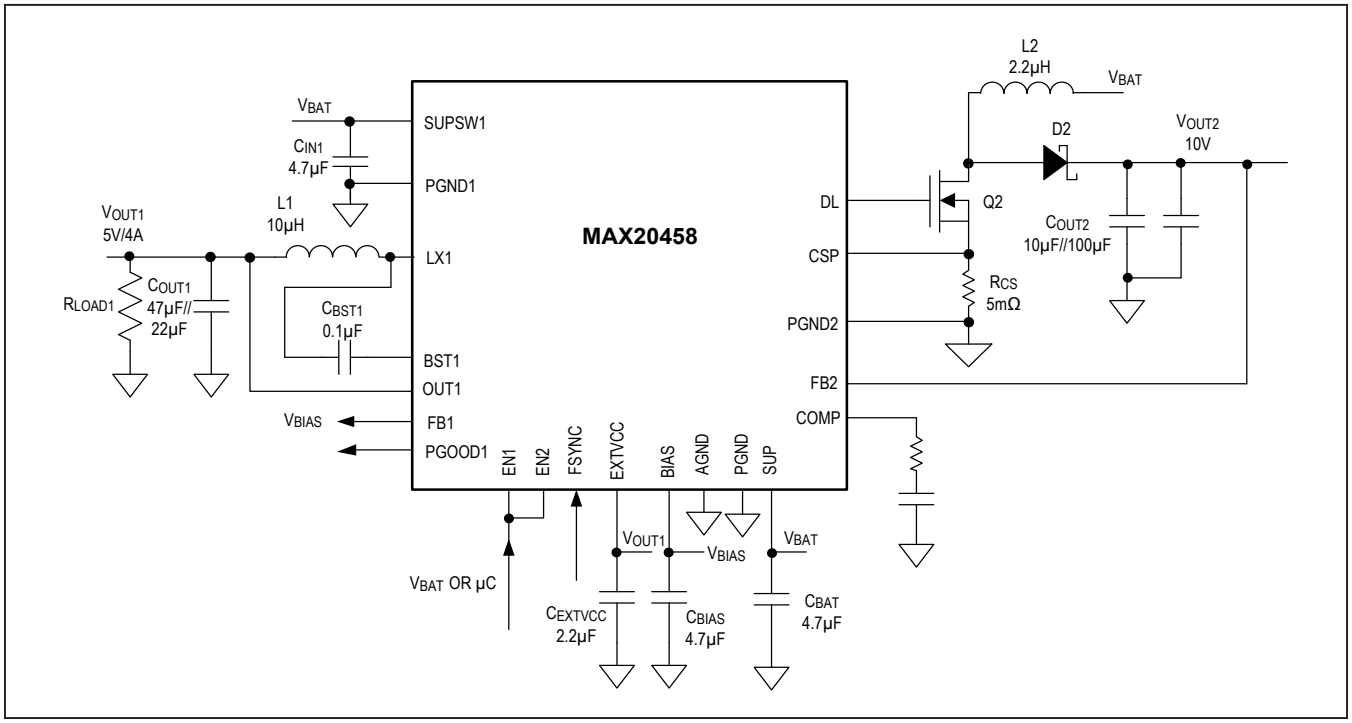


Figure 4. MAX20458ATIE/VY+ Configuration: 2.1MHz, 5V/10V Outputs