**General Description**

The MAX20091 is a 35-channel automotive contact monitor for automotive applications. Ten contact monitor inputs can be used with either ground- or battery-connected switches; the other 25 inputs are for use with ground-connected switches.

The IC operates over a 5.5V to 28V voltage range and withstands voltages up to 42V. It protects low-voltage circuitry from high voltages and reverse-battery conditions. The IC’s low-current operation under all operating conditions makes it suitable for use in electronic control units (ECUs) that are connected directly to the automotive battery. The IC has an adjustable scan mode that reduces the current drawn in key-off while maintaining polling capability.

The IC features an SPI interface to monitor the switch status and set the device configuration. An interrupt output allows the device to wake a local microcontroller when a switch status change is detected. In addition, a switch status change turns on the internal regulator.

The MAX20091 is available in a compact 48-pin TQFN package and operates over the -40°C to +125°C temperature range.

**Applications**

- Automotive Body Computers
- Smart Junction Boxes
- Door Modules

**Benefits and Features**

- Reduces Cost by Eliminating Multiple Microprocessors for Switch-Monitoring Functions
  - Configurable Wetting Current Improves Switch Performance
  - SPI Interface for Control/Readback
  - Built-In Hysteresis and Deglitching
  - Interrupt Output to Processor
- High Channel Count Reduces PCB Area Requirements
- Very Low Operating Current Enables Scanning in Key-Off State with Minimal Current Draw from 12V Battery
  - Ultra-Low 88μA (typ) Operating Current in Polling Mode
- Robust Switch Input Eliminate Need for External Protection Components
  - 5.5V to 28V Operating Voltage Range
  - Switch Inputs Withstand 42V and Reverse Battery
  - IN0-34 ESD Performance to ISO 10605 (In-Circuit): ±10kV Contact

**Ordering Information and Typical Operating Circuit** appears at end of data sheet.
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage Range</td>
<td>VBATT</td>
<td>(Note 3)</td>
<td>7.5</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Battery OVP Threshold</td>
<td>VBATTOV</td>
<td>Polling disabled above VBATT rising</td>
<td>28.4</td>
<td>29.5</td>
<td>30.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VBATT falling</td>
<td>28.1</td>
<td>29</td>
<td>30.4</td>
<td></td>
</tr>
<tr>
<td>VIo Voltage Range</td>
<td>VIo</td>
<td>Rising</td>
<td>4</td>
<td>4.5</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling</td>
<td>3.5</td>
<td>4</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>BATT Undervoltage Lockout</td>
<td>VIUVLO</td>
<td>Continuous mode, IWETT set to 10mA, all switches open, VBAT = 7.5V to 28V</td>
<td>3.3</td>
<td>5.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>IBATT</td>
<td>Continuous mode, IWETT set to 2mA, all switches open, VBAT = 7.5V to 28V</td>
<td>88</td>
<td>110</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Continuous mode, IWETT set to 10mA, all switches open, VBAT = 7.5V to 28V</td>
<td>3.3</td>
<td>5.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>VIo Supply Current</td>
<td>IVIo</td>
<td>Continuous mode, IWETT set to 2mA, all switches open, VBAT = 7.5V to 28V</td>
<td>10</td>
<td>55</td>
<td>200</td>
<td>nA</td>
</tr>
<tr>
<td>PVL Voltage</td>
<td>VPVL</td>
<td>+7.5V ≤ VBATT ≤ +28V</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Thermal Characteristics (Note 1)**

- TQFN (Four-Layer Board)
  - Junction-to-Ambient Thermal Resistance (θJA) | 25°C/W
  - Junction-to-Case Thermal Resistance (θJC) | 1°C/W

- TQFN (Single-Layer Board)
  - Junction-to-Ambient Thermal Resistance (θJA) | 36°C/W
  - Junction-to-Case Thermal Resistance (θJC) | 1°C/W

**Electrical Characteristics**

(VBAT = 14V, VIo = 5V, TA = TJ = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)
### Electrical Characteristics (continued)

(V<sub>BATT</sub> = 14V, V<sub>IO</sub> = 5V, T<sub>A</sub> = T<sub>J</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWITCH INPUTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Threshold</td>
<td>V&lt;sub&gt;THR&lt;/sub&gt;</td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 7.5V to 28V, SPI setting 00</td>
<td>3.7</td>
<td>4.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 7.5V to 28V, SPI setting 01</td>
<td>3.5</td>
<td>3.8</td>
<td>4.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 7.5V to 28V, SPI setting 10</td>
<td>2.75</td>
<td>3</td>
<td>3.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 7.5V to 28V, SPI setting 11</td>
<td>1.8</td>
<td>2</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td>Input Hysteresis</td>
<td>V&lt;sub&gt;HYST&lt;/sub&gt;</td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 7.5V to 28V</td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Wetting Current Accuracy</td>
<td>I&lt;sub&gt;WETT&lt;/sub&gt;</td>
<td>2mA setting, 5.5V &lt; V&lt;sub&gt;BATT&lt;/sub&gt; &lt; 28V</td>
<td>1.7</td>
<td>2</td>
<td>2.3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5mA setting, 5.5V &lt; V&lt;sub&gt;BATT&lt;/sub&gt; &lt; 28V</td>
<td>4.25</td>
<td>5</td>
<td>5.75</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10mA setting, 5.5V &lt; V&lt;sub&gt;BATT&lt;/sub&gt; &lt; 28V</td>
<td>8.5</td>
<td>10</td>
<td>11.5</td>
<td></td>
</tr>
<tr>
<td>IN0–IN34 Input Current</td>
<td>I&lt;sub&gt;IN_&lt;/sub&gt;</td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; = 14V, wetting current set to zero, T&lt;sub&gt;A&lt;/sub&gt; = +25°C</td>
<td>-2</td>
<td>1</td>
<td>+2</td>
<td>µA</td>
</tr>
<tr>
<td>Dropout Voltage with</td>
<td>V&lt;sub&gt;DROPOUT&lt;/sub&gt;</td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; - V&lt;sub&gt;IN_&lt;/sub&gt; , wetting current at 90% of set value (90% of actual value when set to 10mA)</td>
<td>2.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>GND-Connected Switch</td>
<td></td>
<td>V&lt;sub&gt;BATT&lt;/sub&gt; - V&lt;sub&gt;IN_&lt;/sub&gt; , wetting current at 90% of set value (90% of actual value when set to 2mA)</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polling Active Time Accuracy</td>
<td>t&lt;sub&gt;POLLACT&lt;/sub&gt;</td>
<td></td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>%</td>
</tr>
<tr>
<td>Polling Time Accuracy</td>
<td>t&lt;sub&gt;POLL&lt;/sub&gt;</td>
<td></td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>%</td>
</tr>
<tr>
<td><strong>LOGIC LEVELS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT Output Voltage Low</td>
<td>V&lt;sub&gt;OUTL&lt;/sub&gt;</td>
<td>Sinking 2mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SDO Output Voltage Low</td>
<td>V&lt;sub&gt;SDOL&lt;/sub&gt;</td>
<td>Sinking 2mA</td>
<td>0.2</td>
<td>V&lt;sub&gt;IO&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDO Output Voltage High</td>
<td>V&lt;sub&gt;SDOH&lt;/sub&gt;</td>
<td>Sourcing 1mA</td>
<td>0.8</td>
<td>V&lt;sub&gt;IO&lt;/sub&gt;</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SDO Leakage Current in High-impedance Mode</td>
<td>I&lt;sub&gt;LKSDO&lt;/sub&gt;</td>
<td>CS = V&lt;sub&gt;IO&lt;/sub&gt;</td>
<td>-1</td>
<td></td>
<td>+1</td>
<td>µA</td>
</tr>
<tr>
<td>SDI, CLK, CS Input Voltage Low</td>
<td>V&lt;sub&gt;INL&lt;/sub&gt;</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SDI, CLK, CS Input Voltage High</td>
<td>V&lt;sub&gt;INH&lt;/sub&gt;</td>
<td></td>
<td>2.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>INT Output Leakage Current</td>
<td></td>
<td>-5</td>
<td></td>
<td>+5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>SDI Internal Pulldown Resistor</td>
<td>R&lt;sub&gt;SDI&lt;/sub&gt;</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td><strong>THERMAL PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Warming</td>
<td>T&lt;sub&gt;WARN&lt;/sub&gt;</td>
<td>INT asserted low and T bit set in SPI word</td>
<td>145</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>T&lt;sub&gt;SHDN&lt;/sub&gt;</td>
<td></td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal-Shutdown Hysteresis</td>
<td>T&lt;sub&gt;SHDN.HYS&lt;/sub&gt;</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (continued)

\( V_{\text{BATT}} = 14\, \text{V}, V_{\text{IO}} = 5\, \text{V}, T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}, \) unless otherwise noted. Typical values are at \( T_A = +25^\circ \text{C.} \) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIMING</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Frequency Range</td>
<td></td>
<td></td>
<td>0.1</td>
<td></td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>Falling Edge of CS to Rising Edge of SCK Setup Time</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Falling Edge of SCK to Rising Edge of CS Setup Time</td>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum SCK Low After Rising Edge of CS Hold Time</td>
<td>( t_{\text{HS}} )</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Minimum Data Valid to SCK Rising-Edge Setup Time</td>
<td>( t_{\text{DS}} )</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum Data Valid to SCK Rising-Edge Hold Time</td>
<td>( t_{\text{DH}} )</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Minimum SCK High Pulse Width</td>
<td>( t_{\text{CH}} )</td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Minimum SCK Low Pulse Width</td>
<td>( t_{\text{CL}} )</td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Minimum CS High Pulse Width</td>
<td>( t_{\text{CSH}} )</td>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Maximum Transition Time from Falling Edge of CS to Valid SDO</td>
<td>( t_{\text{CSG}} )</td>
<td>( C_L = 10, \text{pF} ) load capacitance from SDO to ground</td>
<td></td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Maximum Transition Time from Falling Edge of SCK to Valid SDO</td>
<td>( t_{\text{CG}} )</td>
<td>( C_L = 10, \text{pF} ) load capacitance from SDO to ground</td>
<td></td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 2:** All devices 100% production tested at \( T_A = +25^\circ \text{C}. \) Limits over temperature are guaranteed by design.

**Note 3:** When BATT is above 28V, the wetting current is disabled to limit power dissipation, and the switch inputs are not monitored. When BATT returns below 28V, there is a 1ms blanking time before the external switches are polled.
Typical Operating Characteristics

\(V_{\text{BATT}} = 14\, \text{V}, \, T_{\text{A}} = +25^\circ\, \text{C}, \) unless otherwise noted.

![SPI Timing Diagram](image)

![Wetting Current vs. Supply Voltage](image)

![Wetting Current vs. Temperature](image)
Typical Operating Characteristics (continued)
($V_{BATT} = 14\,\text{V}, \, T_A = +25^\circ\text{C}$, unless otherwise noted.)
Typical Operating Characteristics (continued)

(V_{BATT} = 14V, T_A = +25°C, unless otherwise noted.)

**QUIESCENT CURRENT IN POLLING MODE**

(PT = 64ms, PAT = 128μs)

**INPUT THRESHOLD vs. TEMPERATURE**

(HIGH-SIDE SWITCH, TH_.1 = TH_.0 = 0)

**INPUT THRESHOLD vs. TEMPERATURE**

(LOW-SIDE SWITCH, TH_.1 = TH_.0 = 0)

**SWITCH THRESHOLD vs. BATT VOLTAGE**

(TH_.1 = TH_.0 = 0)
Pin Configuration

TOP VIEW

MAX20091

TQFN
(7mm x 7mm, 0.5mm PITCH)
## Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>IN8, IN9</td>
<td>Switch Monitor Input Channels 8 and 9. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input.</td>
</tr>
<tr>
<td>3–27</td>
<td>IN10, IN34</td>
<td>Switch Monitor Input Channels 10–34. Connect to a ground-connected switch.</td>
</tr>
<tr>
<td>28</td>
<td>GND</td>
<td>Ground Connection</td>
</tr>
<tr>
<td>29</td>
<td>VIO</td>
<td>Logic Supply for SPI Interface Pins. Connect to a supply between 3V and 5V. Bypass VIO to GND with a 0.1µF capacitor placed as close to VIO as possible.</td>
</tr>
<tr>
<td>30</td>
<td>SDO</td>
<td>SPI Data Output. SDO is high impedance when CS is high.</td>
</tr>
<tr>
<td>31</td>
<td>CS</td>
<td>SPI Active-Low Chip-Select. Drive CS low to enable clocking of data into and out of the IC. SPI data is latched into the device on the rising edge of CS. In polling mode CS must be maintained high to ensure correct operation of the INT output. If needed, the PVL output can be used as the pullup power.</td>
</tr>
<tr>
<td>32</td>
<td>SCK</td>
<td>SPI Clock Input</td>
</tr>
<tr>
<td>33</td>
<td>SDI</td>
<td>SPI Data Input. SPI data is latched into the internal shift register on the rising edges of SCK while CS is held low. SDI has an internal 75kΩ pulldown resistor. Connect SDI to the SDO of a preceding device in a daisy chain or to the microcontroller data output.</td>
</tr>
<tr>
<td>34</td>
<td>INT</td>
<td>Open-Drain Interrupt Output. INT goes low when an input switch change has been detected in scan mode.</td>
</tr>
<tr>
<td>35, 36</td>
<td>PVL</td>
<td>Internal Linear Regulator Output. PVL is the supply for the internal blocks. Bypass PVL with a 2.2µF capacitor to ground.</td>
</tr>
<tr>
<td>37–39</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>40</td>
<td>BATT</td>
<td>Battery Voltage Connection. BATT should be protected from reverse battery using a series diode. Bypass BATT to GND with a 0.1µF ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47µF or greater capacitor.</td>
</tr>
<tr>
<td>41–48</td>
<td>IN0–IN7</td>
<td>Switch Monitor Input Channels 0–7. Connect to a battery-connected or ground-connected switch. When used for a battery-connected switch, add a 100Ω series protection resistor to the input.</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.</td>
</tr>
</tbody>
</table>
Functional Diagram

MAX20091

Bias Circuitry

Oscillator 1MHz

Scan Logic + Control

Temp Sensor

SPI

In0

In9

In10

In34

Batt

IWETH

IWETH

IWETH

10x

25x

REF

MUX

MUX

MUX

+1

+1

1MHz

1MHz

Vio

PVL

SDI

SCK

CS

SDO

Vio

GND

www.maximintegrated.com

Maxim Integrated | 10
Detailed Description
The MAX20091 is a 35-channel automotive contact monitor designed as an interface between mechanical switches and low-voltage microcontrollers or other logic circuits. It features an SPI interface to monitor individual switch inputs and to configure interrupt capability, wetting current, switch configuration (battery-connected or ground-connected), polling time, and polling active time. Any switch status change causes an interrupt signal if the switch is interrupt enabled. The IC has two modes of operation: continuous mode and polling mode.

BATT and V\textsubscript{IO}
V\textsubscript{IO} is the power-supply input for the logic output circuitry. Connect V\textsubscript{IO} to a 3V to 5.5V logic-level supply. Bypass V\textsubscript{IO} to GND with at least a 0.1\textmu F capacitor placed as close as possible to the V\textsubscript{IO} pin.

BATT is the main power-supply input. Bypass BATT to GND with a 0.1\textmu F ceramic capacitor placed as close as possible to the pin. In addition, bypass BATT with a 47\textmu F or greater capacitor. When BATT exceeds 28V (typ) wetting current is disabled, switch scanning is stopped and the OVP bit in SPI register 0x04 is set.

PVL is the output of an internal ultra-low current regulator that is always enabled when BATT is above its undervoltage lockout. Bypass PVL with a 2.2\textmu F capacitor.

Operating Modes
The IC features two modes of operation: continuous mode and polling mode. In continuous mode, the wetting currents (if enabled) are continuously applied to closed switches. In polling mode, the wetting currents are applied to the closed switches for a preset duration to reduce the power consumption.

Continuous Mode Operation (P2:P0 = 0)
In continuous mode, reading of the switch status is initiated by a falling edge on CS. The microcontroller initiates a low pulse on CS to update the IC’s switch status register. If INT remains high, no action needs be taken by the microcontroller. If INT goes low, the microcontroller may perform a read operation to read the updated switch status. On the rising edge of CS, INT is updated. To get correct data, the microcontroller must wait at least 4\textmu s before initiating a switch status read operation.

Polling-Mode Operation
In polling mode, each switch input is sampled for a programmable polling active time set by the PA[2:0] bits between 96\textmu s and 4ms (see Table 5). Sampling is repeated at a period set by the P[3:0] bits (from 8ms to continuous, see Table 4). All switch inputs are sampled simultaneously at the end of the polling active time. Wetting currents (if enabled) are applied to closed switches during the polling active time. Polling mode thus reduces the current consumption from the BATT power supply to a value dependent on the polling time and polling active time chosen.

Mechanical Switch Inputs (IN0–IN34)
IN0–IN34 are the inputs for remote mechanical switches. The switch status is indicated by the SS[34:0] bits in the switch status registers, and each switch input can be programmed to assert an interrupt (INT) by writing to the IE[34:0] bits in registers 0x07 to 0x0B. All switch inputs are interrupt-disabled upon power-up.

The IN10–IN34 inputs are intended for ground-connected switches. The IN0–IN9 inputs can be programmed for either ground-connected switches or battery-connected switches by writing to the LH[9:0] bits in registers 0x05 and 0x06. The default configuration of the IN0–IN9 inputs after power-up is for ground-connected switches. All inputs have an internal glitch filter with a typical filter time of 50\textmu s.

Wetting Current
The IC applies a programmable wetting current to any closed switch to clean switch contacts that are exposed to adverse conditions. The wetting current for each switch can be set to 0mA, 2mA, 5mA, or 10mA by the W_.[1:0] data bits in the wetting current registers by means of SPI. When using wetting current, special care must be taken to avoid exceeding the maximum power dissipation of the IC (see the Applications Information section). Disabling the wetting current or limiting the active-wetting current time reduces power consumption. The default state upon power-up is with wetting current set to 2mA.

Interrupt Output (INT)
INT is an active-low, open-drain output that asserts low when any of the switch inputs change state and is enabled for interrupts, or when the overtemperature warning threshold is exceeded. An external pullup resistor to V\textsubscript{IO} is needed on INT. INT is cleared when CS is driven low for a read/write operation. However, in polling mode, any switch state change or overtemperature change that occurs during an SPI transaction is stored and causes an additional interrupt after the SPI transaction is over and CS goes high. If V\textsubscript{IO} is absent, the INT output is functional provided that it is pulled up to a different supply voltage and that CS is kept high.
Serial Peripheral Interface
The IC is controlled by means of an SPI interface with the local microcontroller. Any number of 8-bit data bursts can be sent within one cycle of CS low to allow for burst-write of all or a subset of the registers. The SPI logic counts the number of bits clocked into the IC and enables data latching only after each 8 bits. The first 8-bit byte is the command byte that is followed by an 8-bit address byte and then by n 8-bit data bytes (write) or n further addresses (read).

SPI Commands
The following four SPI commands are implemented:

**Write:** Within the same CS cycle, a write command is implemented as follows:

SDI: <0x01> <Initial Address> <Data 1> <Data 2> … <Data N>

With this command, Data 1 is written to the address given by <Initial Address>, Data 2 is written to <Initial Address + 1>, and so on.

**Figure 1. Write Sequence**

**Figure 2. Read Sequence**
Table 1. Register Summary

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Switch state register 1</td>
</tr>
<tr>
<td>0x01</td>
<td>Switch state register 2</td>
</tr>
<tr>
<td>0x02</td>
<td>Switch state register 3</td>
</tr>
<tr>
<td>0x03</td>
<td>Switch state register 4</td>
</tr>
<tr>
<td>0x04</td>
<td>Switch state/status register 5</td>
</tr>
<tr>
<td>0x05</td>
<td>Configuration register 1</td>
</tr>
<tr>
<td>0x06</td>
<td>Configuration register 2</td>
</tr>
<tr>
<td>0x07</td>
<td>Interrupt enable register 1</td>
</tr>
<tr>
<td>0x08</td>
<td>Interrupt enable register 2</td>
</tr>
<tr>
<td>0x09</td>
<td>Interrupt enable register 3</td>
</tr>
<tr>
<td>0x0A</td>
<td>Interrupt enable register 4</td>
</tr>
<tr>
<td>0x0B</td>
<td>Interrupt enable register 5</td>
</tr>
<tr>
<td>0x0C</td>
<td>Wetting current register 1</td>
</tr>
<tr>
<td>0x0D</td>
<td>Wetting current register 2</td>
</tr>
<tr>
<td>0x0E</td>
<td>Wetting current register 3</td>
</tr>
<tr>
<td>0x0F</td>
<td>Wetting current register 4</td>
</tr>
<tr>
<td>0x10</td>
<td>Wetting current register 5</td>
</tr>
<tr>
<td>0x11</td>
<td>Wetting current register 6</td>
</tr>
<tr>
<td>0x12</td>
<td>Wetting current register 7</td>
</tr>
<tr>
<td>0x13</td>
<td>Wetting current register 8</td>
</tr>
<tr>
<td>0x14</td>
<td>Wetting current register 9</td>
</tr>
<tr>
<td>0x15</td>
<td>Threshold select register 1</td>
</tr>
<tr>
<td>0x16</td>
<td>Threshold select register 2</td>
</tr>
<tr>
<td>0x17</td>
<td>Threshold select register 3</td>
</tr>
<tr>
<td>0x18</td>
<td>Threshold select register 4</td>
</tr>
<tr>
<td>0x19</td>
<td>Threshold select register 5</td>
</tr>
<tr>
<td>0x1A</td>
<td>Threshold select register 6</td>
</tr>
<tr>
<td>0x1B</td>
<td>Threshold select register 7</td>
</tr>
<tr>
<td>0x1C</td>
<td>Threshold select register 8</td>
</tr>
<tr>
<td>0x1D</td>
<td>Threshold select register 9</td>
</tr>
</tbody>
</table>
**Read**: Within the same CS cycle, a read command is implemented as follows:

SDI: <0x02> <Address 1> <Address 2> <Address 3> ... <Address N> <0x00>
SDO: <0xXX> <0xXX> <Data 1> <Data 2> ... <Data N - 1> <Data N>

With this command, all the registers can be read within the same cycle of CS. The addresses can be given in any order.

**Read All**: Within two CS cycles, the read-all command is implemented as follows:

CS_DEV Cycle 1 CS_DEV Cycle 2
SDI_PWR1: <0x03> <Address N> <0x00> <0x00> <0x00> ... <0x00>
SDO: <Data N><Data N + 1><Data N + 2> ... <Data N + n>

**Reset**: An SPI reset command is implemented as follows:
SDI_PWR1: <0x04>

An internal master reset pulse is generated from the falling edge of the last SCK signal to the falling edge of the following CS signal.

The command bits indicate the registers to be addressed according to Table 2.

**Switch State Bits**
The SS[34:0] bits indicate the state of the switches connected to inputs IN0–IN34, respectively. SS_ is 0 when the switch is open and 1 when the switch is closed.

### Table 2. Register Map

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BIT 7</td>
<td>BIT 6</td>
</tr>
<tr>
<td>0x00</td>
<td>SS34</td>
<td>SS33</td>
</tr>
<tr>
<td>0x01</td>
<td>SS26</td>
<td>SS25</td>
</tr>
<tr>
<td>0x02</td>
<td>SS18</td>
<td>SS17</td>
</tr>
<tr>
<td>0x03</td>
<td>SS10</td>
<td>SS9</td>
</tr>
<tr>
<td>0x04</td>
<td>SS2</td>
<td>SS1</td>
</tr>
<tr>
<td>0x05</td>
<td>P2</td>
<td>P1</td>
</tr>
<tr>
<td>0x06</td>
<td>LH7</td>
<td>LH6</td>
</tr>
<tr>
<td>0x07</td>
<td>IE34</td>
<td>IE33</td>
</tr>
<tr>
<td>0x08</td>
<td>IE26</td>
<td>IE25</td>
</tr>
<tr>
<td>0x09</td>
<td>IE18</td>
<td>IE17</td>
</tr>
<tr>
<td>0x0A</td>
<td>IE10</td>
<td>IE9</td>
</tr>
<tr>
<td>0x0B</td>
<td>IE2</td>
<td>IE1</td>
</tr>
<tr>
<td>0x0C</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0x0D</td>
<td>W31.1</td>
<td>W31.0</td>
</tr>
</tbody>
</table>

**www.maximintegrated.com**
OVP Bit
When 1, the OVP bit indicates that the IC is in overvoltage shutdown due to BATT being over 29.5V (typ).

OTW/OT Bits
The OTW bit indicates an overtemperature warning, while the OT bit indicates overtemperature shutdown when 1.

Interrupt Enable Bits
The IE[34:0] bits program the switch input channel (IN_) to be interrupt-enabled or interrupt-disabled (0 = interrupt disabled, 1 = interrupt enabled). The default value after power-on is 0.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>BIT 7</th>
<th>BIT 6</th>
<th>BIT 5</th>
<th>BIT 4</th>
<th>BIT 3</th>
<th>BIT 2</th>
<th>BIT 1</th>
<th>BIT 0</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0E</td>
<td>W27.1</td>
<td>W27.0</td>
<td>W26.1</td>
<td>W26.0</td>
<td>W25.1</td>
<td>W25.0</td>
<td>W24.1</td>
<td>W24.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x0F</td>
<td>W23.1</td>
<td>W23.0</td>
<td>W22.1</td>
<td>W22.0</td>
<td>W21.1</td>
<td>W21.0</td>
<td>W20.1</td>
<td>W20.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x10</td>
<td>W19.1</td>
<td>W19.0</td>
<td>W18.1</td>
<td>W18.0</td>
<td>W17.1</td>
<td>W17.0</td>
<td>W16.1</td>
<td>W16.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x11</td>
<td>W15.1</td>
<td>W15.0</td>
<td>W14.1</td>
<td>W14.0</td>
<td>W13.1</td>
<td>W13.0</td>
<td>W12.1</td>
<td>W12.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x12</td>
<td>W11.1</td>
<td>W11.0</td>
<td>W10.1</td>
<td>W10.0</td>
<td>W9.1</td>
<td>W9.0</td>
<td>W8.1</td>
<td>W8.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x13</td>
<td>W7.1</td>
<td>W7.0</td>
<td>W6.1</td>
<td>W6.0</td>
<td>W5.1</td>
<td>W5.0</td>
<td>W4.1</td>
<td>W4.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x14</td>
<td>W3.1</td>
<td>W3.0</td>
<td>W2.1</td>
<td>W2.0</td>
<td>W1.1</td>
<td>W1.0</td>
<td>W0.1</td>
<td>W0.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x15</td>
<td>—</td>
<td>—</td>
<td>TH34.1</td>
<td>TH34.0</td>
<td>TH33.1</td>
<td>TH33.0</td>
<td>TH32.1</td>
<td>TH32.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x16</td>
<td>TH31.1</td>
<td>TH31.0</td>
<td>TH30.1</td>
<td>TH30.0</td>
<td>TH29.1</td>
<td>TH29.0</td>
<td>TH28.1</td>
<td>TH28.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x17</td>
<td>TH27.1</td>
<td>TH27.0</td>
<td>TH26.1</td>
<td>TH26.0</td>
<td>TH25.1</td>
<td>TH25.0</td>
<td>TH24.0</td>
<td>TH24.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x18</td>
<td>TH23.1</td>
<td>TH23.0</td>
<td>TH22.1</td>
<td>TH22.0</td>
<td>TH21.1</td>
<td>TH21.0</td>
<td>TH20.1</td>
<td>TH20.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x19</td>
<td>TH19.1</td>
<td>TH19.0</td>
<td>TH18.1</td>
<td>TH18.0</td>
<td>TH17.1</td>
<td>TH17.0</td>
<td>TH16.1</td>
<td>TH16.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x1A</td>
<td>TH15.1</td>
<td>TH15.0</td>
<td>TH14.1</td>
<td>TH14.0</td>
<td>TH13.1</td>
<td>TH13.0</td>
<td>TH12.1</td>
<td>TH12.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x1B</td>
<td>TH11.1</td>
<td>TH11.0</td>
<td>TH10.1</td>
<td>TH10.0</td>
<td>TH9.1</td>
<td>TH9.0</td>
<td>TH8.1</td>
<td>TH8.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x1C</td>
<td>TH7.1</td>
<td>TH7.0</td>
<td>TH6.1</td>
<td>TH6.0</td>
<td>TH5.1</td>
<td>TH5.0</td>
<td>TH4.1</td>
<td>TH4.0</td>
<td>R/W</td>
</tr>
<tr>
<td>0x1D</td>
<td>TH3.1</td>
<td>TH3.0</td>
<td>TH2.1</td>
<td>TH2.0</td>
<td>TH1.1</td>
<td>TH1.0</td>
<td>TH0.1</td>
<td>TH0.0</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Switch Configuration for IN0–IN9
The LH[9:0] bits set the switch configuration for IN0–IN9, respectively. Set LH[9:0] to 0 to configure the input channel for a ground-connected switch. Set LH[9:0] to 1 to configure the input channel to battery connected. The default value after power-on is 0.

Wetting Current-Setting Bits
The W_.[1:0] bits set the corresponding switch channel-wetting current as shown in Table 3.

Table 3. Wetting Current Setting

<table>
<thead>
<tr>
<th>W_.1</th>
<th>W_.0</th>
<th>WETTING CURRENT (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2*</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>10</td>
</tr>
</tbody>
</table>

*Default POR value.
### Table 4. Polling Time Setting

<table>
<thead>
<tr>
<th>P2</th>
<th>P1</th>
<th>P0</th>
<th>POLLING TIME (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Continuous*</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>64</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>128</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>256</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>512</td>
</tr>
</tbody>
</table>

*Default POR value.

### Table 5. Polling Active Time Setting

<table>
<thead>
<tr>
<th>PA2</th>
<th>PA1</th>
<th>PA0</th>
<th>POLLING ACTIVE TIME (Fs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>96</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>128*</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>192</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>256</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>512</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1024</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>2048</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>4096</td>
</tr>
</tbody>
</table>

*Default POR value.

### Table 6. Switch Threshold Setting

<table>
<thead>
<tr>
<th>TH_.1</th>
<th>TH_.0</th>
<th>SWITCH THRESHOLD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>4V*</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>3.8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

*Default POR value.
Applications Information

Power Dissipation

Calculate the total power dissipation of the IC using the following formula:

\[ P = V_{\text{BATT}} \times (I_{\text{BATT}} + I_{\text{WETT}}) \]

where \( I_{\text{WETT}} \) is the total wetting current flowing in all closed switches.

The junction-to-ambient thermal resistance is PCB-dependent and is between 26°C/W (JEDEC multilayer board) and 37°C/W (JEDEC single-layer board) for this package. The junction temperature rise is somewhere between \( P \times 26°C/W \) and \( P \times 37°C/W \). Ensure that the junction temperature does not exceed 150°C during normal operation.

If the IC junction temperature exceeds +165°C, an interrupt signal is generated and the wetting currents are disabled to reduce the on-chip power dissipation. During an overtemperature event, the last switch status is retained in internal memory and the switch status is not updated. The interrupt output is cleared when \( \text{CS} \) goes high, but the overtemperature bit \( T \) in the output word remains for as long as the overtemperature condition persists. When the junction temperature drops by 15°C, the wetting currents are reenabled and there is a 1ms blanking time before the switches can be polled.

Reverse-Battery Tolerance

The IN0–IN23 switch inputs withstand up to -18V DC voltage without damage. A reverse-battery diode is needed to protect BATT, as shown in the Typical Application Circuit.

ISO 7637 Pulse Immunity

The BATT pin and the IN0–IN35 pins are potentially exposed to ISO 7637 pulses. Bypass BATT with a 0.1μF and a 47μF capacitor. The BATT voltage must be limited below 42V during load dump. Bypass IN0–IN35 with at least 0.047μF capacitors at the ECU connector. When IN0–IN9 are used with battery-connected switches, a 100Ω series resistor is needed. These external components allow BATT and IN0–IN35 to withstand ISO 7637 pulses in the application circuit.

Mechanical Switch Characteristics

The IC is designed to operate with switches that have the following characteristics:

1) Minimum resistance value with switch open (due to leakage): 10kΩ.

2) Maximum resistance value with switch closed: 100Ω.

The above resistor value limits vary with the value of wetting current used and the maximum expected ground shift in the system.
Typical Operating Circuit

Chip Information
PROCESS: BICMOS

Package Information
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX20091ATM/V+T</td>
<td>-40°C to +125°C</td>
<td>48 TQFN</td>
</tr>
</tbody>
</table>

/N denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
*EP = Exposed pad.

<table>
<thead>
<tr>
<th>PACKAGE TYPE</th>
<th>PACKAGE CODE</th>
<th>OUTLINE NO.</th>
<th>LAND PATTERN NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>48 TQFN-EP</td>
<td>T4877+6C</td>
<td>21-0144</td>
<td>90-0132</td>
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</table>
### Revision History

<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>6/14</td>
<td>Initial release</td>
<td>—</td>
</tr>
<tr>
<td>1</td>
<td>2/15</td>
<td>Updated the Benefits and Features section</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>11/15</td>
<td>Changed SDI, CLK, CS input voltage low in Electrical Characteristics table from 0.8V to 1V, updated pin 31 in Pin Description table, corrected package code in Package Information table and moved it and Chip Information from page 19 to page 18, removed Selector Guide from Ordering Information header and deleted package code column from the table and page 19 from the data sheet</td>
<td>3, 9, 18</td>
</tr>
<tr>
<td>3</td>
<td>12/15</td>
<td>Added 5mA and 10mA Wetting Current Accuracy specs to the Electrical Characteristics table</td>
<td>3</td>
</tr>
</tbody>
</table>