General Description
The MAX17524 dual-output, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFETs operates over an input-voltage range of 4.5V to 60V. The device can deliver up to 3A on each output and generates output voltages from 0.9V up to 90% of $V_{IN}$. This device features internal compensation. The MAX17524 uses peak current-mode control, and can be operated in pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous-conduction mode (DCM) to enable high efficiency under light-load conditions.

The feedback-voltage regulation accuracy is accurate to within ±1.4% over -40°C to +125°C. The device is available in a 32-pin (5mm x 5mm) Thin QFN (TQFN) package. Simulation models are available.

Applications
- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage Single-Board Systems

Benefits and Features
- Reduces External Components and Total Cost
  - No Schottky - Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable Output Range from 0.9V up to 90% of $V_{IN}$
  - Delivers up to 3A on Each Output Over the Temperature Range
  - 100kHz to 1.1MHz Adjustable Frequency with External Clock Synchronization
  - Available in a 32-Pin, 5mm x 5mm TQFN Package
- Independent Input-Voltage Pins for Each Output
- Reduces Power Dissipation
  - Peak Efficiency of 90.3%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap Supply (EXTVCC) for Improved Efficiency
  - 5.2μA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Independent Adjustable Soft-Start Pin and Programmable EN/UVLO Pin for Each Output
  - Monotonic Startup with Prebiased Output Voltage
  - Built-in Independent Output-Voltage Monitoring with RESET for Each Output
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range / -40°C to +150°C Junction Temperature Range

Ordering Information appears at end of data sheet.
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Stresses</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ to PGND_</td>
<td>-0.3V to +65V</td>
</tr>
<tr>
<td>PGND_ to SGND_</td>
<td>-0.3V to +0.3V</td>
</tr>
<tr>
<td>EXTVCC_ to SGND_</td>
<td>-0.3V to +26V</td>
</tr>
<tr>
<td>EN/UVLO_ to SGND_</td>
<td>-0.3V to +65V</td>
</tr>
<tr>
<td>FB_, $V_{CC}$ to SGND</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>RESET_, SS_, MODE/SYNC_, CF_, RT to SGND</td>
<td>-0.3V to $V_{CC}$+0.3V</td>
</tr>
<tr>
<td>BST_ to PGND_</td>
<td>-0.3V to +70V</td>
</tr>
<tr>
<td>BST_ to LX_</td>
<td>-0.3V to +6V</td>
</tr>
<tr>
<td>BST_ to $V_{CC}$</td>
<td>-0.3V to +65V</td>
</tr>
<tr>
<td>LX_ to PGND_</td>
<td>-0.3V to $V_{IN}$+0.3V</td>
</tr>
<tr>
<td>DL_ to PGND_</td>
<td>-0.3V to $V_{CC}$+0.3V</td>
</tr>
<tr>
<td>LX_ Total RMS Current</td>
<td>4.8A</td>
</tr>
</tbody>
</table>

Continuous Power Dissipation

(Multilayer Board) ($T_A$ = +70°C, derate 34.5mW/°C above +70°C.) 2758.6mW

Output Short-Circuit Duration

Continuous Operating Temperature Range (Note 1) -40°C to 125°C

Junction Temperature +150°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Soldering Temperature (reflow) +260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

- PACKAGE TYPE: 32 TQFN
- Package Code: T3255+4C
- Outline Number: 21-0140
- Land Pattern Number: 90-0012

THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)

- Junction to Ambient ($\theta_{JA}$): 23°C/W
- Junction to Case ($\theta_{JC}$): 1.7°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Note 2: Package thermal resistances were obtained using the MAX17524 Evaluation Kit (EV kit).

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### MAX17524

4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

#### Electrical Characteristics

\( V_{IN} = V_{EN/UVLO} = 24V, R_{RT} = \text{Open} \) (\( f_{SW} = 450 \text{ kHz} \)), \( C_{VCC} = 2.2 \mu F, V_{MODE/SYNC} = V_{SGND} = V_{PGND} = V_{EXTVCC} = 0V, V_{FB} = 1V, \)
\( LX = SS = \text{RESET} = \text{Open}, V_{BST} \) to \( V_{LX} = 5V, T_A = -40^\circ C \) to \( 125^\circ C, \) unless otherwise noted. Typical values are at \( T_A = +25^\circ C. \) All voltages are referenced to \( SGND \) and the data is intended for both the converters, unless otherwise noted. (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT SUPPLY (IN)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input-Voltage Range</td>
<td>( V_{IN} )</td>
<td>( V_{EN/UVLO} = 0V ) (shutdown mode)</td>
<td>4.5</td>
<td>60</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input-Shutdown Current</td>
<td>( I_{IN-SH} )</td>
<td>MODE/SYNC = Open</td>
<td>5.2</td>
<td>9.5</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Input-Quiescent Current</td>
<td>( I_{Q_PFM} )</td>
<td>MODE/SYNC = Open, ( R_{RT} = 22.1k\Omega )</td>
<td>1400</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>( I_{Q_DCM} )</td>
<td>DCM Mode, ( V_{LX} = 0.1V )</td>
<td>1.36</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( I_{Q_PWM} )</td>
<td>( V_{FB} = 0.8V, ) ( \text{EXTVCC} = \text{DL} = \text{Open} )</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ENABLE/UVLO (EN/UVLO)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN/UVLO Threshold</td>
<td>( V_{ENR} )</td>
<td>( V_{EN/UVLO} ) rising</td>
<td>1.19</td>
<td>1.216</td>
<td>1.245</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{ENF} )</td>
<td>( V_{EN/UVLO} ) falling</td>
<td>1.065</td>
<td>1.089</td>
<td>1.116</td>
<td>V</td>
</tr>
<tr>
<td><strong>Vcc (LDO)</strong></td>
<td>( V_{CC} )</td>
<td>1mA ( \leq I_{CC} \leq 20mA )</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Vcc Current Limit</td>
<td>( I_{VCC(MAX)} )</td>
<td>( 6V \leq V_{IN} \leq 60V, I_{CC} = 1mA )</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>mA</td>
</tr>
<tr>
<td>Vcc Dropout</td>
<td>( V_{CC-DO} )</td>
<td>( V_{IN} = 4.5V, I_{VCC} = 25mA )</td>
<td>50</td>
<td>90</td>
<td>140</td>
<td>mA</td>
</tr>
<tr>
<td>Vcc UVLO</td>
<td>( V_{CC_UVR} )</td>
<td>( V_{CC} ) rising</td>
<td>4.09</td>
<td>4.2</td>
<td>4.29</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{CC_UVF} )</td>
<td>( V_{CC} ) falling</td>
<td>3.69</td>
<td>3.8</td>
<td>3.89</td>
<td>V</td>
</tr>
<tr>
<td><strong>EXTVCC</strong></td>
<td>( V_{EXTVCC} )</td>
<td>( V_{EXTVCC} ) rising</td>
<td>4.56</td>
<td>4.7</td>
<td>4.84</td>
<td>V</td>
</tr>
<tr>
<td>EXTVCC Switchover Voltage Hysteresis</td>
<td>( V_{EXTVCC} )</td>
<td>( V_{EXTVCC} ) rising</td>
<td>0.205</td>
<td>0.232</td>
<td>0.26</td>
<td>V</td>
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<tr>
<td><strong>HIGH-SIDE MOSFET AND LOW-SIDE DRIVER</strong></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>High-Side nMOS On-Resistance</td>
<td>( R_{DS-ONH} )</td>
<td>( I_{LX} = 0.3A, ) sourcing</td>
<td>85</td>
<td>180</td>
<td></td>
<td>( \mu \Omega )</td>
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<tr>
<td>LX Leakage Current</td>
<td>( I_{LX_LKG} )</td>
<td>( V_{LX} = (V_{PGND} + 1V) ) to ( (V_{IN} - 1V), T_A = +25^\circ C )</td>
<td>-4</td>
<td>1</td>
<td>+4</td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>SOFT-START (SS)</strong></td>
<td>( I_{SS} )</td>
<td>( V_{SS} = 0.5V )</td>
<td>4.7</td>
<td>5</td>
<td>5.3</td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>FEEDBACK (FB)</strong></td>
<td>( V_{FB-REG} )</td>
<td>MODE/SYNC = SGND or MODE/SYNC = ( V_{CC} )</td>
<td>0.888</td>
<td>0.9</td>
<td>0.912</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MODE/SYNC = Open</td>
<td>0.9</td>
<td>0.915</td>
<td>0.943</td>
<td></td>
</tr>
<tr>
<td>FB Input-Bias Current</td>
<td>( I_{FB} )</td>
<td>( 0 \leq V_{FB} \leq 1V, T_A = 25^\circ C )</td>
<td>-100</td>
<td></td>
<td></td>
<td>( nA )</td>
</tr>
</tbody>
</table>
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Electrical Characteristics (continued)

\( V_{IN} = V_{EN/UVLO} = 24V, R_{RT} = \text{Open (} f_{SW} = 450 \text{ kHz}), C_{VCC} = 2.2\mu F, V_{MODE/SYNC} = V_{SGND}, V_{PGND} = V_{EXTVCC} = 0V, V_{FB} = 1V, L_{X} = SS = \text{RESET} = \text{Open}, V_{BST} = V_{LX} = 5V, T_{A} = -40^{\circ}C \text{ to } 125^{\circ}C, \text{ unless otherwise noted. Typical values are at } T_{A} = +25^{\circ}C. \text{ All voltages are referenced to } SGND \text{ and the data is intended for both the converters, unless otherwise noted.) (Note 3) }

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<tr>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE/SYNC</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>MODE Threshold</td>
<td>VM-DCM</td>
<td>MODE/SYNC = VCC (DCM mode)</td>
<td>VCC - 0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VM-PFM</td>
<td>MODE/SYNC = Open (PFM mode)</td>
<td>VCC/2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VM-PWM</td>
<td>MODE/SYNC = SGND (PWM mode)</td>
<td>0.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SYNC Frequency-Capture Range</td>
<td>fSYNC</td>
<td>fSW set by RRT</td>
<td>1.1 x fSW</td>
<td>1.4 x fSW</td>
<td>1.4 x fSW</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC Pulse Width</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC Threshold</td>
<td>2</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of Pulses Required to Enter into SYNC Mode</td>
<td>8</td>
<td></td>
<td></td>
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<tr>
<td>CURRENT LIMIT</td>
<td>IPEAK-LIMIT</td>
<td>Peak Current-Limit Threshold</td>
<td>4.2</td>
<td>4.6</td>
<td>5.1</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>IRUNAWAY-LIMIT</td>
<td>Runaway Peak Current-Limit Threshold</td>
<td>5.1</td>
<td>5.6</td>
<td>6.3</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>IPFM</td>
<td>PFM Peak Current-Limit Threshold</td>
<td>1.15</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>VNEG-LIM</td>
<td>Negative Current-Limit Threshold</td>
<td>MODE/SYNC = OPEN OR MODE/SYNC = VCC</td>
<td>-8</td>
<td>0</td>
<td>+8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MODE/SYNC = SGND</td>
<td>42</td>
<td>50</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>RT</td>
<td>fSW</td>
<td>Switching Frequency</td>
<td>RRT = 100kΩ</td>
<td>97.5</td>
<td>105</td>
<td>112.5</td>
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<td></td>
<td></td>
<td></td>
<td>RRT = 22.1kΩ</td>
<td>430</td>
<td>454</td>
<td>478</td>
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<td></td>
<td></td>
<td></td>
<td>RRT = 8.25kΩ</td>
<td>950</td>
<td>1100</td>
<td>1250</td>
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<td>RRT = Open</td>
<td>420</td>
<td>450</td>
<td>480</td>
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<tr>
<td></td>
<td>VFB-HICF</td>
<td>VFB Undervoltage Trip Level to Cause Hiccup</td>
<td>0.56</td>
<td>0.58</td>
<td>0.61</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>HICCUP Timeout</td>
<td>(Note 4)</td>
<td>32768</td>
<td></td>
<td></td>
<td>Cycles</td>
</tr>
<tr>
<td></td>
<td>MINIMUM ON-TIME</td>
<td>tON-MIN</td>
<td>90</td>
<td>140</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>MINIMUM OFF-TIME</td>
<td>tOFF-MIN</td>
<td>140</td>
<td>165</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>LX DEAD TIME</td>
<td>LXDT</td>
<td>22</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Electrical Characteristics (continued)

\(V_{\text{IN}} = V_{\text{EN/UVLO}} = 24\text{V}, R_{\text{RT}} = \text{Open (f}_{\text{SW}} = 450\text{ kHz}), C_{\text{VCC}} = 2.2\text{µF}, V_{\text{MODE/SYNC}} = V_{\text{SGND}} = V_{\text{PGND}} = V_{\text{EXTVCC}} = 0\text{V}, V_{\text{FB}} = 1\text{V}, L_X = SS = \text{RESET} = \text{Open, V}_{\text{BST}} \text{ to } V_{\text{LX}} = 5\text{V}, T_A = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \) unless otherwise noted. Typical values are at \(T_A = +25^\circ\text{C}.\) All voltages are referenced to SGND and the data is intended for both the converters, unless otherwise noted. (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET Output-Level Low</td>
<td>(V_{\text{RESETL}})</td>
<td>(I_{\text{RESET}} = 10\text{mA})</td>
<td>110</td>
<td>200</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>RESET Output-Leakage Current</td>
<td>(I_{\text{RESETLKG}})</td>
<td>(T_A = T_J = 25^\circ\text{C}, V_{\text{RESET}} = 5.5\text{V})</td>
<td>-100</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>FB Threshold for RESET Assertion</td>
<td>(V_{\text{FB-OKF}})</td>
<td>(V_{\text{FB}} ) falling</td>
<td>90.4</td>
<td>92.5</td>
<td>94.6</td>
<td>%</td>
</tr>
<tr>
<td>FB Threshold for RESET Deassertion</td>
<td>(V_{\text{FB-OKR}})</td>
<td>(V_{\text{FB}} ) rising</td>
<td>93.4</td>
<td>95.5</td>
<td>97.7</td>
<td>%</td>
</tr>
<tr>
<td>RESET Delay after FB Reaches 95% Regulation</td>
<td>()</td>
<td>()</td>
<td>1024</td>
<td></td>
<td>cycles</td>
<td></td>
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THERMAL SHUTDOWN (TEMP)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal-Shutdown Threshold</td>
<td>Temperature rising</td>
<td>165</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal-Shutdown Hysteresis</td>
<td></td>
<td>10</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 3: Electrical specifications are production tested at \(T_A = +25^\circ\text{C}.\) Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 4: See the Overcurrent Protection (OCP)/Hiccup Mode section for more details.
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

**Typical Operating Characteristics**

\( V_{E N / U V L O 1} = V_{I N 1} = V_{E N / U V L O 2} = V_{I N 2} = 24V, V_{S G N D} = V_{P G N D 1} = V_{P G N D 2} = 0V, C_{V C C 1} = C_{V C C 2} = 2.2\mu F, C_{B S T 1} = C_{B S T 2} = 0.1\mu F, C_{S S 1} = C_{S S 2} = 5600pF, T_A = -40^\circ C \) to \(+125^\circ C\), unless otherwise noted. Typical values are at \( T_A = +25^\circ C\). All voltages are referenced to SGND, unless otherwise noted.)

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Typical Operating Characteristics (continued)

(V\textsubscript{EN/UVLO1} = V\textsubscript{IN1} = V\textsubscript{EN/UVLO2} = V\textsubscript{IN2} = 24V, V\textsubscript{SGND} = V\textsubscript{PGND1} = V\textsubscript{PGND2} = 0V, C\textsubscript{VCC1} = C\textsubscript{VCC2} = 2.2\mu F, C\textsubscript{BST1} = C\textsubscript{BST2} = 0.1\mu F, C\textsubscript{SS1} = C\textsubscript{SS2} = 5600pF, T\textsubscript{A} = -40°C to +125°C, unless otherwise noted. Typical values are at T\textsubscript{A} = +25°C. All voltages are referenced to SGND, unless otherwise noted.)
Typical Operating Characteristics (continued)

(V_{EN/UVLO1} = V_{IN1} = V_{EN/UVLO2} = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2\mu F, C_{BST1} = C_{BST2} = 0.1\mu F, C_{SS1} = C_{SS2} = 5600pF, T_{A} = -40°C to +125°C, unless otherwise noted. Typical values are at T_{A} = +25°C. All voltages are referenced to SGND, unless otherwise noted.)
Typical Operating Characteristics (continued)

\( V_{\text{EN/UVLO1}} = V_{\text{IN1}} = V_{\text{EN/UVLO2}} = V_{\text{IN2}} = 24V, V_{\text{SGND}} = V_{\text{PGND1}} = V_{\text{PGND2}} = 0V, C_{\text{VCC1}} = C_{\text{VCC2}} = 2.2\mu F, C_{\text{BST1}} = C_{\text{BST2}} = 0.1\mu F, C_{\text{SS1}} = C_{\text{SS2}} = 5600\text{pF}, T_A = -40^\circ \text{C} \text{ to } +125^\circ \text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^\circ \text{C. All voltages are referenced to SGND, unless otherwise noted.)}

**MAX17524, 3.3V OUTPUT**

- **LOAD TRANSIENT BETWEEN 1.5A AND 3A**
  \( f_{\text{SW}} = 450\text{kHz}, \text{PWM MODE} \)

- **LOAD TRANSIENT BETWEEN 50mA AND 1.5A**
  \( f_{\text{SW}} = 450\text{kHz}, \text{DCM MODE} \)

- **LOAD TRANSIENT BETWEEN 50mA AND 1.5A**
  \( f_{\text{SW}} = 450\text{kHz}, \text{PFM MODE} \)

**MAX17524, 5V OUTPUT**

- **OVERLOAD PROTECTION**
  \( \text{PWM MODE, } f_{\text{SW}} = 450\text{kHz} \)

- **OVERLOAD PROTECTION**
  \( \text{PWM MODE, } f_{\text{SW}} = 450\text{kHz} \)

- **EXTERNAL CLOCK SYNCHRONIZATION WITH 630kHz**
  \( \text{PWM MODE, 3A LOAD} \)

- **EXTERNAL CLOCK SYNCHRONIZATION WITH 495kHz**
  \( \text{PWM MODE, 3A LOAD} \)
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Typical Operating Characteristics (continued)

(V_{EN/UVLO1} = V_{IN1} = V_{EN/UVLO2} = V_{IN2} = 24V, V_{SGND} = V_{PGND1} = V_{PGND2} = 0V, C_{VCC1} = C_{VCC2} = 2.2μF, C_{BST1} = C_{BST2} = 0.1μF, C_{SS1} = C_{SS2} = 5600pF, T_{A} = -40°C to +125°C, unless otherwise noted. Typical values are at T_{A} = +25°C. All voltages are referenced to SGND, unless otherwise noted.)
PGND1

ename a Power Ground Pin of the Converter. Connect the PGND1 pin externally to the power-ground plane. Connect the SGND and PGND1 pins together at the ground return path of the VCC1 bypass capacitor. Refer to the MAX17524 EV kit data sheet for a layout example.

IN1

Power-Supply Input for Converter. Connect the IN1 pins together. Decouple to PGND1 with a 2.2μF capacitor; place the capacitor close to the IN1 and PGND1 pins. Refer to the MAX17524 EV kit data sheet for a layout example.

VCC1

5V LDO Output for Converter. Bypass VCC1 with a 1μF ceramic capacitance to SGND. LDO does not support the external loading on VCC1.

EN/UVLO1

Enable/Undervoltage Lockout Pin for Converter. Drive EN/UVLO1 high to enable the output of converter. Connect to the center of the resistor-divider between VIN1 and SGND to set the input voltage at which converter turns on. Connect to the VIN1 pins for always-on operation. Pull lower than VENF for disabling the converter.

EXTVCC1

External Power-Supply Input for the Internal LDO of Converter. Applying a voltage between 4.84V and 24V at the EXTVCC1 pin bypasses the internal LDO and improves the overall efficiency. Add a local bypassing cap (0.1μF) on EXTVCC1 pin to SGND and also, add a 4.7Ω resistor from buck converter output node to EXTVCC1 pin to limit VCC1 bypass-cap discharge current during an output short-circuit condition. When EXTVCC1 is not used, connect it to SGND.
### Pin Description (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SS1</td>
<td>Soft-Start Input for Converter 1. Connect a capacitor from SS1 to SGND to set the soft-start time.</td>
</tr>
<tr>
<td>8</td>
<td>CF1</td>
<td>Compensator Output for Converter 1. At switching frequencies, lower than 450kHz, connect a capacitor from CF1 to FB1. Leave CF1 open if the switching frequency is equal to, or more than 450kHz. See the Loop Compensation section for more details.</td>
</tr>
<tr>
<td>9</td>
<td>FB1</td>
<td>Feedback Input for Converter 1. Connect FB1 to the center tap of an external resistor-divider from the output node of converter 1 to SGND to set the output voltage. See the Adjusting Output Voltage section for more details.</td>
</tr>
<tr>
<td>10</td>
<td>RT</td>
<td>Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the switching frequency of both the converters. Leave RT open for the default 450kHz frequency. See the Setting the Switching Frequency (RT) section for more details.</td>
</tr>
<tr>
<td>11</td>
<td>RESET1</td>
<td>Open-Drain RESET1 Output. The RESET1 output is driven low if FB1 drops below 92.5% of its set value. RESET1 goes high 1024 cycles after FB1 rises above 95.5% of its set value.</td>
</tr>
<tr>
<td>12</td>
<td>MODE/SYNC1</td>
<td>Mode Selection and External Clock Synchronization Input for Converter 1. The MODE/SYNC1 Pin configures the converter 1 to operate either in PWM, PFM or DCM modes of operation. Leave MODE/SYNC1 unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC1 to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC1 to VCC1 for DCM operation at light loads. MODE/SYNC1 can also be used to synchronize the converter 1 to an external clock irrespective of the operating condition of converter 2. See the Mode Selection and External Synchronization (MODE/SYNC) section for more details.</td>
</tr>
<tr>
<td>13</td>
<td>SGND</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>14</td>
<td>MODE/SYNC2</td>
<td>Mode Selection and External Clock Synchronization Input for Converter 2. The MODE/SYNC2 Pin configures the converter 2 to operate either in PWM, PFM or DCM modes of operation. Leave MODE/SYNC2 unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC2 to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC2 to VCC2 for DCM operation at light loads. MODE/SYNC2 can also be used to synchronize the converter 2 to an external clock irrespective of the operating condition of converter 1. See the Mode Selection and External Synchronization (MODE/SYNC) section for more details.</td>
</tr>
<tr>
<td>15</td>
<td>RESET2</td>
<td>Open-Drain RESET2 Output. The RESET2 output is driven low if FB2 drops below 92.5% of its set value. RESET2 goes high 1024 cycles after FB2 rises above 95.5% of its set value.</td>
</tr>
<tr>
<td>16</td>
<td>FB2</td>
<td>Feedback Input for Converter 2. Connect FB2 to the center tap of an external resistor-divider from the output node of converter 2 to SGND to set the output voltage. See the Adjusting Output Voltage section for more details.</td>
</tr>
<tr>
<td>17</td>
<td>CF2</td>
<td>Compensator Output for Converter 2. At switching frequencies, lower than 450kHz, connect a capacitor from CF2 to FB2. Leave CF2 open if the switching frequency is equal to, or more than 450kHz. See the Loop Compensation section for more details.</td>
</tr>
<tr>
<td>18</td>
<td>SS2</td>
<td>Soft-Start Input for Converter 2. Connect a capacitor from SS2 to SGND to set the soft-start time.</td>
</tr>
<tr>
<td>19</td>
<td>EXTVCC2</td>
<td>External Power-Supply Input for the Internal LDO of Converter 2. Applying a voltage between 4.84V and 24V at the EXTVCC2 pin bypasses the internal LDO and improves efficiency. Add a local bypassing cap (0.1μF) on EXTVCC2 pin to SGND and also add a 4.7Ω resistor from the buck converter output node to the EXTVCC2 pin to limit VCC2 bypass-cap discharge current during an output short-circuit condition. When EXTVCC2 is not used, connect it to SGND.</td>
</tr>
</tbody>
</table>
## MAX17524 Pin Description (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>EN/UVLO2</td>
<td>Enable/Undervoltage Lockout Pin for Converter 2. Drive EN/UVLO2 high to enable the output of converter 2. Connect to the center of the resistor-divider between V\text{IN2} and SGND to set the input voltage at which converter 2 turns on. Connect to the V\text{IN2} pins for always-on operation. Pull lower than V\text{ENF} for disabling the converter.</td>
</tr>
<tr>
<td>21</td>
<td>V\text{CC2}</td>
<td>5V LDO Output for Converter 2. Bypass V\text{CC2} with a 1μF ceramic capacitance to SGND. LDO does not support the external loading on V\text{CC2}.</td>
</tr>
<tr>
<td>22, 23</td>
<td>IN2</td>
<td>Power-Supply Input for Converter 2. 4.5V to 60V Input-Supply Range. Connect the IN2 pins together. Decouple to PGND2 with a 2.2μF capacitor; place the capacitor close to the IN2 and PGND2 pins. Refer to the MAX17524 EV kit data sheet for a layout example.</td>
</tr>
<tr>
<td>24</td>
<td>PGND2</td>
<td>Power Ground Pin of the Converter 2. Connect the PGND2 pin externally to the power-ground plane. Connect the SGND and PGND2 pins together at the ground return path of the V\text{CC2} bypass capacitor. Refer to the MAX17524 EV kit data sheet for a layout example.</td>
</tr>
<tr>
<td>25</td>
<td>DL2</td>
<td>Low-Side Gate Driver Output for Converter 2. Use DL2 pin to drive the gate of the low-side external nMOSFET.</td>
</tr>
<tr>
<td>26, 27</td>
<td>LX2</td>
<td>Switching Node of Converter 2. Connect LX2 pins to the switching side of the inductor.</td>
</tr>
<tr>
<td>28</td>
<td>BST2</td>
<td>Boost Flying Capacitor of Converter 2. Connect a 0.1μF ceramic capacitor between BST2 and LX2.</td>
</tr>
<tr>
<td>29</td>
<td>BST1</td>
<td>Boost Flying Capacitor of Converter 1. Connect a 0.1μF ceramic capacitor between BST1 and LX1.</td>
</tr>
<tr>
<td>30, 31</td>
<td>LX1</td>
<td>Switching Node of Converter 1. Connect LX1 pins to the switching side of the inductor.</td>
</tr>
<tr>
<td>32</td>
<td>DL1</td>
<td>Low-Side Gate Driver Output for Converter 1. Use DL1 pin to drive the gate of the low-side external nMOSFET.</td>
</tr>
<tr>
<td>–</td>
<td>EP</td>
<td>Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large SGND plane with several thermal vias for best thermal performance. Refer to the MAX17524 EV kit data sheet for an example of the correct method for EP connection and thermal vias.</td>
</tr>
</tbody>
</table>
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Functional Diagram

MAX17524

- LDO SELECT
- INLDO
- ENOK1
- ENOK2
- FB1
- FB2
- PWM/PFM/DCM HICCUP LOGIC
- ERROR AMPLIFIER LOOP COMPENSATION
- CURRENT SENSE
- SLOPE COMPENSATION
- HICCUP1
- HICCUP2
- RESET LOGIC
- BST1
- IN1
- BST2
- IN2
- VCC1
- VCC2
- VX1
- VX2
- SGND1
- SGND2
- ENUVLO1
- ENUVLO2
- CF1
- CF2
- SS1
- SS2
- MODE SELECTION LOGIC
- OSCILLATOR
- RT
- DL1
- DL2
- PGND1
- PGND2
- MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

www.maximintegrated.com
Detailed Description

The MAX17524 dual-output, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFETs operates over an input-voltage range of 4.5V to 60V. Output voltages from 0.9 up to 90% of VOUT can be generated, and 3A load on each output can be delivered by the device. Each converter features internal compensation. The feedback-voltage regulation accuracy is accurate to within ±1.4% over −40°C to +125°C.

The MAX17524 features a peak-current-mode control architecture. Internal transconductance error amplifiers produce integrated-error voltages at two internal nodes, which set the duty cycle using PWM comparators, high-side current-sense amplifiers, and slope-compensation generators. At each rising edge of the clock, the high-side MOSFETs turn on and remain on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFETs’ on-time, the inductor currents ramp up. During the second half of the switching cycle, high-side MOSFETs turn off and the low-side MOSFETs turn on. The inductors release the stored energy as their currents ramp down and provide current to the outputs.

The MAX17524 features a RT pin to program the switching frequency and two MODE/SYNC pins to program the mode of operation and to synchronize to an external clock. The device also features independent adjustable-input undervoltage lockout, adjustable soft-start, open-drain RESET, and auxiliary bootstrap LDO for improved efficiency.

Mode Selection and External Synchronization (MODE/SYNC)

The MAX17524 features two independent mode selection pins for the two converters. The logic state of the MODE/SYNC pin is latched when VCC and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the state of the MODE/SYNC pin is open at power-up, the converter operates in PFM mode at light loads. If the voltage at the MODE/SYNC pin is lower than VM-PWM at power-up, the converter operates in constant-frequency PWM mode at all loads. If the voltage at the MODE/SYNC pin is higher than VM-DCM at power-up, the converter operates in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

The internal clocks of the MAX17524 can be synchronized to external clock signals on the MODE/SYNC pins. The external synchronization clock frequency must be between 1.1 × fSW and 1.4 × fSW, where fSW is the switching frequency programmed by the resistor connected at the RT pin. The external clock signals on the MODE/SYNC pins can have different frequency, but with 1.1 × fSW and 1.4 × fSW. When an external clock is applied to MODE/SYNC pins, the internal oscillator frequency changes to external clock frequency (from the original frequency based on the RT setting) after detecting 8 external clock edges. When the external clock is applied on-fly then the converter operates in PWM mode during synchronization operation irrespective of the initial mode. After the exit from external synchronization, the converter enters into its original mode, which was set before synchronization. Only if the initial mode is PFM, after the exit from external synchronization, the part enters into DCM mode initially and after 32 internal clock cycles, the part enters PFM mode. MODE/SYNC pin of one converter can be synchronized to the external clock irrespective of the MODE/SYNC condition of the other converter. The minimum external clock pulse-width high should be greater than 50ns. See the MODE/SYNC section in the Electrical Characteristics table for details.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of Ip_{PFM} (1.15A (typ)) every clock cycle until the output rises to 103.5% of the set nominal output voltage. Once the output reaches 103.5% of the set nominal output voltage, both the high-side and low-side FETs are turned off and the converter enters hibernate operation until the load discharges the output to 101% of the set nominal output voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the set nominal output voltage, the converters come out of hibernate operation, turn on all internal blocks, and again commence the process of delivering pulses of energy to the output until it reaches 103.5% of the set nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.
DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, not by skipping pulses, but by disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The output-voltage ripple in DCM mode is comparable to PWM mode and relatively lower compared to PFM mode.

Linear Regulator (VCC and EXTVCC)

The MAX17524 has two internal LDO (Low-dropout) regulators for each converter that power VCC. One LDO is powered from VIN and the other LDO is powered from EXTVCC. Only one of the two LDOs is in operation at a time depending on the voltage levels present at the EXTVCC pin. When VCC is above its UVLO and if EXTVCC is greater than 4.7V (typ), internal VCC is powered by EXTVCC and LDO from VIN is disabled. If EXTVCC is less than 4.7V, VCC is powered up from VIN. Powering VCC from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 24V.

Typical VCC output voltage is 5V. Bypass VCC to SGND with a 2.2μF low-ESR ceramic capacitor. VCC powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor. Both LDOs can source up to 90mA (typ). The MAX17524 employs an undervoltage-lockout circuit that forces both the converters off when VCC falls below VCC_UVF. The buck converter can be immediately re-enabled when VCC > VCC_UVR. The 400mV UVLO hysteresis prevents chattering on power-up and power-down.

Add a local bypassing cap of 0.1μF on the EXTVCC pin to SGND. Also, add a 4.7Ω resistor from buck converter output node to the EXTVCC pin to limit VCC bypass cap discharge current and to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit condition. In applications where the buck-converter output is connected to the EXTVCC pin, if the output is shorted to ground, then the transfer from EXTVCC to internal LDO happens seamlessly without any impact to the normal functionality. Connect EXTVCC pin to SGND when the pin is not being used.

Table 1. Switching Frequency vs. RT Resistor

<table>
<thead>
<tr>
<th>SWITCHING FREQUENCY (kHz)</th>
<th>RT RESISTOR (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>105</td>
</tr>
<tr>
<td>200</td>
<td>51.1</td>
</tr>
<tr>
<td>450</td>
<td>Open or 22.1</td>
</tr>
<tr>
<td>1100</td>
<td>8.25</td>
</tr>
</tbody>
</table>
Overcurrent Protection (OCP)/Hiccup Mode
MAX17524 has a robust overcurrent-protection (OCP) scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of IPKLM (4.6A (typ)). A runaway peak current limit on the high-side switch current at IRUNAWAY-LIMIT (5.6A (typ)) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, feedback voltage drops to VFB-HICF any time after soft-start is complete and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload conditions, if feedback voltage does not exceed VFB-HICF, the device continues to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

Thermal-Shutdown Protection
The MAX17524 features independent thermal-shutdown protection for both the converters to limit the junction temperature. When the junction temperature of the converter exceeds +165ºC, an on-chip thermal sensor shuts down the converter, allowing the converter to cool. The thermal sensor turns the converter on again after the junction temperature cools by 10ºC. Soft-start gets deasserted during thermal shutdown and it initiates the startup operation when the converter recovers from thermal shutdown. Carefully evaluate the total power dissipation (see the Power Dissipation section) to avoid unwanted triggering of the thermal shutdown during normal operation.

Applications Information
Input-Capacitor Selection
The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit’s switching. The input capacitor RMS current requirement (IRMS) is defined by the following equation:

\[ I_{\text{RMS}} = \frac{I_{\text{OUT(MAX)}} \times \sqrt{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}} \]

where, \(I_{\text{OUT(MAX)}}\) is the maximum load current, \(I_{\text{RMS}}\) has a maximum value when the input voltage equals twice the output voltage \(V_{\text{IN}} = 2 \times V_{\text{OUT}}\), so

\[ I_{\text{RMS(MAX)}} = \frac{I_{\text{OUT(MAX)}}}{2}. \]

Choose an input capacitor that exhibits less than +10ºC temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

\[ C_{\text{IN}} = \frac{I_{\text{OUT(MAX)}} \times D \times (1 - D)}{\eta \times f_{\text{SW}} \times \Delta V_{\text{IN}}} \]

where:
- \(D = V_{\text{OUT}}/V_{\text{IN}}\) is the duty ratio of the converter
- \(f_{\text{SW}}\) = Switching frequency
- \(\Delta V_{\text{IN}}\) = Allowable input-voltage ripple
- \(\eta\) = Efficiency
In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

**Low-Side MOSFET Selection**

The MAX17524 requires an external nMOSFET for each converter to operate and the low-side gate drive output DL pin drives the nMOSFET. The key selection parameters to select the nMOSFET include:

- Maximum Drain-Source Voltage (V_{DS-MAX})
- Miller Plateau Voltage during all operating conditions < 3.5V
- Low Drain-Source On-State Resistance (R_{DS(ON)})
- Total Gate Charge (Q_g)
- Output Capacitance (C_{oss})
- Power-Dissipation Rating and Package Thermal Resistance

The nMOSFET must be of logic-level type with guaranteed on-state resistance specification at V_{GS} ≈ 4.5V. It is also important that the chosen nMOSFET has suitable dynamic parameters so that the MAX17524 is able to turn it on and off within the specified dead time (L_{DT}). Ensure that the losses in the selected MOSFET do not exceed its power rating. Using a low body diode reverse recovery charge (Q_{rr}) MOSFET reduces the converter loss.

The negative current capability of the low-side MOSFET is limited by V_{NEG-LIM}. V_{NEG-LIM} translates to negative current limit (I_{NEG-LIM}) by the following relation:

\[ V_{NEG-LIM} = I_{NEG-LIM} \times R_{DS(ON)LS} \]

where R_{DS(ON)LS} is the on-state resistance of the low-side MOSFET.

**Inductor Selection**

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value (L) in Henry as follows:

\[ L = \frac{0.9 \times V_{OUT}}{f_{SW}} \]

where V_{OUT} is the output voltage in V and f_{SW} is the switching frequency in Hz.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit (I_{PEAK-LIMIT}).

**Output-Capacitor Selection**

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows:

\[ C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}} \]

\[ t_{RESPONSE} = \frac{0.33}{f_C} \]

where:

- I_{STEP} = Load current step
- t_{RESPONSE} = Response time of the controller
- \Delta V_{OUT} = Allowable output-voltage deviation
- f_C = Target closed-loop crossover frequency

Select f_C to be 1/10th of f_{SW} if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 50kHz. Actual derating of ceramic capacitors with DC bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

**Adjusting Output Voltage**

Set the output voltage of each converter with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see Figure 1). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{TOP} from the output to the FB pin as follows:

\[ R_{TOP} = \frac{301 \times 10^3}{(f_C \times C_{OUT\_SEL})} \]

where:

- R_{TOP} is in kΩ
- f_C = Crossover frequency is in kHz
$C_{\text{OUT\_SEL}} = \text{Actual capacitance of the selected output capacitor at DC-bias voltage in } \mu\text{F.}$

Calculate resistor $R_{\text{BOT}}$ from the FB pin to SGND as follows:

$$R_{\text{BOT}} = \frac{R_{\text{TOP}} \times 0.9}{(V_{\text{OUT}} - 0.9)}$$

$R_{\text{BOT}}$ is in kΩ.

**Loop Compensation**

The MAX17524 is internally loop compensated. However, if the switching frequency is less than 450kHz, connect a 0402 capacitor ($C_F$) between the CF pin and the FB pin. Use Table 2 to select the value of $C_F$.

**Soft-Start Capacitor Selection**

The MAX17524 implements independent adjustable soft-start operation to reduce inrush currents for both the converters. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance ($C_{\text{OUT\_SEL}}$) and the output voltage ($V_{\text{OUT}}$) determine the minimum required soft-start capacitor as follows:

$$C_{\text{SS}} \geq 28 \times 10^{-6} \times C_{\text{OUT\_SEL}} \times V_{\text{OUT}}$$

**Table 2. Selection of Capacitor $C_F$**

<table>
<thead>
<tr>
<th>SWITCHING FREQUENCY RANGE (kHz)</th>
<th>$C_F$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 to 300</td>
<td>2.2</td>
</tr>
<tr>
<td>300 to 450</td>
<td>1.2</td>
</tr>
</tbody>
</table>

The soft-start time ($t_{SS}$) is related to the capacitor connected at SS ($C_{SS}$) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to SGND. Note that during start-up, the device operates at half the programmed switching frequency until the output voltage reaches 67% of set output nominal voltage.

**Setting the Input Undervoltage-Lockout Level**

The MAX17524 features two independent EN/UVLO pins for the two converters. Each EN/UVLO pin has an adjustable input undervoltage-lockout level. Set the voltage at which the converter turns on with a resistive voltage-divider connected from $V_{IN}$ to SGND as shown in Figure 2. Connect the center node of the divider to EN/UVLO. Choose $R_1$ to be 3.3MΩ and then calculate $R_2$ as follows:

$$R_2 = \frac{R_1 \times 1.216}{(V_{INU} - 1.216)}$$

where $V_{INU}$ is the input-voltage level at which the converter is required to turn on. Ensure that $V_{INU}$ is higher than 0.8 $\times$ $V_{OUT}$ to avoid hiccup during slow power up (slower than soft-start)/power down. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin, to reduce voltage ringing on the line.
Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

\[ P_{IC\_LOSS} = P_{IC\_LOSS1} + P_{IC\_LOSS2} \]

\[ P_{IC\_LOSS1} = \left( P_{OUT1} \times \left( \frac{1}{\zeta_1} - 1 \right) \right) - \left( I_{OUT1}^2 \times R_{DCR1} \right) - P_{ACLOSS\_L1} \]

\[ = \left( I_{OUT1}^2 \times R_{DS\_ON1(LS)} \times (1 - D_1) \right) - \left( V_{IN1} \times \left( \frac{1}{2} Q_{oss1} + Q_{rr1} \right) \times f_{SW} \right) \]

\[ P_{OUT1} = V_{OUT1} \times I_{OUT1} \]

The expressions for \( P_{IC\_LOSS2} \) and \( P_{OUT2} \) are same as of \( P_{IC\_LOSS1} \) and \( P_{OUT1} \), where:

- \( P_{OUT} \) = Output power of the converter.
- \( \eta_\_ = \) Efficiency of the converter.
- \( R_{DCR} = \) DC resistance of the inductor (see the Typical Operating Characteristics for more information on efficiency at typical operating conditions).
- \( P_{ACLOSS\_L} = \) AC loss of the inductor.
- \( R_{DS\_ON(LS)} = \) On-state resistance of the low side MOSFET.
- \( Q_{rr} = \) Body-diode reverse-recovery charge of the low-side MOSFET.
- \( D = \) Duty cycle of the converter.
- \( Q_{oss} = \) Output charge of the low side MOSFET.

For a typical multi-layer board, the thermal performance metrics for the package are given below:

\[ \theta_{JA} = 23^\circ C/W \]

\[ \theta_{JC} = 1.7^\circ C/W \]

The junction temperature of the device can be estimated at any given maximum ambient temperature \( (T_{A(MAX)}) \) from the following equation:

\[ T_{J(MAX)} = T_{A(MAX)} + \left( \theta_{JA} \times P_{IC\_LOSS} \right) \]

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature \( (T_{EP(MAX)}) \) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

\[ T_{J(MAX)} = T_{EP(MAX)} + \left( \theta_{JC} \times P_{IC\_LOSS} \right) \]

Note: Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor at the V\text{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous (unbroken) as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17524 EV kit layout available at www.maximintegrated.com.
Coincident/ Ratiometric Tracking and Output Voltage Sequencing

The soft-start pins (SS1 and SS2) can be used to track the output voltages to that of another power supply at startup. Figure 3 shows the independent soft-start of each converter output. Figure 4 shows the coincident tracking of the converter outputs. Figure 5 shows the ratiometric tracking of the converter outputs. Figure 6 shows the output voltage sequencing where converter 1 is the master.
MAX17524 4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

Figure 5. Ratiometric Tracking of the Converter Outputs

Figure 6. Output-Voltage Sequencing
**MAX17524**

4.5V to 60V, 3A, Dual-Output, High-Efficiency, Synchronous Step-Down DC-DC Converter

**Typical Application Circuit**

![Typical Application Circuit Diagram](image)

**Ordering Information**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
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<td>MAX17524ATJ+</td>
<td>-40°C to +125°C</td>
<td>32 TQFN (5mm x 5mm)</td>
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*Denotes a lead(Pb)-free/RoHS compliant package.*
Revision History

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<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
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<td>12/17</td>
<td>Initial release</td>
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<tr>
<td>0.5</td>
<td></td>
<td>Corrected Document Control Identification number</td>
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</tr>
</tbody>
</table>

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