General Description
The MAX16997/MAX16998 are microprocessor (μP) supervisory circuits for high-input-voltage and low-quiescent-current applications. These devices detect downstream circuit failures and provide switchover to redundant circuitry. See the Selector Guide for the different versions of this product family.

The MAX16997/MAX16998 family has four independent inputs for reset and watchdog functions. SWT and SRT inputs independently set the timeout periods of watchdog and reset timers through external capacitors. RESETIN/EN monitor voltages at respective inputs. A resistive voltage-divider sets the reset threshold.

The MAX16998A/B/D generate two output signals, RESET and ENABLE. RESET asserts whenever RESETIN drops below its threshold voltage or when the watchdog timer detects a timing fault at WDI. Once asserted, and after all reset conditions are removed, RESET remains low for the reset timeout period, \( t_{\text{reset}} \), and then goes high. The MAX16997A generates one output signal (ENABLE) based on the voltage level at EN and the signal at WDI.

The MAX16997A does not have a RESET output. The watchdog is disabled if the voltage at EN is below its threshold. The MAX16997A watchdog timer starts timing when the voltage at EN becomes higher than the preset threshold voltage level. Each time EN rises above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period (\( t_{\text{wp}} \)).

The MAX16997/MAX16998 are available in 8-pin lead(Pb)-free μMAX® packages and are fully specified over the -40°C to +125°C automotive temperature range.

Applications
- Automotive
- Industrial

Selector Guide

<table>
<thead>
<tr>
<th>PART</th>
<th>WINDOW SIZE (%)</th>
<th>ENABLE</th>
<th>RESET</th>
<th>EN</th>
<th>RESETIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX16997A</td>
<td>100</td>
<td>✓</td>
<td></td>
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<tr>
<td>MAX16998A</td>
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<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
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<tr>
<td>MAX16998B</td>
<td>50</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>MAX16998D</td>
<td>75</td>
<td>✓</td>
<td>✓</td>
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<td>✓</td>
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</table>

Features
- Wide 5V to 40V Input Voltage Range
- 18μA Quiescent Current (Typical at +125°C)
- Capacitor-Adjustable Timeout Period for Watchdog and Reset
- Windowed Watchdog Timer Options (MAX16998B/D)
- External Voltage Monitoring (RESETIN for the MAX16998A/B/D and EN for the MAX16997A)
- Car Battery-Compatible EN Input
- TTL- and CMOS-Compatible Open-Drain Outputs
- 18V Maximum Open-Drain Reset Output Voltage
- 28V Maximum Open-Drain Enable Output Voltage
- Power-On/Power-Off Reset Functionality (MAX16998A/B/D Only)
- AEC-Q100 Qualified
- -40°C to +125°C Operating Temperature Range
- Small (3mm x 3mm) μMAX Package
- WDI Narrow Pulse Immunity

Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX16997AAUA+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998AAUA+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998AAUA/V+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998BAUA+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998BAUA/V+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998DAUA+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
<tr>
<td>MAX16998DAUA/V+</td>
<td>-40°C to +125°C</td>
<td>8 μMAX</td>
</tr>
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</table>

Denotes a lead(Pb)-free/RoHS-compliant package.
N denotes an automotive qualified part.

Pin Configurations appear at end of data sheet.

μMAX is a registered trademark of Maxim Integrated Products, Inc.
MAX16997/MAX16998 High-Voltage Watchdog Timers with Adjustable Timeout Delay

Absolute Maximum Ratings

(All pins referenced to GND, unless otherwise noted.)

- Continuous Power Dissipation (T_A = +70°C)
- 8-Pin μMAX (derate 4.8mW/°C above +70°C)...........387.8mW
- Operating Temperature Range (T_A)..............-40°C to +125°C
- Junction Temperature (T_J)..........................+150°C
- Storage Temperature Range....................-65°C to +150°C
- Lead Temperature (soldering, 10s)............+300°C

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

- Junction-to-Case Thermal Resistance (θ_JC).............42°C/W
- Junction-to-Ambient Thermal Resistance (θ_JA)........206.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_IN = 14V, T_A = TJ = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Operating Voltage Range</td>
<td>V_IN</td>
<td></td>
<td>5.0</td>
<td>40.0</td>
<td>V</td>
<td></td>
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<tr>
<td>Supply Current</td>
<td>I_IN</td>
<td></td>
<td>18</td>
<td>30</td>
<td>µA</td>
<td></td>
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<tr>
<td>SWT Ramp Current</td>
<td>I_RAMP_SWT</td>
<td>V_SWT = 1.0V</td>
<td>450</td>
<td>500</td>
<td>550</td>
<td>nA</td>
</tr>
<tr>
<td>SRT Ramp Current</td>
<td>I_RAMP_SRT</td>
<td>V_SR_T = 1.0V</td>
<td>410</td>
<td>500</td>
<td>600</td>
<td>nA</td>
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<tr>
<td>SWT/SRT Ramp Threshold Voltage</td>
<td>V_RAMP</td>
<td></td>
<td>1.115</td>
<td>1.235</td>
<td>1.363</td>
<td>V</td>
</tr>
<tr>
<td>Power-On Reset Input Threshold Voltage</td>
<td>V_PON</td>
<td></td>
<td>1.135</td>
<td>1.255</td>
<td>1.383</td>
<td>V</td>
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<tr>
<td>RESETIN Reset Input Threshold Voltage</td>
<td>V_RESETIN</td>
<td></td>
<td>1.115</td>
<td>1.235</td>
<td>1.363</td>
<td>V</td>
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<tr>
<td>RESET Input Leakage Current</td>
<td>I_LPON</td>
<td></td>
<td>0.1</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>RESET Output Low Voltage</td>
<td>V_OLRST</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>RESET Leakage Current</td>
<td>I_LKGR</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>ENABLE Output Low Voltage</td>
<td>V_OLEN</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td>ENABLE Leakage Current</td>
<td>I_LKGE</td>
<td>V_ENABLE = 14V, ENABLE not asserted</td>
<td></td>
<td></td>
<td>µA</td>
<td></td>
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<tr>
<td>Minimum Reset Timeout Period</td>
<td>t_RESETmin</td>
<td></td>
<td>1</td>
<td></td>
<td>ms</td>
<td></td>
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<tr>
<td>Reset Timeout Period</td>
<td>t_RESET</td>
<td></td>
<td>5</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Maximum Reset Time Period</td>
<td>t_RESETmax</td>
<td></td>
<td>116.09</td>
<td></td>
<td>ms</td>
<td></td>
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<tr>
<td>RESET to ENABLE Delay</td>
<td>t_REDL</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>RESETIN to RESET Delay</td>
<td>t_RRD</td>
<td></td>
<td>1</td>
<td></td>
<td>µs</td>
<td></td>
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</table>
### Electrical Characteristics (continued)

\( V_{IN} = 14V, \ T_A = T_J = -40^\circ C \) to +125°C, unless otherwise noted. Typical values are at \( T_A = +25^\circ C. \) (Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>WATCHDOG TIMER</td>
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<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>WDI Input Threshold</td>
<td>( V_{IH} )</td>
<td></td>
<td>2.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{IL} )</td>
<td></td>
<td>0.9</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>WDI Input Hysteresis</td>
<td>( WDHYST )</td>
<td></td>
<td>200</td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>WDI Minimum Pulse Width</td>
<td>( t_{WDimin} )</td>
<td>(Note 4)</td>
<td>6.5</td>
<td></td>
<td></td>
<td>( \mu )s</td>
</tr>
<tr>
<td>WDI Input Current</td>
<td>( I_{WDI} )</td>
<td>( WDI = 0 ) or 14V</td>
<td>0.1</td>
<td></td>
<td></td>
<td>( \mu )A</td>
</tr>
<tr>
<td>Minimum Watchdog Timeout Period</td>
<td>( t_{WPmin} )</td>
<td>( C_{SWT} = 680pF ) (Note 3)</td>
<td>6.8</td>
<td></td>
<td></td>
<td>ms</td>
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<td>Watchdog Timeout Period</td>
<td>( t_{WP} )</td>
<td>( C_{SWT} = 1200pF ) (Note 3)</td>
<td>12</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Maximum Watchdog Timeout</td>
<td>( t_{WPmax} )</td>
<td>( C_{SWT} = 22nF )</td>
<td>217.36</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>Watchdog Window</td>
<td>( D_{WDI} )</td>
<td>MAX16998B</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%( t_{WP} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX16998D</td>
<td>67.5</td>
<td>75</td>
<td>82.5</td>
<td></td>
</tr>
<tr>
<td>WDI to ENABLE Output Delay</td>
<td></td>
<td>Start from WDI third wrong trigger</td>
<td>100</td>
<td></td>
<td></td>
<td>( \mu )s</td>
</tr>
<tr>
<td>RESET Pullup Resistor Supply Voltage</td>
<td></td>
<td>(Note 5)</td>
<td>2.25</td>
<td>2.5</td>
<td>18.00</td>
<td>V</td>
</tr>
<tr>
<td>ENABLE Pullup Resistor Supply Voltage</td>
<td></td>
<td>(Note 5)</td>
<td>2.25</td>
<td>2.5</td>
<td>28.00</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 2:** \( R_{RESET} \) and \( R_{ENABLE} \) are external pullup resistors for open-drain outputs. Connect \( R_{RESET} \) and \( R_{ENABLE} \) to a minimum 2.5V voltage. Connect \( R_{RESET} \) to a maximum voltage of 18V and connect \( R_{ENABLE} \) to a maximum voltage of 28V.

**Note 3:** Calculated based on \( V_{RAMP} = 1.235V \) and \( I_{RAMP} = 500nA \).

**Note 4:** WDI pulses narrower than 1\( \mu \)s will be ignored. WDI pulses wider than 6.5\( \mu \)s will be recognized.

**Note 5:** Not production tested, guaranteed by design.

### Typical Operating Characteristics

\( C_{SWT} = C_{SRT} = 1500pF, \ T_A = +25^\circ C, \) unless otherwise noted.

---

**RESET TIMEOUT PERIOD** vs. \( C_{SRT} \)

**WATCHDOG TIMEOUT PERIOD** vs. \( C_{SWT} \)

**SUPPLY CURRENT** vs. \( \text{SUPPLY VOLTAGE} \)

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Typical Operating Characteristics (continued)

\( C_{SWT} = C_{SRT} = 1500\,\text{pF}, T_A = +25^\circ\text{C}, \) unless otherwise noted.

- **SUPPLY CURRENT** vs. TEMPERATURE
- **RESETIN/EN THRESHOLD VOLTAGE** vs. TEMPERATURE
- **RESETIN/EN THRESHOLD VOLTAGE** vs. SUPPLY VOLTAGE
- **RESETIN TO RESET DELAY** vs. TEMPERATURE
- **RESETIN/WATCHDOG PERIOD** vs. SUPPLY VOLTAGE
- **IRAMP** vs. TEMPERATURE
- **RESET OUTPUT VOLTAGE** vs. SINK CURRENT
- **ENABLE OUTPUT VOLTAGE** vs. SINK CURRENT
# MAX16997/MAX16998 High-Voltage Watchdog Timers with Adjustable Timeout Delay

## Pin Configuration

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX16997A</td>
<td>MAX16998A/B/D</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>IN</td>
</tr>
<tr>
<td>2</td>
<td>—</td>
<td>EN</td>
</tr>
<tr>
<td>3, 7</td>
<td>—</td>
<td>N.C.</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>SWT</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>WDI</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>ENABLE</td>
</tr>
<tr>
<td>—</td>
<td>2</td>
<td>RESETIN</td>
</tr>
<tr>
<td>—</td>
<td>3</td>
<td>SRT</td>
</tr>
<tr>
<td>—</td>
<td>7</td>
<td>RESET</td>
</tr>
</tbody>
</table>
### MAX16997/MAX16998 High-Voltage Watchdog Timers with Adjustable Timeout Delay

#### Timing Diagrams

**Figure 1. MAX16997A Timing Diagram**

- $t_{WP\text{ INITIAL}} = \text{WATCHDOG TIMEOUT PERIOD} \times 8$
- $t_{WP} = \text{WATCHDOG TIMEOUT PERIOD}$
- $t_{WDI} = \text{WDI TRIGGER PERIOD}$

3 CONSECUTIVE $t_{WP}$ WITHOUT TRIGGER ENABLE GOES LOW

3 CONSECUTIVE WATCHDOG TRIGGER (WDI) ENABLE GOES ACTIVE HIGH

**Figure 2. MAX16998A Timing Diagram**

- $t_{RESET} = \text{RESET TIMEOUT PERIOD}$
- $t_{WP} = \text{WATCHDOG TIMEOUT PERIOD}$
- $t_{WDI} = \text{WDI TRIGGER PERIOD}$

3 CONSECUTIVE RESETS ENABLE GOES ACTIVE LOW

3 CONSECUTIVE WATCHDOG TRIGGER (WDI) ENABLE GOES ACTIVE HIGH
Figure 3. MAX16998B/D Timing Diagram

Figure 4. RESETIN, RESET, VIN, ENABLE, and WDI Voltage Monitoring
Detailed Description
The MAX16997/MAX16998 are μP supervisory circuits for high-input-voltage and low-quiescent-current applications. These devices improve system reliability by monitoring the sub-system for software code execution errors. The MAX16997A/MAX16998A/B/D detect downstream circuit failures, and provide switchover to redundant circuitry. These devices provide complete adjustability for reset and watchdog functions.

The MAX16998A/B/D generate two output signals, RESET and ENABLE, that depend on the voltage level at RESETIN and the signal at WDI. RESET asserts whenever RESETIN drops below the selected reset threshold voltage. RESET remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. RESET also asserts for a period of tRESET when two consecutive WDI falling edges do not occur within the open window period. The MAX16997A generates one output signal (ENABLE) based on the voltage level at EN and the signal at WDI.

The MAX16997A/MAX16998A provide watchdog timeout adjustability with an external capacitor. The MAX16998A asserts RESET when two consecutive WDI falling edges do not occur within the watchdog timeout period. This device also asserts ENABLE if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI. ENABLE remains low until three consecutive good WDI falling edges occur. ENABLE does not assert if the voltage at RESETIN (EN) is below its threshold. For the MAX16997A, the watchdog timer starts timing if the voltage at EN is higher than a preset threshold level. Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period (tPON). Other than described above, the MAX16997A behaves the same as the MAX16998A.

The MAX16998B/MAX16998D contain a window watchdog timer that looks for activity outside an expected window of operation. The window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the adjusted watchdog timeout period.

Reset Output (RESET) (MAX16998A/B/D)
The reset output is typically connected to the reset input of the μC to start or restart it in a known state. The MAX16998A/B/D provide an active-low open-drain reset logic to prevent code execution errors.

For the MAX16998A/B/D, RESET asserts whenever RESETIN drops below the selected reset threshold voltage (V_{PON}). RESET remains low for the reset timeout period after RESETIN exceeds the selected threshold voltage, and then goes high.

The MAX16998A asserts RESET for a period of tRESET when two consecutive WDI falling edges do not occur within the adjusted watchdog timeout period. The MAX16998B/D also assert RESET for a period of tRESET when a WDI falling edge does not occur within the open window period. Anytime reset asserts, the watchdog timer clears. At the end of the reset timeout period, RESET goes high, and the watchdog timer is restarted from zero (see the Selecting the Watchdog Timeout Capacitor section).

Enable Output (ENABLE)
If the μC fails to operate correctly (e.g., the software execution is stuck in a loop), WDI does not trigger any more and RESET pulls low, resetting the μC. If the μC does not work properly in the next loop either, the device asserts ENABLE again. After three watchdog timeout periods elapse with no falling edges at WDI, ENABLE asserts and flags a backup circuit that can take over the operation.

ENABLE remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout occur. ENABLE does not assert if the voltage at RESETIN (EN) is below its threshold. These devices are guaranteed to be in correct ENABLE output logic state when V_{IN} remains greater than 1.1V.

Power-On/Power-Off Sequence
Figure 5 shows the power-up and power-down sequence for RESET and ENABLE for the MAX16998A/B/D. On power-up, once V_{IN} reaches 1.1V, RESET goes logic-low. As RESETIN rises, RESET remains low. When RESETIN rises above V_{PON}, the reset timer starts and RESET remains low. When the reset timeout period ends, RESET goes high.

For proper RESET operation, V_{IN} must rise above the minimum operating voltage of 5V for longer than 270μs before the RESETIN signal crosses the V_{PON} rising threshold of 1.135V (minimum). See Figure 6 for details.

On power-down, once RESETIN goes below V_{PON}, RESET goes low and remains low until V_{IN} drops below 1.1V. Figure 6 shows the detailed power-up sequence for the MAX16998A/B/D.
Figure 5. Power-On Reset and Power-Down Reset for the MAX16998A/B/D

THE THREE CONSECUTIVE RESET COULD BE CAUSED BY THREE TIMEOUTS AS SHOWN HERE OR BY THREE WDI FALLING EDGE OUTSIDE THE OPEN WINDOW, OR A COMBINATION OF ANY RESET CONDITIONS EXCEPT VRESETIN DROPS TOO LOW.

Figure 6. Detailed Power-Up Sequence for the MAX16998A/B/D

WDI CLEAR AND STARTS COUNTING FROM 0
MAX16997/MAX16998

RESETPIN Input (MAX16998A/B/D)
The MAX16998A/B/D monitor the voltage at RESETPIN using an adjustable reset threshold, set with an external resistive divider (see Figure 7). RESET asserts when VRESETPIN is below 1.235V.
Use the following equations to calculate the externally monitored voltage (VCC).

\[
V_{\text{TH}} = V_{\text{PON}} \left[ \frac{R_1}{R_2} + 1 \right]
\]

where \(V_{\text{TH}}\) is the desired reset threshold voltage, and \(V_{\text{PON}} = 1.235\text{V}\). To simplify the resistor selection, choose a value for \(R_2\) (< than 1MΩ) and calculate \(R_1\).

\[
R_1 = R_2 \left[ \frac{V_{\text{TH}}}{V_{\text{PON}}} - 1 \right]
\]

EN Input
The MAX16997A provides a high-impedance input (EN) to the enable comparator. Based on the voltage level at EN, the watchdog timer is turned on or off. The watchdog timer starts timing if the voltage level at EN is higher than a preset threshold voltage (VPPN). Each time the voltage at EN rises from below to above the preset threshold voltage, the initial watchdog timeout period is 8 times the normal watchdog timeout period (tWP).

Watchdog Timer
MAX16997A
The watchdog circuit monitors the µC’s activity. For the MAX16997A, the watchdog timer starts timing once the voltage at EN is higher than a preset threshold voltage. ENABLE asserts if three consecutive watchdog timeout periods have elapsed without a falling edge at WDI. ENABLE remains low until three consecutive WDI falling edges with periods shorter than the watchdog timeout period occur (see Figure 2).

The internal watchdog timer is cleared by a RESET rising edge or by a falling edge at WDI. The watchdog timer remains cleared while RESET is asserted; as soon as RESET is released, the timer starts counting. WDI falling edges are ignored when RESET is low. If no WDI falling edge occurs within the watchdog timeout period, RESET immediately goes low and stays low for the adjusted reset timeout period.

MAX16998B/D
The MAX16998B/D have a windowed watchdog timer. The watchdog timeout period (tWP) is the sum of a closed window period (tCW) and an open window period (tOW). If the µC issues a WDI falling edge within the open window period, RESET stays high. Once a WDI falling edge occurs within the closed window period, RESET immediately goes low and stays low for the adjusted reset timeout period (see Figure 3). If no WDI falling edge occurs within the watchdog timeout period, RESET immediately goes low and stays low for the adjusted reset timeout period. The open window size is factory-set to 50% of the watchdog timeout period for the MAX16998B and 75% for the MAX16998D.

Figure 8 shows a WDI falling edge identified as a good or a bad WDI signal edge. In case 1, the WDI falling edge occurs within the closed window period and is considered a bad WDI falling edge (early fault); therefore, it asserts RESET. Case 2 also shows another fault. In this case,
no WDI falling edge occurs within the watchdog timeout period (t_{WP}) and is considered a late fault that asserts RESET. In case 3, the WDI falling edge occurs within the open window period and is considered a good WDI signal falling edge. In this case, RESET stays high. In case 4, the WDI falling edge occurs within the indeterminate region. In this case, the RESET state is indeterminate.

These devices assert ENABLE after three consecutive bad WDI falling edges. ENABLE returns high after three consecutive good WDI signal falling edges (see Figure 3).

Either a rising edge at RESET or a falling edge at WDI clears the internal watchdog timer. The watchdog timer remains cleared while RESET is asserted. The watchdog timer begins counting when RESET goes high. WDI falling edges are ignored when RESET is low.

### Applications Information

#### Selecting the Reset Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RESET}) by connecting a capacitor (C_{SRT}) between SRT and ground. See the Reset Timeout Period vs. C_{SRT} graph in the Typical Operating Characteristics section. Calculate the reset timeout capacitance using the equation below:

\[
C_{SRT} = t_{RESET} \times \frac{I_{RAMP}}{V_{RAMP}}
\]

where \(V_{RAMP}\) is in volts, \(I_{RAMP}\) is in nA, and \(C_{SRT}\) is in nF.

Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SRT may cause errors in the reset timeout period. If precise time control is required, use capacitors with low leakage current and high stability.

#### Selecting the Watchdog Timeout Capacitor

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer determines how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WP}) by connecting a capacitor (C_{SWT}) between SWT and GND. For normal mode operation, calculate the watchdog timeout capacitance using the following equation:

\[
C_{SWT} = t_{WP} \times \frac{I_{RAMP}}{4 \times V_{RAMP}}
\]

where \(V_{RAMP}\) is in volts, \(I_{RAMP}\) is in nA, and \(C_{SWT}\) is in nF. See the Watchdog Timeout Period vs. C_{SWT} graph in the Typical Operating Characteristics section.

For the MAX16998B/MAX16998D, the open window size is factory-set to 50% (MAX16998B) or 75% (MAX16998D) of the watchdog period. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at SWT may cause errors in the watchdog timeout period. If precise time control is required, use capacitors with low leakage current and high stability. To disable the watchdog timer function, connect SWT to ground and connect WDI to either the high- or low-logic state.

![Figure 8. The MAX16998B/D Window Watchdog Diagram](image)
Interfacing to Other Voltages for Logic Compatibility

As shown in Figure 9, the open-drain RESET output can operate in the 2.5V to 18V range. This allows the device to interface a µP with other logic levels.

WDI Glitch Immunity

For additional glitch immunity, connect an RC lowpass filter as close as possible to WDI (see Figure 10).

For example, for glitches with duration of 1μs, a 12kΩ resistor and a 47pF capacitor will provide immunity.

Layout Considerations

SRT and SWT are connected to internal precision current sources. When developing the layout for the application, minimize stray capacitance attached to SRT and SWT as well as leakage currents that can reach those nodes. SRT and SWT traces should be as short as possible. Route traces carrying high-speed digital signals and traces with large voltage potentials as far from SRT and SWT as possible. Leakage currents and stray capacitance (e.g., a scope probe, which induces both) at these pins may cause errors in the reset and/or watchdog timeout period.

When evaluating these parts, use clean prototype boards to ensure accurate reset and watchdog timeout periods.

RESETIN is a high-impedance input and a high-impedance resistive divider (e.g., 100kΩ to 1MΩ) sets the threshold level. Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESETIN (e.g., a scope probe) causes errors in the programmed reset threshold.

Typical Operating Circuits

RESET remains asserted as long as RESETIN is below the regulated voltage and for the reset timeout period after RESETIN goes high to assure that the monitored LDO voltage is settled. Then, the µC starts operating and triggers WDI.

If the µC fails to operate correctly (e.g., the software execution is stuck in a loop), the WDI signal does not trigger the watchdog timer any more, and RESET is pulled low, resetting the µC. If the µC does not work properly in the next loop either, the device asserts RESET again. After three watchdog timeout periods with no WDI falling edges, ENABLE asserts and flags backup or safety circuits that take over the operation.
Figure 11. MAX16998A/B/D Switch Over to Backup Circuitry

Figure 12. MAX16997A Application Diagram
MAX16997/MAX16998 High-Voltage Watchdog Timers with Adjustable Timeout Delay

Pin Configurations

Chip Information
PROCESS: BiCMOS

Package Information
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

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## Revision History

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<td>—</td>
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<tr>
<td>1</td>
<td>4/09</td>
<td>Added bullet to Features section, revised Electrical Characteristics table</td>
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<td>Changes to Power-on/Power-off Sequence section and updated Figure 6</td>
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