General Description

The MAX15021 is a dual-output, pulse-width-modulated (PWM), step-down DC-DC regulator with tracking (coincident and ratiometric) and sequencing options. The device operates from 2.5V to 5.5V and each output can be adjusted from 0.6V to the input supply (V\textsubscript{AVIN}). The MAX15021 delivers up to 4A (regulator 1) and 2A (regulator 2) of output current. This device offers the ability to adjust the switching frequency from 500kHz to 4MHz and provides the capability of optimizing the design in terms of size and performance.

The MAX15021 utilizes a voltage-mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types. The dual switching regulators operate 180° out-of-phase, thereby reducing the RMS input ripple current and thus the size of the input bypass capacitor significantly.

The MAX15021 offers the ability to track (coincident or ratiometric) or sequence during power-up and power-down operation. When sequencing, it powers up glitch-free into a prebiased output.

Additional features include an internal undervoltage lockout with hysteresis and a digital soft-start/soft-stop for glitch-free power-up and power-down. Protection features include lossless cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

The MAX15021 is available in a space-saving, 5mm x 5mm, 28-pin TQFN-EP package and is specified for operation from -40°C to +125°C temperature range.

Applications

- RFID Reader Cards
- Power-over-Ethernet (PoE) IP Phones
- Automotive Multimedia
- Multivoltage Supplies
- Networking/Telecom

Benefits and Features

- Integration Reduces Power-Supply Footprint for Space-Constrained Designs
- Dual-Output Synchronous Buck Regulators
- Integrated Switches for 4A and 2A Output Currents
- Programmable Switching Frequency from 500kHz to 4MHz
- 28-Pin TQFN Package (5mm x 5mm)
- 180° Out-Of-Phase Operation Reduces Input Ripple Current and Thus the Size of the Input Bypass Capacitors
- Sophisticated Tracking/Sequencing Functions Facilitate Reliable Processor Operation
- Digital Soft-Start and Soft-Stop for Tracking Applications
- Digital Soft-Start into a Prebiased Load for Sequencing Applications
- Sequencing or Coincident/Ratiometric Tracking
- Flexible Enough for Use in a Range of Designs
  - 2.5V to 5.5V Input Voltage Range
  - Output-Voltage Adjustable from 0.6V to V\textsubscript{AVIN}
  - External Compensation for Maximum Flexibility
  - 100% Maximum Duty Cycle
- Integrated Protection Features Save Space and Increase Reliability
  - Lossless, Cycle-by-Cycle Current Sensing
  - Thermal Shutdown and Hiccup-Mode Short-Circuit Protection
- 20µA Shutdown Current Extends Battery Life in Portable Applications

Pin Configuration

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX15021ATI/V+</td>
<td>-40°C to +125°C</td>
<td>28 TQFN-EP*</td>
</tr>
</tbody>
</table>


Ordering Information


er={\text{TOP VIEW}}
Absolute Maximum Ratings

AVIN, PVIN1, PVIN2, DVDD1, EN1, FB1, RT1,
SEL to SGND.................................................................-0.3V to +6V
COMP1 to SGND.......................................................-0.3V to (VAVIN + 0.3V)
PGND1 to SGND.............................................................-0.3V to +0.3V
LX1 Current (Note 1)..................................................6A
Regulator 1.................................................................6A
Regulator 2.................................................................3A
Current into Any Pin other than PVIN1,
LX1, and PGND1.....................................................50mA

Continuous Power Dissipation (TJA = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) ....2758.6mW
Junction-to-Case Thermal Resistance (θJC)(Note 2) ...2°C/W
Junction-to-Ambient Thermal Resistance (θJA)(Note 2) ...29°C/W
Operating Temperature Range .................................-40°C to +125°C
Maximum Junction Temperature .................................+150°C
Storage Temperature Range .......................................-60°C to +150°C
Lead Temperature (soldering, 10s) ...............................+300°C

Note 1: LX1 has internal diodes to PGND1 and PVIN2. Applications that forward bias these diodes should take care not to exceed
the IC’s package power dissipation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-
layer board. For detailed information on package thermal considerations see www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional
operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to
absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(\text{VAVIN} = \text{VPVIN1} = \text{VPVIN2} = \text{VDVDD1} = \text{VDVDD2} = 3.3\text{V}, \text{VPGND1} = \text{VPGND2} = 0\text{V}, \text{RT1} = 25\text{kΩ}, \text{RT2} = 25\text{kΩ}, \text{TJ} = -40°C to +125°C, unless otherwise noted.
Typical values are at TA = +25°C.) (Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSTEM SPECIFICATIONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input-Voltage Range</td>
<td>\text{VAVIN} = \text{VPVIN1} = \text{VPVIN2} = \text{VDVDD1} = \text{VDVDD2}</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout Threshold</td>
<td>AVIN rising</td>
<td>2.1</td>
<td>2.2</td>
<td>2.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout Hysteresis</td>
<td></td>
<td>0.12</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Supply Current</td>
<td>\text{VEN1} = 1.3V, \text{VF1} = 0.8V</td>
<td>3.5</td>
<td>6</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>\text{VEN1} = 0V</td>
<td>20</td>
<td>65</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM DIGITAL SOFT-START/SOFT-STOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft-Start/Soft-Stop Duration</td>
<td></td>
<td>4096</td>
<td></td>
<td></td>
<td>Clock Cycles</td>
<td></td>
</tr>
<tr>
<td>Reference Voltage Steps</td>
<td></td>
<td>64</td>
<td></td>
<td></td>
<td>Steps</td>
<td></td>
</tr>
<tr>
<td>PWM ERROR AMPLIFIERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB1, FB2 Input Bias Current</td>
<td></td>
<td>-1</td>
<td></td>
<td>+1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>FB1, FB2 Voltage Set-Point</td>
<td></td>
<td>0.593</td>
<td>0.599</td>
<td>0.605</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>COMP1, COMP2 Voltage Range</td>
<td>\text{ICOMP1} = -250µA to +250µA</td>
<td>0.3</td>
<td>\text{VAVIN} - 0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error-Amplifier Open-Loop Gain</td>
<td></td>
<td>80</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Error-Amplifier Unity-Gain</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>MHz</td>
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<tr>
<td>POWER MOSFETs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 1 p-Channel MOSFET</td>
<td>\text{VDVDD1} = 5V</td>
<td>50</td>
<td>90</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 1 n-Channel MOSFET</td>
<td>\text{VDVDD1} = 5V</td>
<td>30</td>
<td>50</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 1 Gate Charge</td>
<td>\text{VDVDD1} = 5V</td>
<td>8</td>
<td></td>
<td>nC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum LX1 RMS Current</td>
<td></td>
<td>4</td>
<td></td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 2 p-Channel MOSFET</td>
<td>\text{VDVDD2} = 5V</td>
<td>100</td>
<td>180</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 2 n-Channel MOSFET</td>
<td>\text{VDVDD2} = 5V</td>
<td>60</td>
<td>100</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulator 2 Gate Charge</td>
<td>\text{VDVDD2} = 5V</td>
<td>4</td>
<td></td>
<td>nC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum LX2 RMS Current</td>
<td></td>
<td>2</td>
<td></td>
<td>A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

www.maximintegrated.com
Electrical Characteristics (continued)

(V_{AVIN} = V_{PGND_} = V_{SGND_} = 3.3V, V_{PGND_} = V_{SGND_} = 0V, R_T = 25k \Omega, and T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3).

<table>
<thead>
<tr>
<th>PARAMETER SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM CURRENT LIMIT AND HICCUP MODE</td>
<td>V_{AVIN} = 3.3V</td>
<td>4.5</td>
<td>4.9</td>
<td>5.3</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 2.5V</td>
<td>3.4</td>
<td>3.65</td>
<td>3.95</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 3.3V</td>
<td>4.0</td>
<td>4.9</td>
<td>5.65</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 2.5V</td>
<td>3.0</td>
<td>3.7</td>
<td>4.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 3.3V</td>
<td>2.25</td>
<td>2.45</td>
<td>2.65</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 2.5V</td>
<td>1.70</td>
<td>1.85</td>
<td>1.98</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 3.3V</td>
<td>2.0</td>
<td>2.5</td>
<td>2.83</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>V_{AVIN} = 2.5V</td>
<td>1.5</td>
<td>1.85</td>
<td>2.13</td>
<td></td>
</tr>
<tr>
<td>Number of Cumulative Current-Limit Events to Hiccup</td>
<td>NCL</td>
<td>4</td>
<td></td>
<td></td>
<td>Clock Cycles</td>
</tr>
<tr>
<td>Number of Consecutive Noncurrent Limit Cycles to Clear NCL</td>
<td>NCLR</td>
<td>3</td>
<td></td>
<td></td>
<td>Clock Cycles</td>
</tr>
<tr>
<td>Hiccup Timeout</td>
<td>N_HT</td>
<td>8192</td>
<td></td>
<td></td>
<td>Clock Cycles</td>
</tr>
<tr>
<td>ENABLE/SEL</td>
<td>EN_ Threshold</td>
<td>V_{EN_} rising</td>
<td>1.207</td>
<td>1.225</td>
<td>1.243</td>
</tr>
<tr>
<td></td>
<td>EN_ Hysteresis</td>
<td></td>
<td>0.12</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN_ Input Current</td>
<td></td>
<td>-2.5</td>
<td></td>
<td>+2.5</td>
</tr>
<tr>
<td></td>
<td>SEL High Threshold</td>
<td>0.85 x V_{AVIN}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SEL Low Threshold</td>
<td>0.2 x V_{AVIN}</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SEL Input Bias Current</td>
<td>Present only during startup</td>
<td>-100</td>
<td></td>
<td>+100</td>
</tr>
<tr>
<td>OSCILLATOR</td>
<td>Switching Frequency Range</td>
<td>f_{SW} = 3MHz x \left[ \frac{V_{RT}(V)}{1.067(V)} \right] (Note 4)</td>
<td>500</td>
<td>4000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillator Accuracy</td>
<td>f_{SW} \leq 1500kHz</td>
<td>-6</td>
<td></td>
<td>+6</td>
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<tr>
<td></td>
<td></td>
<td>f_{SW} &gt; 1500kHz</td>
<td>-10</td>
<td></td>
<td>+10</td>
</tr>
<tr>
<td></td>
<td>Phase Shift Between Regulators</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RT Current</td>
<td>0 &lt; V_{RT} &lt; 1.067V</td>
<td>31.30</td>
<td>32</td>
<td>32.58</td>
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<tr>
<td></td>
<td>RT Voltage Range</td>
<td>V_{RT}</td>
<td></td>
<td>0.13</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minimum Controllable On-Time</td>
<td></td>
<td></td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minimum Controllable Off-Time</td>
<td></td>
<td></td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PWM Ramp Amplitude</td>
<td>V_{AVIN}/4</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>PWM Ramp Valley</td>
<td></td>
<td></td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>THERMAL SHUTDOWN</td>
<td>Thermal Shutdown Temperature</td>
<td>Temperature rising</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 3: Specifications are 100% production tested at T_A = +25°C and T_A = +125°C. Maximum and minimum specifications over temperature are guaranteed by design.

Note 4: When operating with V_{AVIN} = 2.5V, the maximum switching frequency should be derated to 3MHz.
Typical Operating Characteristics

(VAVIN = VVD01 = VVD02 = VPVIN1 = VPVIN2 = 5V, VOUT1 = 3.3V, VOUT2 = 1.5V, VPGN0_ = 0V, RT = 16.5kΩ. TA = +25°C, unless otherwise noted.)
Typical Operating Characteristics (continued)

(V\textsubscript{VIN} = V\textsubscript{DVDD1} = V\textsubscript{DVDD2} = V\textsubscript{PVIN1} = V\textsubscript{PVIN2} = 5V, V\textsubscript{OUT1} = 3.3V, V\textsubscript{OUT2} = 1.5V, V\textsubscript{PGND} = 0V, R\textsubscript{T} = 16.5\, \Omega, T\textsubscript{A} = +25°C, unless otherwise noted.)
Typical Operating Characteristics (continued)

\( (V_{VIN} = V_{DVDD1} = V_{DVDD2} = V_{VPVIN1} = V_{VPVIN2} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.5V, V_{PGND} = 0V, R_T = 16.5\,\Omega, \; T_A = +25^\circ C, \) unless otherwise noted.)
## Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SEL</td>
<td>Track/Sequence Select Input. Connect SEL to ground to configure the device as a sequencer. Connect SEL to AVIN for tracking with output 1 as the master. Leave SEL unconnected for tracking with output 2 as the master. Use the output with the higher voltage as the master and the output with the lower voltage as the slave.</td>
</tr>
<tr>
<td>2, 7, 8</td>
<td>PGND1</td>
<td>Power Ground Connection for Regulator 1. Connect the negative terminals of the input and output filter capacitor to PGND1. Connect PGND1 externally to SGND at a single point, typically at the negative terminal of the input capacitor.</td>
</tr>
<tr>
<td>3, 6</td>
<td>LX1</td>
<td>Inductor Connection for Regulator 1. LX1 is the drain connection of the internal high-side p-channel MOSFET and the drain connection of the internal synchronous n-channel MOSFET for regulator 1.</td>
</tr>
<tr>
<td>4, 5</td>
<td>PVIN1</td>
<td>Input Supply Voltage for Regulator 1. Connect to an external voltage source from 2.5V to 5.5V. Bypass PVIN1 to PGND1 with a 1µF (min) ceramic capacitor.</td>
</tr>
<tr>
<td>9</td>
<td>DVDD1</td>
<td>Switch Driver Supply for Regulator 1. Connect externally to PVIN1.</td>
</tr>
<tr>
<td>10</td>
<td>EN1</td>
<td>Enable Input for Regulator 1. When configured as a sequencer, EN1 must exceed 1.225V (typ) for the PWM controller to begin regulating output 1. When configured as a tracker, connect EN1 to the center tap of a resistive divider from the regulator 2 output.</td>
</tr>
<tr>
<td>11</td>
<td>FB1</td>
<td>Feedback Regulation Point for Regulator 1. Connect FB1 to the center tap of a resistive divider from the regulator 1 output to SGND to set the output voltage. The FB1 voltage regulates to 0.6V (typ).</td>
</tr>
<tr>
<td>12</td>
<td>COMP1</td>
<td>Error-Amplifier Output for Regulator 1. Connect COMP1 to the compensation feedback network.</td>
</tr>
<tr>
<td>13, 14, 15, 20, 21, 22</td>
<td>N.C.</td>
<td>No Connection. Do not connect.</td>
</tr>
<tr>
<td>16</td>
<td>DVDD2</td>
<td>Switch Driver Supply for Regulator 2. Connect externally to PVIN2.</td>
</tr>
<tr>
<td>17</td>
<td>PGND2</td>
<td>Power Ground Connection for Regulator 2. Connect the negative terminals of the input and output filter capacitors to PGND2. Connect PGND2 externally to SGND at a single point, typically at the negative terminal of the input capacitor.</td>
</tr>
<tr>
<td>18</td>
<td>LX2</td>
<td>Inductor Connection for Regulator 2. LX2 is the drain connection of the internal high-side p-channel MOSFET and the drain connection of the internal synchronous n-channel MOSFET for regulator 2.</td>
</tr>
<tr>
<td>19</td>
<td>PVIN2</td>
<td>Input Supply Voltage for Regulator 2. Connect to an external voltage source from 2.5V to 5.5V. Bypass PVIN2 to PGND2 with a 1µF (min) ceramic capacitor.</td>
</tr>
<tr>
<td>23</td>
<td>COMP2</td>
<td>Error-Amplifier Output for Regulator 2. Connect COMP2 to the compensation feedback network.</td>
</tr>
<tr>
<td>24</td>
<td>FB2</td>
<td>Feedback Regulation Point for Regulator 2. Connect to the center tap of a resistive divider from the regulator 2 output to SGND to set the output voltage. The FB2 voltage regulates to 0.6V (typ).</td>
</tr>
<tr>
<td>25</td>
<td>EN2</td>
<td>Enable Input for Regulator 2. When configured as a sequencer, EN2 must exceed 1.225V (typ) for the PWM controller to begin regulating output 2. When configured as a tracker, connect EN2 to the center tap of a resistive divider from the regulator 1 output.</td>
</tr>
<tr>
<td>26</td>
<td>SGND</td>
<td>Signal Ground. Connect SGND to PGND_ at a single point, typically near negative terminal of the input bypass capacitor.</td>
</tr>
<tr>
<td>27</td>
<td>AVIN</td>
<td>Input Voltage. Bypass AVIN to SGND with a 100nF (min) ceramic capacitor.</td>
</tr>
<tr>
<td>28</td>
<td>RT</td>
<td>Oscillator Timing Resistor Connection. Connect a 4.2kΩ to 33kΩ resistor from RT to SGND to program the switching frequency from 500kHz to 4MHz.</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>Exposed Pad. Connect EP to a large copper plane at SGND potential to improve thermal dissipation. Do not use as the main SGND connection.</td>
</tr>
</tbody>
</table>
Functional Diagrams
Functional Diagrams (continued)
Detailed Description

The MAX15021 incorporates dual-output, PWM, step-down, DC-DC regulators with tracking and sequencing options. The device operates over the input-voltage range of 2.5V to 5.5V. Each PWM regulator provides an adjustable output down to 0.6V and delivers up to 4A (regulator 1) and 2A (regulator 2) of load current. The high switching frequency (up to 4MHz) and integrated power switches optimize the MAX15021 for high-performance and small-size power management solutions.

Each of the MAX15021 PWM regulator sections utilizes a voltage-mode control scheme for good noise immunity and offers external compensation allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The device operates at a fixed switching frequency that is programmable from 500kHz to 4MHz with a single resistor. Operating the regulators with 180° out-of-phase clocking, and at frequencies up to 4MHz, significantly reduces the RMS input ripple current. The resulting peak input current reduction (and increase in the ripple frequency) significantly reduces the required amount of input bypass capacitance.

The MAX15021 provides coincident tracking, ratiometric tracking, or sequencing to allow tailoring of power-up/power-down sequence depending on the system requirements. When sequencing, it powers up glitch-free into a prebiased output.

The MAX15021 includes internal undervoltage lockout with hysteresis, digital soft-start/soft-stop for “glitch-free” power-up and power-down. Protection features include lossless, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

Undervoltage Lockout (UVLO)

The supply voltage (V_{AVIN}) must exceed the default UVLO threshold before any operation starts. The UVLO circuitry keeps the MOSFET drivers, oscillator, and all the internal circuitry shut down to reduce current consumption. The UVLO rising threshold is 2.2V (typ) with a 120mV (typ) hysteresis.

Digital Soft-Start/Soft-Stop

The MAX15021 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output-voltage overshoot. Soft-start begins after V_{AVIN} exceeds the undervoltage lockout threshold and the enable input is above 1.225V (typ). The soft-start circuitry ramps up the reference voltage, controlling the rate of rise of the output voltage, and reducing input surge currents during startup. The soft-start duration is 4096 clock cycles. The output voltage is incremented through 64 equal steps. The output reaches regulation when soft-start is completed, regardless of the output capacitance and load.

For tracking applications, soft-stop commences when the enable input falls below 1.1V (typ). The soft-stop circuitry ramps down the reference voltage controlling the output-voltage rate of fall. The output voltage is decremented through 64 equal steps in 4096 clock cycles.

Oscillator

Use an external resistor at RT to program the MAX15021 switching frequency from 500kHz to 4MHz. Calculate the appropriate resistor at RT for the desired output switching frequency (f_{SW}):

\[
RT [\Omega] = \frac{f_{SW} [kHz] \times 1.067 [V]}{32 [\mu A] \times 4 [MHz]}
\]

Tracking/Sequencing

The MAX15021 features coincident/ratiometric tracking and sequencing (see Figure 1). Connect SEL to ground to configure the device as sequencer. Connect SEL to AVIN for tracking with output 1 as the master. Leave SEL unconnected for tracking with output 2 as the master. Assign the output with the higher voltage as the master.

Figure 1. Graphical Representation of Coincident Tracking, Ratiometric Tracking, and Sequencing
Coincident/Ratiometric Tracking
The enable inputs in conjunction with digital soft-start and soft-stop provide coincident/ratiometric tracking. Track an output voltage by connecting a resistive divider from the output being tracked to its enable input. For example, for V\textsubscript{OUT2} to coincidentally track V\textsubscript{OUT1}, connect the same resistive divider used for FB2, from V\textsubscript{OUT1} to EN2 to SGND (see Figure 2).

Track ratiometrically by connecting EN\textsubscript{n} to SGND. This synchronizes the soft-start and soft-stop of all the regulator references, and hence their respective output voltages will track ratiometrically (see Figure 2).

When the MAX15021 regulators are configured as voltage trackers, output short-circuit fault conditions at either master or slave output are handled carefully—neither the master nor slave output will remain energized when the other output is shorted to ground. When the slave is shorted and enters hiccup mode, the master will soft-stop. When the master is shorted and the part enters in hiccup mode, the slave will ratiometrically soft-stop. Coming out of hiccup mode, both outputs will soft-start coincidently or ratiometrically depending on their initial configuration. During the thermal shutdown or power-off when the input falls below its UVLO, the output voltages decrease at a rate depending on the respective output capacitance and load.

See Figure 1 for a graphical representation of coincident/ratiometric tracking.

Sequencing
When sequencing, the voltage at the enable inputs must exceed 1.225V (typ) for each PWM controller to start (see Figure 1c).
Error Amplifier
The output of the internal voltage-mode error amplifier (COMP_) is provided for frequency compensation (see the Compensation-Design Guidelines section). FB_ is the inverting input of the error amplifier. The error amplifier has an 80dB open-loop gain and a 12MHz gain bandwidth (GBW) product.

Output Short-Circuit Protection (Hiccup Mode)
The MAX15021 features lossless, high-side peak current limit and low-side, valley current limit. At short duty cycles, both limits are active. At high duty cycles, only the high-side peak current limit is active. Either limit causes the hiccup mode count (NCL) to increment.

For duty cycles less than 50%, the low-side valley current limit is active. Once the high-side MOSFET turns off, the voltage across the low-side MOSFET is monitored. If this voltage does not exceed the current-limit threshold at the end of the cycle, the high-side MOSFET turns on normally at the start of the next cycle. If the voltage exceeds the current-limit threshold just before the beginning of a new PWM cycle, the controller skips that cycle. During severe overload or short-circuit conditions, the switching frequency of the device appears to decrease because the on-time of the low-side MOSFET extends beyond a clock cycle.

If the current-limit threshold is exceeded for more than four cumulative clock cycles (NCL), the device shuts down for 8192 clock cycles (hiccup timeout) and then restarts with a soft-start sequence. If three consecutive cycles pass without a current-limit event, the count of NCL is cleared (see Figure 3). Hiccup mode protects the device against a continuous output short circuit.

The internal current limit is constant from 5.5V down to 3V and decreases linearly by 50% from 3V to 2V. See the Electrical Characteristics table.

Thermal-Overload Protection
The MAX15021 features an integrated thermal-overload protection with temperature hysteresis. Thermal-overload protection limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C, an internal thermal sensor shuts down the device, turning off the internal power MOSFETs and allowing the die to cool. After the die temperature falls by +15°C, the part restarts with a soft-start sequence.

Startup into a Prebiased Output (Sequencing Mode)
In sequencing mode, the regulators start into a prebiased output and soft-stop is disabled. During soft-start, the complementary switching sequence is inhibited until the PWM comparator commands its first PWM pulse. Until then, the converters do not sink current from the outputs. The first PWM pulse occurs when the ramping reference voltage increases above the FB_ voltage.

PWM Controllers Design Procedure
Setting the Switching Frequency
Connect a 4.2kΩ to 33kΩ resistor from RT to SGND to program the switching frequency from 500kHz to 4MHz. Calculate the resistor connected to RT using the following equation:

\[
RT[k\Omega] = \frac{fSW[kHz] \times 1.067[V]}{32[\mu A] \times 4[MHz]}
\]

Higher frequencies allow designs with lower inductor values and less output capacitance. At higher switching frequencies core losses, gate-charge currents, and switching losses increase. When operating from VAVIN ≤ 3V, the switching frequency (fSW) should be derated to 3MHz (maximum).

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Effective Input-Voltage Range

Although the MAX15021's regulators can operate from input supplies ranging from 2.5V to 5.5V, the input-voltage range can be effectively limited by the MAX15021's duty-cycle limitations for a given output voltage (V\text{OUT}_\text{..}). The maximum input voltage (VP\text{VIN}_\text{MAX}) can be effectively limited by the controllable minimum on-time (t\text{ON(MIN)}):

\[
VP\text{VIN}_\text{MAX}[V] \leq \frac{V\text{OUT}_\text{..}[V]}{t\text{ON(MIN)}[\mu s] \times f\text{SW}[MHz]}
\]

where t\text{ON(MIN)} is 0.06\mu s (typ).

The minimum input voltage (VP\text{VIN}_\text{MIN}) can be effectively limited by the maximum controllable duty cycle and is calculated using the following equation:

\[
VP\text{VIN}_\text{MIN}[V] \geq \frac{V\text{OUT}_\text{..}[V]}{1-(t\text{OFF(MIN)}[\mu s] \times f\text{SW}[MHz])}
\]

where V\text{OUT}_\text{..} is the regulator output voltage and t\text{OFF(MIN)} is the 0.06\mu s (typ) controllable off-time.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15021: inductance value (L), peak inductor current (I\text{PEAK}), and inductor saturation current (I\text{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (\Delta I\text{P-P}). Higher \Delta I\text{P-P} allows for a lower inductor value. A lower inductance minimizes size and cost and improves large-signal and transient response. However, efficiency is reduced due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. A higher inductance increases efficiency by reducing the ripple current; however, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions. Choose the inductor’s peak-to-peak current, \Delta I\text{P-P}, in the range of 20% to 50% of the full load current; as a rule of thumb 30% is typical.

Calculate the inductance, L, using the following equation:

\[
L[\mu H] = \frac{V\text{OUT}_\text{..}[V] \times (VP\text{VIN}_\text{..}[V] - V\text{OUT}_\text{..}[V])}{VP\text{VIN}_\text{..}[V] \times f\text{SW}[MHz] \times \Delta I\text{P-P}[A]}
\]

where VP\text{VIN}_\text{..} is the input supply voltage, V\text{OUT}_\text{..} is the regulator output voltage, and f\text{SW} is the switching frequency. Use typical values for VP\text{VIN}_\text{..} and V\text{OUT}_\text{..} so that efficiency is optimum for typical conditions. The switching frequency (f\text{SW}) is programmable between 500kHz and 4MHz (see the Oscillator section).

The peak-to-peak inductor current (\Delta I\text{P-P}), which reflects the peak-to-peak output ripple, is largest at the maximum input voltage. See the Output-Capacitor Selection section to verify that the worst-case output current ripple is acceptable.

Select an inductor with a saturation current, I\text{SAT}, higher than the maximum peak current to avoid runaway current during continuous output short-circuit conditions. Also, confirm that the inductor’s thermal performance and projected temperature rise above ambient does not exceed its thermal capacity. Many inductor manufacturers provide bias/load current versus temperature rise performance curves (or similar) to obtain this information.

Input-Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents and therefore, the input capacitor must be carefully chosen to withstand the input ripple current and keep the input-voltage ripple within design requirements.

The input-voltage ripple is comprised of \Delta V\text{Q} (caused by the capacitor discharge) and \Delta V\text{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of \Delta V\text{Q} and \Delta V\text{ESR} which peaks at the end of the on-cycle. Calculate the required input capacitance and ESR for a specified ripple using the following equations:

\[
ESR[\Omega] = \frac{\Delta V\text{ESR}[mV]}{\left(I\text{LOAD(MAX)} + \frac{\Delta I\text{P-P}}{2}\right)[A]}
\]

\[
C\text{PVIN}_\text{..}[\mu F] = \frac{\Delta V\text{Q}[V] \times f\text{SW}[MHz]}{V\text{PVIN}_\text{..}[V] \times V\text{OUT}_\text{..}[V]}
\]

\[
\Delta I\text{P-P}[A] = \frac{(VP\text{VIN}_\text{..} - V\text{OUT}_\text{..})[V] \times V\text{OUT}_\text{..}[V]}{VP\text{VIN}_\text{..}[V] \times f\text{SW}[MHz] \times L[\mu H]}
\]

I\text{LOAD(MAX)} is the maximum output current, \Delta I\text{P-P} is the peak-to-peak inductor current, and VP\text{VIN}_\text{..} is the input supply voltage, V\text{OUT}_\text{..} is the regulator output voltage, and f\text{SW} is the switching frequency.
Use the following equation to calculate the input ripple when only one regulator is enabled:

\[ I_{\text{CIN(RMS)[A]}} = I_{\text{LOAD(MAX)[A]}} \times \sqrt{\frac{V_{\text{OUT}[V]} \times (V_{\text{PIN}} - V_{\text{OUT}}[V])}{V_{\text{PIN}[V]}}} \]

The MAX15021 includes UVLO hysteresis to avoid possible unintentional chattering during turn-on. Use additional bulk capacitance if the input source impedance is high. If using a lower input voltage, additional input capacitance helps to avoid possible undershoot below the undervoltage lockout threshold during transient loading.

**Output-Capacitor Selection**

The allowed output-voltage ripple and the maximum deviation of the output voltage during load steps determine the required output capacitance and its ESR. The output ripple is mainly composed of \( \Delta V_Q \) (caused by the capacitor discharge) and \( \Delta V_{ESR} \) (caused by the voltage drop across the equivalent series resistance of the output capacitor). The equations for calculating the output capacitance and its ESR are:

\[ C_{\text{OUT[\mu F]}} = \frac{\Delta l_{p-P}[A]}{8 \times \Delta V_Q[V] \times f_{SW}[\text{MHz}]} \]

\[ \text{ESR}[\text{m}\Omega] = \frac{2 \times \Delta V_{ESR}[\text{mV}]}{\Delta l_{p-P}[A]} \]

where \( \Delta l_{p-P} \) is the peak-to-peak inductor current, and \( f_{SW} \) is the switching frequency.

\( \Delta V_{ESR} \) and \( \Delta V_Q \) are not directly additive since they are out of phase from each other. If using ceramic capacitors, which generally have low ESR, \( \Delta V_Q \) dominates. If using electrolytic capacitors, \( \Delta V_{ESR} \) dominates.

The allowable deviation of the output voltage during fast load transients also affects the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with an increased duty cycle. The response time (t RESPONSE) depends on the gain bandwidth of the controller (see the Compensation-Design Guidelines section). The resistive drop across the output capacitor’s ESR (\( \Delta V_{ESR} \)), the drop across the capacitor’s ESL (\( \Delta V_{ESL} \)), and the capacitor discharge (\( \Delta V_Q \)) cause a voltage droop during the load-step (t RESPONSE). Use a combination of low-ESR tantalum/aluminum electrolyte and ceramic capacitors for better load transient and voltage ripple performance. Nonlead capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output voltage deviation below the tolerable limits of the electronics being powered.

Use the following equations to calculate the required output capacitance, ESR, and ESL for minimal output deviation during a load step:

\[ C_{\text{OUT[\mu F]}} = \frac{I_{\text{STEP}[A]} \times t_{\text{RESPONSE}[\mu s]}}{\Delta V_Q[V]} \]

\[ \text{ESL[nH]} = \frac{\Delta V_{ESL}[\text{mV}] \times I_{\text{STEP}[A]}}{t_{\text{RESPONSE}[\mu s]}} \]

where \( I_{\text{STEP}} \) is the load step, \( t_{\text{RESPONSE}} \) is the rise time of the load step, and \( t_{\text{RESPONSE}} \) is the response time of the controller.

**Compensation-Design Guidelines**

The MAX15021 uses a fixed-frequency, voltage-mode control scheme that regulates the output voltage by comparing the output voltage against a fixed reference. The subsequent “error” voltage that appears at the error-amplifier output (COMP_) is compared against an internal ramp voltage to generate the required duty cycle of the pulse-width modulator. A second-order lowpass LC filter removes the switching harmonics and passes the DC component of the pulse-width-modulated signal to the output. The LC filter has an attenuation slope of -40dB/decade and introduces 180° of phase shift at frequencies above the LC resonant frequency. This phase shift in addition to the inherent 180° of phase shift of the regulator’s negative feedback system turns the feedback into unstable positive feedback. The error amplifier and its associated circuitry must be designed to achieve a stable closed-loop system.

The basic controller loop consists of a power modulator (comprised of the regulator’s pulse-width modulator, associated circuitry, and LC filter), an output feedback divider, and an error amplifier. The power modulator has a DC gain set by \( V_{AVIN}/VRAMP \) where the ramp voltage (\( V_{RAMP} \)) is a function of the \( V_{AVIN} \) and results in a fixed DC gain of 4V/V, providing effective feed-forward compensation of input-voltage supply DC variations. The feed-forward compensation eliminates the dependency of the power modulator’s gain on the input voltage such that the feedback compensation of the error amplifier requires no modifications for nominal input-voltage changes. The output filter is effectively modeled as a double-pole and a single zero set by the output inductance (L), the DC resistance of the inductor (DCR), the output capacitance (\( C_{\text{OUT}} \)) and its equivalent series resistance (ESR).
Below are equations that define the power modulator:

\[
\text{Gain}_{\text{MOD(\text{DC})}} = \frac{V_{\text{AVIN}}}{V_{\text{RAMP}}} \approx \frac{V_{\text{AVIN}}}{4V/V}
\]

\[
f_{\text{LC}} = \frac{1}{2\pi \sqrt{L \times C_{\text{OUT}}} \left(\frac{R_{\text{OUT}} + \text{ESR}}{R_{\text{OUT}} + \text{DCR}}\right)} \approx \frac{1}{2\pi \sqrt{L \times C_{\text{OUT}}}}
\]

\[
f_{\text{ESR}} = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}}
\]

\(R_{\text{OUT}}\) is the load resistance of the regulator, \(f_{\text{LC}}\) is the resonant break frequency of the filter, and \(f_{\text{ESR}}\) is the ESR zero of the output capacitor. See the Closed-Loop Response and Compensation of Voltage-Mode Regulators section for more information on \(f_{\text{LC}}\) and \(f_{\text{ESR}}\).

The switching frequency (\(f_{\text{SW}}\)) is programmable between 500kHz and 4MHz. Typically, the crossover frequency (\(f_{\text{CO}}\))—the frequency at which the system’s closed-loop gain is equal to unity (crosses 0dB)—should be set at or below one-tenth the switching frequency (\(f_{\text{SW}}/10\)) for stable closed-loop response.

The MAX15021 provides an internal voltage-mode error amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each controller offers a wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use aluminum electrolytic capacitors while for space-sensitive applications, use low-ESR tantalum or multilayer ceramic chip (MLCC) capacitors at the output. The higher switching frequencies of the MAX15021 allow the use of MLCC as the primary filter capacitor(s).

First, select the passive and active power components that meet the application output ripple, component size, and component cost requirements. Second, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined below.

**Closed-Loop Response and Compensation of Voltage-Mode Regulators**

The power modulator’s LC lowpass filter exhibits a variety of responses, dependent on the value of the L and C and their parasitics. Higher resistive parasitics reduce the Q of the circuit, reducing the peak gain and phase of the system; however, efficiency is also reduced under these circumstances.

One such response is shown in Figure 4a. In this example, the ESR zero occurs relatively close to the filter’s resonant break frequency, \(f_{\text{LC}}\). As a result, the power modulator’s uncompensated crossover is approximately one-third the desired crossover frequency, \(f_{\text{CO}}\). Note also, the uncompensated rolloff through the 0dB plane follows a single-pole, -20dB/decade slope, and 90° of phase lag. In this instance, the inherent phase margin ensures a stable system; however, the gain-bandwidth product is not optimized.

**Figure 4a. Power Modulator Gain and Phase Response with Lossy Bulk Output Capacitor(s) (Aluminum)**

**Figure 4b. Power Modulator and Type II Compensator Gain and Phase Response with Lossy Bulk Output Capacitor(s) (Aluminum)**
As seen in Figure 4b, a Type II compensator provides for stable closed-loop operation, leveraging the +20dB/decade slope of the capacitor’s ESR zero, while extending the closed-loop gain-bandwidth of the regulator. The zero crossover now occurs at approximately three times the uncompensated crossover frequency, f_C0.

The Type II compensator’s midfrequency gain (approximately 12dB shown here) is designed to compensate for the power modulator’s attenuation at the desired crossover frequency, f_C0 (Gain_E/A + Gain_MOD = 0dB at f_C0). In this example, the power modulator’s inherent -20dB/decade rolloff above the ESR zero (f_ZERO,ESR) is leveraged to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 4b, the net result is a three times increase in the regulator’s gain bandwidth while providing greater than 75° of phase margin (the difference between Gain_E/A and Gain_MOD respective phases at crossover, f_C0).

Other filter schemes pose their own problems. For instance, when choosing high-quality filter capacitor(s), e.g. MLCCs, the inherent ESR zero may occur at a much higher frequency, as shown in Figure 4c.

As with the previous example, the actual gain and phase response is overlaid on the power modulator’s asymptotic gain response. One readily observes the more dramatic gain and phase transition at or near the power modulator’s resonant frequency, f_LC, versus the gentler response of the previous example. This is due to the filter components’ lower parasitic (DCR and ESR) and corresponding higher frequency of the inherent ESR zero. In this example, the desired crossover frequency occurs below the ESR zero frequency.

In this example, a compensator with an inherent midfrequency double-zero response is required to mitigate the effects of the filter’s double-pole phase lag. This is available with the Type III topology.

As demonstrated in Figure 4d, the Type III’s midfrequency double-zero gain (exhibiting a +20dB/dec slope, noting the compensator’s pole at the origin) is designed to compensate for the power modulator’s double-pole -40dB/decade attenuation at the desired crossover frequency, f_C0 (again, Gain_E/A + Gain_MOD = 0dB at f_C0) (see Figure 4d).

In the above example the power modulator’s inherent (midfrequency) -40dB/decade rolloff is mitigated by the midfrequency double zero’s +20dB/decade gain to extend the active regulation gain-bandwidth of the voltage regulator. As shown in Figure 4d, the net result is an approximate doubling in the controller’s gain bandwidth while providing greater than 55 degrees of phase margin (the difference between Gain_E/A and Gain_MOD respective phases at crossover, f_C0).

Design procedures for both Type II and Type III compensators are shown below.
Type II: Compensation when fCO > fZERO,ESR

When the fCO is greater than fESR, a Type II compensation network provides the necessary closed-loop compensated response. The Type II compensation network provides a midband compensating zero and a high-frequency pole (see Figures 5a and 5b).

RfCF provides the midband zero fMID,ZERO, and RFCCF provides the high-frequency pole, fHIGH,POLE. Use the following procedure to calculate the compensation network components.

Calculate the fESR and LC double pole, fLC:

\[ f_{ESR} = \frac{1}{2\pi \times ESR \times COUT} \]
\[ f_{LC} = \frac{1}{2\pi \sqrt{L \times COUT}} \]

where COUT is the regulator output capacitor and ESR is the series resistance of COUT. See the Output-Capacitor Selection section for more information on calculating COUT and ESR.

Set the compensator’s leading zero, fZ1, at or below the filter’s resonant double-pole frequency from:

\[ f_{Z1} \leq f_{LC} \]

Set the compensator’s high-frequency pole, fP1, at or below one-half the switching frequency, fSW:

\[ f_{P1} \leq \frac{f_{SW}}{2} \]

To maximize the compensator’s phase lead, set the desired crossover frequency, fCO, equal to the geometric mean of the compensator’s leading zero, fZ1, and high-frequency pole, fP1, as follows:

\[ f_{CO} = \sqrt{f_{Z1} \times f_{P1}} \]

Select the feedback resistor, RF, in the range of 3.3kΩ to 30kΩ.

Calculate the gain of the modulator (GainMOD)—comprised of the regulator’s pulse-width modulator, LC filter, feedback divider, and associated circuitry—at the desired crossover frequency, fCO, using the following equation:

\[ \text{GainMOD} = 4(V/V) \times \frac{ESR \ [m\Omega]}{(2\pi f_{CO}[kHz] \times L[\mu H]) \times \frac{V_{FB}[V]}{V_{OUT_+}[V]}} \]

where VFB is the 0.6V (typ) FB_ input-voltage set-point, L is the value of the regulator inductor, ESR is the series resistance of the output capacitor, and VOUT_+ is the desired output voltage.

The gain of the error amplifier (GainE/A) in the midband frequencies is:

\[ \text{GainE/A} = \frac{R_F \ [k\Omega]}{R_1 \ [k\Omega]} \]

The total loop gain is the product of the modulator gain and the error amplifier gain at fCO and should be set equal to 1 as follows:

\[ \text{GainMOD} \times \text{GainE/A} = 1 \]

So:

\[ 20 \times \log_{10} \left( \frac{R_F}{R_1} \right) + 20 \times \log_{10} \left( \frac{4 \times ESR \times V_{FB}}{2\pi f_{CO} \times L \times V_{OUT_+}} \right) = 0 \text{dB} \]

\[ \frac{R_F}{R_1} \times \frac{4 \times ESR \times V_{FB}}{2\pi f_{CO} \times L \times V_{OUT_+}} = 1 \]
Solving for $R_1$:

$$R_1 [\text{k}\Omega] = \frac{R_F[k\Omega] \times 4 \times ESR[m\Omega] \times V_{FB}[V]}{2 \pi \times f_{CO} [kHz] \times L[\mu H] \times V_{OUT_}[V]}$$

where $V_{FB}$ is the 0.6V (typ) $FB_-$ input-voltage set-point, $L$ is the value of the regulator inductor, $ESR$ is the series resistance of the output capacitor, and $V_{OUT_}$ is the desired output voltage.

1) $C_F$ is determined from the compensator’s leading zero, $f_{Z1}$, and $R_F$ as follows:

$$C_F[\mu F] = \frac{1}{2 \pi \times R_F[k\Omega] \times f_{Z1}[kHz]}$$

2) $C_{CF}$ is determined from the compensator’s high-frequency pole, $f_{P1}$, and $R_F$ as follows:

$$C_{CF}[\mu F] = \frac{1}{2 \pi \times R_F[k\Omega] \times f_{P1}[kHz]}$$

3) Calculate $R_2$ using the following equation:

$$R_2[k\Omega] = R_1[k\Omega] \times \frac{V_{FB}[V]}{V_{OUT_}[V] - V_{FB}[V]}$$

where $V_{FB} = 0.6V$ (typ) and $V_{OUT_}$ is the output voltage of the regulator.

**Type III: Compensation when $f_{CO} < f_{ESR}$**

As indicated above, the position of the output capacitor’s inherent ESR zero is critical in designing an appropriate compensation network. When low-ESR ceramic output capacitors (MLCCs) are used, the ESR zero frequency ($f_{ESR}$) is usually much higher than the desired crossover frequency ($f_{CO}$). In this case, a type III compensation network is recommended (see Figure 6a).

As shown in Figure 6b, the Type III compensation network introduces two zeros and three poles into the control loop. The error amplifier has a low-frequency pole at the origin, two zeros, and two higher frequency poles at the following frequencies:

$$f_{Z1} = \frac{1}{2 \pi \times R_F \times C_F}$$

$$f_{Z2} = \frac{1}{2 \pi \times C_F \times (R_1 + R_F)}$$

Two midband zeros ($f_{Z1}$ and $f_{Z2}$) are designed to compensate for the pair of complex poles introduced by the LC filter.

Figure 6a. Type III Compensation Network

Figure 6b. Type III Compensation Network Response

$f_{P1}$ introduces a pole at zero frequency (integrator) for nulling DC output voltage errors.

$$f_{P1} = \text{at the origin (0Hz)}$$

Depending on the location of the ESR zero ($f_{ESR}$), $f_{P2}$ can be used to cancel it, or to provide additional attenuation of the high-frequency output ripple.

$$f_{P2} = \frac{1}{2 \pi \times R_1 \times C_F}$$

$f_{P3}$ attenuates the high-frequency output ripple.

$$f_{P3} = \frac{1}{2 \pi \times R_F \times \left(C_F + C_{CF}\right)} = \frac{1}{2 \pi \times R_F \times C_F \times C_{CF}} \times \frac{C_{CF}}{C_F + C_{CF}}$$

Since $C_{CF} << C_F$ then:

$$f_{P3} = \frac{1}{2 \pi \times R_F \times C_{CF}}$$
The locations of the zeros and poles should be such that the phase margin peaks around $f_{CO}$.

Set the ratios of $f_{CO}$-to-$f_Z$ and $f_{P}$-to-$f_{CO}$ equal to one another, e.g., $f_{CO} = f_Z = 5$ is a good number to get approximately $60^\circ$ of phase margin at $f_{CO}$. Whichever technique, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

The following procedure is recommended:

1) Select a crossover frequency, $f_{CO}$, at or below one-tenth the switching frequency ($f_{SW}$):

$$f_{CO}[kHz] \leq \frac{f_{SW}[kHz]}{10}$$

2) Calculate the LC double-pole frequency, $f_{LC}$:

$$f_{LC}[MHz] = \frac{1}{2\pi \times \sqrt{L[\mu H] \times C_{OUT}[\mu F]}}$$

where $C_{OUT}$ is the output capacitor of the regulator.

3) Select the feedback resistor, $R_F$, in the range of $3.3k\Omega$ to $30k\Omega$.

4) Place the compensator’s first $f_Z = \frac{1}{2\pi \times R_F \times C_F}$ zero at or below the output filter’s double-pole, $f_{LC}$, as follows:

$$C_F[\mu F] = \frac{1}{2\pi \times R_F[k\Omega] \times 0.5 \times f_{LC}[kHz]}$$

5) The gain of the modulator (Gain$_{MOD}$)—comprised of the regulator’s pulse-width modulator, LC filter, feedback divider, and associated circuitry—at the crossover frequency is:

$$\text{Gain}_{MOD} = 4 \times \frac{1}{(2\pi \times f_{CO}[MHz])^2 \times L[\mu H] \times C_{OUT}[\mu F]}$$

The gain of the error amplifier (Gain$_{E/A}$) in midband frequencies is:

$$\text{Gain}_{E/A} = 2\pi \times f_{CO}[kHz] \times C_I[\mu F] \times R_F[k\Omega]$$

The total loop gain is the product of the modulator gain and the error amplifier gain at $f_{CO}$ should be equal to 1, as follows:

$$\text{Gain}_{MOD} \times \text{Gain}_{E/A} = 1$$

So:

$$4 \times \frac{1}{(2\pi \times f_{CO}[kHz])^2 \times C_{OUT}[\mu F] \times L[\mu H] \times 2\pi \times f_{CO}[kHz] \times C_I[\mu F] \times R_F[k\Omega]} = 1$$

Solving for $C_I$:

$$C_I[\mu F] = \frac{(2\pi \times f_{CO}[kHz] \times L[\mu H] \times C_{OUT}[\mu F])}{4 \times R_F[k\Omega]}$$

6) For those situations where $f_{LC} < f_{CO} < f_{ESR} < f_{SW}/2$, as with low-ESR tantalum capacitors, the compensator’s second pole ($f_{P2}$) should be used to cancel $f_{ESR}$. This provides additional phase margin. On the system Bode plot, the loop gain maintains its +20dB/decade slope up to $1/2$ of the switching frequency versus flattening out soon after the 0dB crossover. Then set:

$$f_{P2} = f_{ESR}$$

If a ceramic capacitor is used, then the capacitor ESR zero, $f_{ESR}$, is likely to be located even above one-half of the switching frequency, that is $f_{LC} < f_{CO} < f_{SW}/2 < f_{ESR}$. In this case, the frequency of the second pole ($f_{P2}$) should be placed high enough not to significantly erode the phase margin at the crossover frequency. For example, $f_{P2}$ can be set at 5 x $f_{CO}$, so that its contribution to phase loss at the crossover frequency $f_{CO}$ is only about $11^\circ$:

$$f_{P2} = 5 \times f_{CO}$$

Once $f_{P2}$ is known, calculate $R_I$:

$$R_I[k\Omega] = \frac{1}{2\pi \times f_{P2}[kHz] \times C_I[\mu F]}$$

7) Place the second zero ($f_{Z2}$) at 0.2 x $f_{CO}$ or at $f_{LC}$, whichever is lower, and calculate $R_1$ using the following equation:

$$R_1[k\Omega] = \frac{1}{2\pi \times f_{Z2}[kHz] \times C_I[\mu F]}$$

8) Place the third pole ($f_{P3}$) at 1/2 the switching frequency and calculate $C_{CF}$ from:

$$C_{CF}[\mu F] = \frac{1}{(2\pi \times 0.5 \times f_{SW}[MHz] \times R_F[k\Omega])}$$

9) Calculate $R_2$ as:

$$R_2[k\Omega] = R_1[k\Omega] \times \frac{V_{FB}[V]}{V_{OUT}[V]-V_{FB}[V]}$$

where $V_{FB} = 0.6V$ (typ).
Applications Information

PCB Layout Guidelines
Careful PCB layout is critical to achieve clean and stable operation. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close as possible to the IC pins.
2) Keep SGND and PGND isolated and connect them at one single point close to the negative terminal of the input filter capacitor.
3) Route high-speed switching nodes away from sensitive analog areas (FB_, COMP_, and EN_).
4) Distribute the power components evenly across the board for proper heat dissipation.
5) Ensure timing resistor and all feedback connections are short and direct. Place feedback resistors as close as possible to the IC.
6) Place the bank of the output capacitors close to the load.
7) Connect the MAX15021 exposed pad to a large copper plane to maximize its power dissipation capability. Connect the exposed pad to SGND plane. Do not connect the exposed pad to the SGND pin directly underneath the IC.
8) Use 2oz. copper to keep trace inductance and resistance to a minimum. Thin copper PCBs can compromise efficiency since high currents are involved in the application. Also thicker copper conducts heat more effectively, thereby reducing thermal impedance.
9) A reference PCB layout included in the MAX15021 Evaluation Kit is also provided to further aid layout.
Typical Operating Circuits

Figure 7. MAX15021 Double Buck with Tracking
Typical Operating Circuits (continued)

Figure 8. MAX15021 Double Buck with Sequencing
MAX15021 Dual, 4A/2A, 4MHz, Step-Down DC-DC Regulator with Tracking/Sequencing Capability

Chip Information
PROCESS: BiCMOS

Package Information
For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

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