The MAX15018A/MAX15018B/MAX15019A/MAX15019B high-frequency, 125V half-bridge, n-channel MOSFET drivers drive high- and low-side MOSFETs in high-voltage applications. These drivers are independently controlled, and their 35ns (typ) propagation delay, from input to output, are matched to within 2ns (typ). The high-voltage operation with very low and matched propagation delay between drivers, and high source-/sink-current capabilities in a thermally enhanced package make these devices suitable for high-power, high-frequency telecom power converters. The 125V maximum input voltage provides plenty of margin over the 100V input transient requirement of telecom standards. A reliable on-chip bootstrap diode connected between VDD and BST eliminates the need for an external discrete diode.

The MAX15018A/MAX15019A both offer noninverting drivers. The MAX15018B/MAX15019B offer a noninverting high-side driver and an inverting low-side driver (see the Selector Guide.) The MAX15018_ feature CMOS (VDD/2) logic inputs. The MAX15019_ feature TTL-logic inputs. The drivers are available in the industry-standard 8-pin SO footprint and pin configuration with a thermally enhanced 8-pin SO package. All devices operate over the -40°C to +125°C automotive temperature range.

### Applications
- Telecom Power Supplies
- Synchronous Buck DC-to-DC Converters
- Half-Bridge, Full-Bridge, and Two-Switch Forward Converters
- Power-Supply Modules
- Motor Control

### Features
- HIP2100IB/HIP2101IB Pin Compatible (MAX15018A/MAX15019A)
- Up to 125V VIN Operation
- 8V to 12.6V VDD Input Supply Range
- 3A Peak Source and Sink Current
- 35ns Propagation Delay
- Guaranteed 8ns or Less Propagation Delay Matching Between High- and Low-Side Drivers
- Both Noninverting/Noninverting and Noninverting/Inverting Logic-Input Versions Available
- Up to 15V Logic Inputs, Independent of VDD Supply Voltage
- Low 8pF Input Capacitance
- Available in CMOS (VDD/2) or TTL Logic-Level Inputs with Hysteresis
- Available in a Space-Saving, Thermally Enhanced 8-Pin SO-EP Package

### Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>TEMP RANGE</th>
<th>PIN-PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX15018A</td>
<td>-40°C to +125°C</td>
<td>8 SO-EP*</td>
</tr>
<tr>
<td>MAX15018B</td>
<td>-40°C to +125°C</td>
<td>8 SO-EP*</td>
</tr>
<tr>
<td>MAX15019A</td>
<td>-40°C to +125°C</td>
<td>8 SO-EP*</td>
</tr>
<tr>
<td>MAX15019B</td>
<td>-40°C to +125°C</td>
<td>8 SO-EP*</td>
</tr>
</tbody>
</table>

+ Denotes a lead-free/RoHS-compliant package.
* EP = Exposed pad. Internally connected to GND.

### Typical Operating Circuit
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

- V_{DD} to GND: -0.3V to +15V
- IN\_H, IN\_L to GND: -0.3V to +15V
- DL to GND: -0.3V to (V_{DD} + 0.3V)
- DH to HS: -0.3V to (V_{DD} + 0.3V)
- BST to HS: -0.3V to +15V
- HS to GND (repetitive transient): -5V to +130V
- HS dv/dt to GND: 50V/\mu s

Continuous Power Dissipation (T_{A} = +70°C)

Single and Multilayer Board

Continuous Power Dissipation (T_{A} = +70°C)

8-Pin SO-EP (derate 23.8mW/°C above +70°C)

θ_{JC} = 6°C/W

Operating Temperature: -40°C to +125°C

Maximum Junction Temperature: +150°C

Storage Temperature Range: -65°C to +150°C

Lead Temperature (soldering, 10s): +300°C

*As per JEDEC Standard 51 (Single-Layer Board).

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{BST} = 8V to 12.6V, V_{HS} = V_{GND} = 0V, T_{A} = T_{J} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = V_{BST} = 12V and T_{A} = +25°C.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage</td>
<td>V_{DD}</td>
<td></td>
<td>8.0</td>
<td>12.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{DD} Quiescent Supply Current</td>
<td>I_{DDQ}</td>
<td>IN_H and IN_L are unconnected (no switching)</td>
<td>MAX15018A/MAX15018B</td>
<td>65</td>
<td>130</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B</td>
<td>95</td>
<td>190</td>
<td>µA</td>
</tr>
<tr>
<td>V_{DD} Operating Supply Current</td>
<td>I_{DDO}</td>
<td>f_{SW} = 500kHz, V_{DD} = 12V, no capacitive load</td>
<td>2.75</td>
<td>3.75</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>BST Quiescent Supply Current</td>
<td>I_{BSTQ}</td>
<td>IN_H and IN_L are unconnected (no switching)</td>
<td>95</td>
<td>190</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>BST Operating Supply Current</td>
<td>I_{BSTO}</td>
<td>f_{SW} = 500kHz, V_{BST} - V_{HS} = 12V, no capacitive load</td>
<td>2.75</td>
<td>3.75</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>UVLO (V_{DD} to GND)</td>
<td>V_{DDUVLO}</td>
<td>V_{DD} rising</td>
<td>6.5</td>
<td>7.3</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>UVLO (BST to HS)</td>
<td>V_{BSTUVLO}</td>
<td>V_{BST} rising</td>
<td>6.2</td>
<td>6.9</td>
<td>7.6</td>
<td>V</td>
</tr>
<tr>
<td>UVLO Hysteresis</td>
<td></td>
<td></td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

LOGIC INPUT

| Input-Logic High | V_{IH} | MAX15018A/MAX15018B (CMOS) | 0.67 x V_{DD} |
| | | MAX15019A/MAX15019B (TTL) | 2 |
| Input-Logic Low | V_{IL} | MAX15018A/MAX15018B (CMOS) | 0.33 x V_{DD} |
| | | MAX15019A/MAX15019B (TTL) | 0.8 |
| Logic-Input Hysteresis | V_{HYS} | MAX15018A/MAX15018B (CMOS) | 1.65 |
| | | MAX15019A/MAX15019B (TTL) | 0.4 |
### ELECTRICAL CHARACTERISTICS (continued)

(VDD = VBST = 8V to 12.6V, VHS = VGND = 0V, TA = Tj = -40°C to +125°C, unless otherwise noted. Typical values are at VDD = VBST = 12V and TA = +25°C.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic-Input Current</td>
<td>IN_</td>
<td>IN_H = IN_L = GND (MAX15018A/MAX15019A)</td>
<td>-1</td>
<td>+1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IN_H = GND, IN_L = VDD (MAX15018B/MAX15019B)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>RIN_</td>
<td>IN_L to GND (MAX15018A/MAX15019A)</td>
<td>5001</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IN_L to VDD (MAX15018B/MAX15019B)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IN_H to GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Cin_</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

#### HIGH-SIDE GATE DRIVER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS Maximum Voltage</td>
<td>VHS_MAX</td>
<td></td>
<td>125</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>BST Maximum Voltage</td>
<td>VBST_MAX</td>
<td></td>
<td>140</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Driver Output Resistance</td>
<td>RON_HP</td>
<td>(VBST - VHS) = 12V, IDH = 100mA (sourcing)</td>
<td>1.75</td>
<td>2.4</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>RON_HN</td>
<td>(VBST - VHS) = 12V, IDH = 100mA (sinking)</td>
<td>1.1</td>
<td>1.75</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Power-Off Pulldown Clamp</td>
<td></td>
<td>Voltage</td>
<td>0.88</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>IPK_HP</td>
<td>VDH = 0V</td>
<td>3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>IPK_HN</td>
<td>VDH = 12V</td>
<td>3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

#### LOW-SIDE GATE DRIVER

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver Output Resistance</td>
<td>RON_LP</td>
<td>VDD = 12V, IDL = 100mA (sourcing)</td>
<td>1.75</td>
<td>2.4</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>RON_LN</td>
<td>VDD = 12V, IDL = 100mA (sinking)</td>
<td>1.1</td>
<td>1.75</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Power-Off Pulldown Clamp</td>
<td></td>
<td>Voltage</td>
<td>0.88</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Peak Output Current</td>
<td>IPK_LP</td>
<td>VDL = 0V</td>
<td>3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>IPK_LN</td>
<td>VDL = 12V</td>
<td>3</td>
<td></td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

#### INTERNAL BOOTSTRAP DIODE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Voltage Drop</td>
<td>VF</td>
<td>IBST = 100mA</td>
<td>0.9</td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Turn-On and Turn-Off Time</td>
<td>TRR</td>
<td>IBST = 100mA</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
# 125V/3A, High-Speed, Half-Bridge MOSFET Drivers

## ELECTRICAL CHARACTERISTICS (continued)

(VDD = VBST = 8V to 12.6V, VHS = VGND = 0V, TA = TJ = -40°C to +125°C, unless otherwise noted. Typical values are at VDD = VBST = 12V and TA = +25°C.) (Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWITCHING CHARACTERISTICS FOR HIGH- AND LOW-SIDE DRIVERS (VDD = VBST = +12V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>tR</td>
<td>No CL</td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 1000pF</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 5000pF</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 10,000pF</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>tf</td>
<td>No CL</td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 1000pF</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 5000pF</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CL = 10,000pF</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-On Propagation Delay Time</td>
<td>tD_ON</td>
<td>Figure 1, CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>33</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>36</td>
<td>66</td>
<td></td>
</tr>
<tr>
<td>Turn-Off Propagation Delay Time</td>
<td>tD_OFF</td>
<td>Figure 1, CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>30</td>
<td>55</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>36</td>
<td>66</td>
<td></td>
</tr>
<tr>
<td>Delay Matching Between High-Side Turn-On to Low-Side Turn-On</td>
<td>tMATCH1</td>
<td>CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>1</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>1</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>Delay Matching Between High-Side Turn-Off to Low-Side Turn-Off</td>
<td>tMATCH2</td>
<td>CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>1</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>1</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>Delay Matching Between High-Side Turn-Off to Low-Side Turn-On</td>
<td>tMATCH3</td>
<td>CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>2</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>1</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>Delay Matching Between High-Side Turn-On to Low-Side Turn-Off</td>
<td>tMATCH4</td>
<td>CL = 1000pF (Note 2)</td>
<td>MAX15018A/MAX15018B (CMOS)</td>
<td>2</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MAX15019A/MAX15019B (TTL)</td>
<td>1</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>Minimum Input Pulse Width for Output Change</td>
<td>tPW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** All devices are 100% production tested at TA = TJ = +125°C. Limits over temperature are guaranteed by design and characterization.

**Note 2:** Guaranteed by design, not production tested.
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

**Typical Operating Characteristics**

(TA = +25°C, unless otherwise noted.)

- **VDD AND BST UNDERVOLTAGE LOCKOUT** vs. TEMPERATURE
- **VDD AND BST UNDERVOLTAGE LOCKOUT HYSTERESIS vs. TEMPERATURE**
- **UNDERSWITCH RESPONSE**
  - (VDD RISING)
  - (VDD FALLING)
- **INTERNAL BOOTSTRAP DIODE I-V CHARACTERISTICS**
- **MAX15018A IDD AND IBST CURRENT** vs. VDD (250kHz SWITCHING)
- **MAX15018A BST QUIESCENT CURRENT** vs. VBST (NO SWITCHING)
- **MAX15018A IDD AND IBST** vs. SWITCHING FREQUENCY
**125V/3A, High-Speed, Half-Bridge MOSFET Drivers**

(T<sub>A</sub> = +25°C, unless otherwise noted.)

**Typical Operating Characteristics (continued)**

**DH OR DL OUTPUT LOW VOLTAGE vs. TEMPERATURE**

**DH AND DL OUTPUT HIGH VOLTAGE vs. TEMPERATURE**

**PEAK OUTPUT CURRENT vs. OUTPUT VOLTAGE**

**DH OR DL OUTPUT RISE TIME vs. TEMPERATURE**

**DH OR DL OUTPUT FALL TIME vs. TEMPERATURE**

**DH OR DL RISING PROPAGATION DELAY vs. TEMPERATURE**

**DH OR DL FALLING PROPAGATION DELAY vs. TEMPERATURE**

**DELAY MATCHING (DH AND DL RISING)**
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

Typical Operating Characteristics (continued)

(TA = +25°C, unless otherwise noted.)

### Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Input Supply Voltage. Valid supply voltage ranges from 8V to 12.6V. Bypass VDD to GND with a parallel combination of 0.1µF and 1µF ceramic capacitors as close to the IC as possible.</td>
</tr>
<tr>
<td>2</td>
<td>BST</td>
<td>Boost Flying Capacitor Connection. Connect a 0.22µF ceramic capacitor from BST to HS as close to the IC as possible for the high-side MOSFET driver supply.</td>
</tr>
<tr>
<td>3</td>
<td>DH</td>
<td>High-Side Gate Driver Output. Driver output for the high-side MOSFET gate.</td>
</tr>
<tr>
<td>4</td>
<td>HS</td>
<td>Source Connection for High-Side MOSFET. Also serves as the return for the high-side driver.</td>
</tr>
<tr>
<td>5</td>
<td>IN_H</td>
<td>High-Side Noninverting Logic Input</td>
</tr>
<tr>
<td>6</td>
<td>IN_L</td>
<td>Low-Side Noninverting (MAX15018A/MAX15019A) or Low-Side Inverting (MAX15018B/MAX15019B) Input</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Ground. Use GND as a return path to the DL driver output and the IN_H, IN_L inputs. Must be connected to ground.</td>
</tr>
<tr>
<td>8</td>
<td>DL</td>
<td>Low-Side Gate Driver Output. Driver output for the low-side MOSFET gate.</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>Exposed Pad. Internally connected to GND. Externally connect the exposed pad to a large ground plane to aid in heat dissipation. Grounding EP does not substitute the requirement to connect GND to ground.</td>
</tr>
</tbody>
</table>
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

Detailed Description

The MAX15018A/MAX15018B/MAX15019A/MAX15019B half-bridge, n-channel MOSFET drivers control high- and low-side MOSFETs in high-voltage, high peak-current applications and offer a high 125V voltage range that allows ample margin above the 100V transient specification of telecom standards. These drivers operate with an IC supply voltage of 8V to 12.6V, and consume only 2.75mA of supply current during typical switching operations. The MAX15018_/MAX15019_ provide 3A (typ) sink/source peak current per output and are capable of operating with large capacitive loads and with switching frequencies near 1MHz.

These drivers are intended to be used to drive the high-side MOSFET without requiring an isolation device such as an optocoupler or a drive transformer. The high-side driver is controlled by a TTL/CMOS logic signal referenced to ground and is powered by a bootstrap circuit formed by an integrated diode and an external capacitor. Undervoltage lockout (UVLO) protection is provided for both the high- and low-side driver supplies (BST and VDD) and includes a UVLO hysteresis of 0.5V (typ).

The drivers are independently controlled and feature exceptionally fast switching times, very short propagation delays (35ns typ), and matched propagation delay-times (2ns typ) between drivers, making them ideally suited for high-frequency applications. Internal logic circuitry prevents shoot-through during output state changes and minimizes package power dissipation.

These devices are available with CMOS (VDD/2) or TTL logic-level inputs. The MAX15018A/MAX15018B accept CMOS input logic levels, while the MAX15019A/ MAX15019B accept TTL input logic levels. For both versions, the logic inputs are protected against voltage spikes up to +15V, regardless of VDD. See the Driver Logic Inputs (IN_H, IN_L) section.

The MAX15018_/MAX15019_ are available with both high-side and low-side noninverting logic inputs or with noninverting high-side and inverting low-side logic inputs. See the Functional Diagrams and Selector Guide. The MAX15018A and MAX15019A are pin-for-pin replacements for the HIP2100IB and HIP2101IB, respectively.

The MAX15018_/MAX15019_ are available in a space-saving, high-power, 8-pin SO-EP package that can dissipate up to 1.95W at +70°C. All devices operate over the -40°C to +125°C automotive temperature range.

Undervoltage Lockout

Both the high- and low-side drivers feature separate UVLO protection that monitors each driver’s input supply voltage (BST and VDD). The low-side driver UVLO threshold (VDD_UVLO) is referenced to GND and pulls both driver outputs low when VDD falls below 7.3V (typ). The high-side driver UVLO threshold (VBST_UVLO) is referenced to HS, and only pulls DH low when VBST falls below 6.9V (typ) with respect to HS. After the IC is first energized, and once VDD rises above its UVLO threshold, DL starts switching and either follows the IN_L logic input (MAX15018A/MAX15019A) or is inverted with reference to the IN_L logic input (MAX15018B/ MAX15019B). At this time, the bootstrap capacitor is not charged, and DH does not switch since the BST-to-HS voltage is below VBST_UVLO. Within a short time following engagement of low-side switching, CBST charges through VDD and causes VBST to exceed VBST_UVLO. DH then starts switching and follows IN_H. For synchronous buck and half-bridge converter topologies, the bootstrap capacitor can charge up in one cycle. Normal operation then begins in a few microseconds after the BST-to-HS voltage exceeds VBST_UVLO. In the two-switch forward topology, CBST takes more time (a few hundred microseconds) to charge and increase its voltage above VBST_UVLO. The typical hysteresis for both UVLO thresholds is 0.5V. The bootstrap capacitor value should be selected carefully to avoid oscillations during turn-on and turn-off at the DH output. Choose a capacitor value 20 times greater than the total gate capacitance of the MOSFET. Use a low ESR-type X7R dielectric ceramic capacitor at BST (typically a 0.1µF ceramic is adequate) and a parallel combination of 1µF and 0.1µF ceramic capacitors from VDD to GND. The high-side MOSFET’s continuous on-time is limited due to the charge loss from the high-side driver’s quiescent current. The maximum on-time is dependent on the size of CBST, IBST (190µA, max), and VBST_UVLO.
Output Driver

The MAX15018_/MAX15019_ drivers contain low on-resistance p-channel and n-channel devices in a totem pole configuration for the driver output stage. This allows for rapid turn-on and turn-off of high gate-charge \( (Q_g) \) external switching MOSFETs.

The drivers exhibit low drain-to-source resistance \( (R_{DS\_ON}) \), which decreases for higher values of \( V_{DD} \) and for lower operating temperatures. Lower \( R_{DS\_ON} \) means higher source and sink currents from the IC, and results in faster switching speeds, since the external MOSFET gate capacitance will charge and discharge at a quicker rate. The peak source and sink current provided by the drivers is typically 3A.

Propagation delay from the logic inputs to the driver outputs is matched to within 8ns (max) between the low-side and high-side drivers. Turn-on and turn-off propagation delays are typically 35ns and 36ns. See Figure 1. The internal drivers also contain break-before-make logic to eliminate shoot-through conditions that would cause unnecessarily high operating supply currents, efficiency reduction, and voltage spikes at \( V_{DD} \).

Voltage at DL is approximately equal to \( V_{DD} \) when in a high state, and zero when in a low state. Voltage from DH to HS is approximately equal to \( V_{DD} \) minus the diode drop of the integrated bootstrap diode when in a high state, and zero when in a low state. The high-side MOSFET's continuous on-time is limited due to the charge loss from the high-side driver's quiescent current. The maximum on-time is dependent on the size of the bootstrap capacitor \( (C_{BST}) \), \( I_{BST} \) (190µA max), and \( V_{BST\_UVLO} \).

Integrated Bootstrap Diode

An integrated diode between \( V_{DD} \) and BST is used in conjunction with an external bootstrap capacitor \( (C_{BST}) \) to provide the voltage required to turn on the high-side MOSFET (see the Typical Operating Circuit). The internal diode charges the bootstrap capacitor from \( V_{DD} \) when the low-side switch is on, and isolates \( V_{DD} \) when HS is pulled high when the high-side driver turns on. The internal bootstrap diode has a typical forward voltage drop of 0.9V and has a 40ns (typ) turn-off/on time. The turn-off time (reverse recovery time) depends on the reverse-recovery current and can be as low as 10ns. If a lower diode voltage-drop between \( V_{DD} \) and BST is needed, connect an external Schottky diode between \( V_{DD} \) and BST.

Figure 1. Timing Characteristics of Logic Inputs (MAX15018A/MAX15019A)
**Bootstrap Capacitor**

The bootstrap capacitor is used to ensure adequate charge is available to switch the high-side MOSFET. This capacitor is charged from VDD through the internal bootstrap diode when the low-side MOSFET is on. The bootstrap capacitor value should be selected carefully to avoid oscillations during turn-on and turn-off at the DH output. Choose a capacitor value approximately 20 times greater than the total gate capacitance of the MOSFET being switched. Use a low-ESR, X7R-type dielectric ceramic capacitor (typically a 0.1µF ceramic is adequate). The high-side MOSFET’s continuous on-time is limited due to the charge loss from the high-side driver’s quiescent current. The maximum on-time is dependent on the size of CBST, IBST (190µA max), and VBST_UVLO. Note that the bootstrap capacitor requires time to charge up to VDD, according to the time constant of the charging loop through the lower MOSFET (see the Typical Operating Circuit). Ensure that the lower MOSFET is on for at least the minimum time required to charge CBST.

**Driver Logic Inputs (IN_H, IN_L)**

The MAX15018_ are CMOS (VDD/2) logic-input drivers, and the MAX15019_ are TTL-compatible logic-input drivers. The required logic-input levels are independent of VDD. For example, the IC can be powered by a 10V supply while the logic inputs are provided from 12V CMOS logic. Additionally, the logic inputs are protected against voltage spikes up to 15V, regardless of VDD voltage. The TTL and CMOS logic inputs have 400mV and 1.6V hysteresis, respectively, to avoid double pulsing during signal transition. The logic inputs are high-impedance pins (500kΩ typ) and should not be left unconnected to ensure the input logic state is at a known level. With the logic inputs unconnected, the DH and DL outputs pull low as VDD rises up above the UVLO threshold. The PWM output from the controller must assume a proper state while powering up the device.

**Applications Information**

**Supply Bypassing and Grounding**

Careful attention is required when choosing the bypassing and grounding scheme of the MAX15018_/MAX15019_. Peak supply and output currents may exceed 6A when both drivers are simultaneously driving large external capacitive loads in phase. Supply drops and ground shifts create forms of negative feedback for inverting topologies and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the VDD, DH, DL, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX15018_/MAX15019_ with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel from VDD to GND as close as possible to the device to bypass the input supply. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFETs as close as possible to the MAX15018_/MAX15019_ to reduce trace length and further minimize board inductance and AC path resistance.

**Power Dissipation**

Power dissipation in the MAX15018_/MAX15019_ is primarily due to power loss in the internal boost diode and the internal nMOS and pMOS FETS. For capacitive loads, the total power dissipation for the device is:

\[ P_D = (C_L \times VDD^2 \times fSW) + (I_{VDDO} + I_{BSTO}) \times VDD \]

where C_L is the combined capacitive load at DH and DL, VDD is the supply voltage, and fSW is the switching frequency of the IC. P_D includes the power dissipated in the internal bootstrap diode (PDIODE). The internal power dissipation reduces by PDIODE, if an external bootstrap Schottky diode is used. The power dissipation in the internal boost diode (when driving a capacitive load) will be the charge through the diode per switching period multiplied by the maximum diode forward voltage drop (VF = 1V) as given in the following equation.

\[ P_{DIODE} = C_{DH} \times (VDD - 1) \times fSW \times VF \]

where CDH is the capacitive load at DH, VDD is the supply voltage, fSW is the switching frequency of the converter, VF is the maximum diode forward voltage drop. The total power dissipation when using the internal boost diode will be PD and, when using an external Schottky diode, will be PD - PDIODE. The total power dissipated in the device must be kept below the maximum of 1.95W for the 8-pin SO with exposed pad at TA = +70°C ambient.
**125V/3A, High-Speed, Half-Bridge MOSFET Drivers**

**Layout Information**
The MAX15018/MAX15019 drivers source and sink large currents to create very fast rise and fall edges at the gates of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PCB layout guidelines when designing with the MAX15018/MAX15019:

- It is important that the VDD voltage (with respect to ground) or BST voltage (with respect to HS) does not exceed 15V. Voltage spikes higher than 15V from VDD to GND or from BST to HS can damage the device. Place one or more low-ESL 0.1µF decoupling ceramic capacitors from VDD to GND and from BST to HS as close as possible to the part. The ceramic decoupling capacitors should be at least 20 times the gate capacitance being driven.
- There are two AC current loops formed between the IC and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from the MOSFET driver output (DL or DH) to the MOSFET gate, to the MOSFET source, and to the return terminal of the MOSFET driver (either GND or HS). When the gate of the MOSFET is being pulled high, the active current loop is from the MOSFET driver output, (DL or DH), to the MOSFET gate, to the MOSFET source, to the return terminal of the drivers decoupling capacitor, to the positive terminal of the decoupling capacitor, and to the supply connection of the MOSFET driver. The decoupling capacitor will be either CBST for the high-side MOSFET or the VDD decoupling capacitor for the low-side MOSFET. Care must be taken to minimize the physical distance and the impedance of these AC current paths.
- Solder the exposed pad of the 8-pin SO-EP package to a large copper plane to achieve the rated power dissipation.

**Typical Application Circuits**

![Typical Application Circuits](image)

*Figure 2. Half-Bridge Converter Application with Secondary-Side Synchronous Rectification*
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

Typical Application Circuits (continued)

Figure 3. Two-Switch Forward Application
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

Functional Diagrams

Selector Guide

<table>
<thead>
<tr>
<th>PART</th>
<th>HIGH-SIDE DRIVER</th>
<th>LOW-SIDE DRIVER</th>
<th>LOGIC LEVEL</th>
<th>PIN COMPATIBLE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX15018AASA+</td>
<td>Noninverting</td>
<td>Noninverting</td>
<td>CMOS (V_{DD}/2)</td>
<td>HIP 2100IB</td>
</tr>
<tr>
<td>MAX15018BASA+</td>
<td>Noninverting</td>
<td>Inverting</td>
<td>CMOS (V_{DD}/2)</td>
<td>—</td>
</tr>
<tr>
<td>MAX15019AASA+</td>
<td>Noninverting</td>
<td>Noninverting</td>
<td>TTL</td>
<td>HIP 2101IB</td>
</tr>
<tr>
<td>MAX15019BASA+</td>
<td>Noninverting</td>
<td>Inverting</td>
<td>TTL</td>
<td>—</td>
</tr>
</tbody>
</table>

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

<table>
<thead>
<tr>
<th>PACKAGE TYPE</th>
<th>PACKAGE CODE</th>
<th>DOCUMENT NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 SO</td>
<td>S8E-14</td>
<td>21-0111</td>
</tr>
</tbody>
</table>
125V/3A, High-Speed, Half-Bridge MOSFET Drivers

Revision History

<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5/08</td>
<td>Initial release</td>
<td>—</td>
</tr>
<tr>
<td>1</td>
<td>9/08</td>
<td>Removed future product asterisk for the MAX15018B.</td>
<td>1</td>
</tr>
</tbody>
</table>

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.