MAX14890E

Incremental Encoder Interface for RS-422, HTL, and TTL with Digital Inputs

General Description

The MAX14890E incremental encoder receiver contains four differential receivers and two single-ended receivers.

The differential receivers can be operated in RS-422 or differential high-threshold logic (HTL) modes and are optionally configurable for single-ended TTL/HTL operation. The MAX14890E features a wide common mode input range of -20V to +20V in RS-422 mode.

The auxiliary IEC 61131-2 Type-1/Type-3 digital inputs are designed for operation with switches or proximity sensors and can be individually configured for TTL operation.

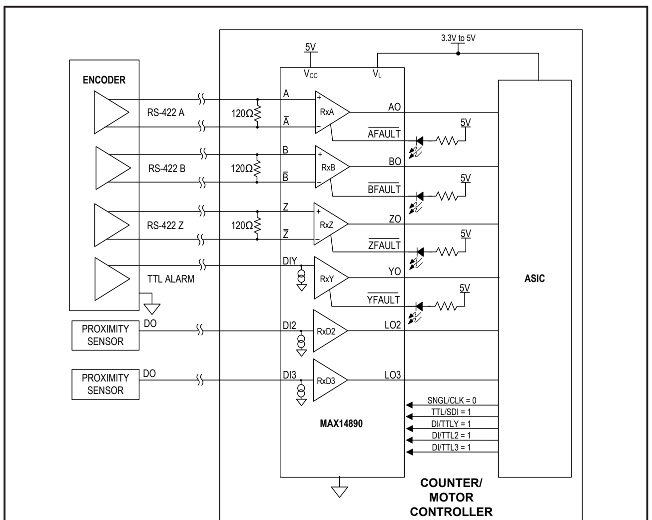
All receiver input signals are fault protected to voltage shorts in the ±40V range. Per channel fault detection provides warning of irregular conditions such as small differential signals, shorts, opens, overvoltages, and undervoltages.

The MAX14890E features a pin-selectable SPI or parallel-logic interface. SPI control provides detailed diagnostics and individual configurations for receivers.

The MAX14890E is available in a 32-pin TQFN-EP (5mm x 5mm) and operates over the -40°C to +125°C temperature range.

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



ENCODER CIRCUIT WITH RS-422 SIGNALS AND TTL ALARM SIGNAL

Benefits and Features

- High Flexibility Supports All Encoder Types
  - Selectable RS-422/HTL/TTL/DI Receivers
  - RS-422 Switching Rates Up to 35Mbps
  - TTL Switching Rates Up to 5MHz
  - HTL Switching Rates Up to 400kHz
  - SPI or Pin-Controlled Operation
  - SPI Interface Allows Per-Receiver Configuration
  - 1.62V to 5.5V Logic Interface
- Integrated Fault Detection Reduces Down-Time
  - Open-Wire and Short-Circuit Detection
  - Overvoltage and Undervoltage Fault Detection
- Integrated Protection Ensures Robust Communication
  - ±40V Fault Protection Range
  - ±20V RS-422 Common Mode Range
  - DI Glitch Filters
  - ±25kV HBM ESD
  - ±7kV Air-Gap per IEC 61000-4-2 ESD
  - ±10kV Contact per IEC 61000-4-2 ESD
  - -40°C to +125°C Operating Temperature Range

Applications

- Encoder Interfaces
- Motor Controllers
- Pulse Counters
- Servo Control Commutation

Input Receiver Modes

MODE	RxA	RxB	RxZ	RxY	RxDI2	RxDI3
RS-422	√	√	√	√		
D-HTL	√	√	√			
SE-HTL	√	√	√			
TTL	√	√	√	√	√	√
DI			√	√	√	√

Absolute Maximum Ratings

(All voltages referenced to GND)
V_{CC} .... -0.3V to +6V
V_L .... -0.3V to (V_{CC} + 0.3V)
AO, BO, ZO, YO, LO, LO2, LO3 .... -0.3V to (V_L + 0.3V)
_FAULT, D2FAULT/IRQ .... -0.3V to +6V
D3FAULT/ SDO (SPI is High) .... -0.3V to (V_L + 0.3V)
D3FAULT/SDO (SPI is Low) .... -0.3V to +6V
TTL/SDI, SNGL/SCLK, HITH/CS, DI/TTLY,
DI/TTL2, DI/TTL3, SPI .... -0.3V to +6V
A, A, B, B, Z, Z, DIY, Y, DI2, DI3 .... -40V to +40V

Short-Circuit Duration (_O, _FAULT, LO2,
D2FAULT/IRQ, LO3, D3FAULT/SDO to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Thin QFN (derate 19mW/°C above +70°C) 1520mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10s) .... +300°C
Soldering Temperature (Reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

Package Code	T3255+6
Outline Number	**21-0140**
Land Pattern Number	**90-0603**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{CC}		4.5		5.5	V
Supply Current	I_{CC}	Outputs not switching, no load		9	14	mA
Logic Supply Voltage	V_L		1.62		5.5	V
RS-422 RECEIVERS (RxA, RxB, RxZ, RxY)						
Differential Threshold Voltage	V_{TH}	-20V ≤ V_{CM} ≤ +20V	-200		+200	mV
Differential Input Hysteresis	ΔV_{TH}	-20V ≤ V_{CM} ≤ +20V		230		mV
Single-Ended Input Current	I_{IN}	V_{CC} = 0V or 5V, V_{IN} = +10V		+100	+160	µA
		V_{CC} = 0V or 5V, V_{IN} = -10V	-270	-170		
Low Differential Voltage Fault Threshold	V_{TH_DFP}	-20V ≤ V_{CM} ≤ +20V, positive	+270		+460	mV
	V_{TH_DFN}	-20V ≤ V_{CM} ≤ +20V, negative	-460		-270	
Single-Ended Input Fault Threshold	V_{TH_SELP}	Positive	+15		+18	V
	V_{TH_SELN}	Negative	-18		-15	
DIFFERENTIAL HTL RECEIVERS (RxA, RxB, RxZ)						
Differential Threshold Voltage	V_{TH}	0V ≤ V_{CM} ≤ +25V	-900		+900	mV
Differential Input Hysteresis	ΔV_{TH}	0V ≤ V_{CM} ≤ +25V		1		V
Single-Ended Input Current	I_{IN}	V_{TH} = +24V		+280	+460	µA
		V_{TH} = -10V	-270	-170		
Low Differential Voltage Fault Threshold	V_{TH_DFP}	0V ≤ V_{CM} ≤ +24V, Positive	+1.2		+2.0	V
	V_{TH_DFN}	0V ≤ V_{CM} ≤ +24V, Negative	-2.0		-1.2	
Single-Ended Input Fault Threshold	V_{TH_SEN}	Negative	-18		-15	V
SINGLE-ENDED HTL RECEIVERS (RxA, RxB, RxZ)						
Input Logic High Voltage	V_{IH_SE}	HITH is low	8		40	V
		HITH is high	13		40	
Input Logic Low Voltage	V_{IL_SE}	HITH is low	-40		6	V
		HITH is high	-40		11	
Input Hysteresis	ΔV_{ITH_SE}			270		mV
Input Current (A, B, Z)	$I_{\_HTL}$	V_{CC} = 0V or normally powered, V_{IN} = 24V			460	µA
Input Current ($\overline{A}$, $\overline{B}$, $\overline{Z}$)	$\overline{I}_{\_HTL}$	V_{CC} = 0V or normally powered, V_{IN} = 24V			460	µA
Fault Threshold Voltage	V_{TH_HTLF}		-18		-15	V
TTL RECEIVERS (RxA, RxB, RxZ, RxY, RxD2, RxD3)						
Input High Voltage	V_{IH_TTL}	TTL mode	2.0		40	V
Input Low Voltage	V_{IL_TTL}	TTL mode	-40		0.8	V
Input Hysteresis	V_{HY_TTL}	TTL mode		0.53		V

Electrical Characteristics (continued)

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current (A, B, Z, DIY, DI2, DI3)	$I_{\_TTL}$	TTL mode, V_{CC} = 0V or 5V, V_{IN} = 5V			85	µA
Input Current ($\overline{A}$, $\overline{B}$, $\overline{Z}$, $\overline{Y}$)	$I_{\_TTL}$	TTL mode, V_{CC} = 0V or 5V, V_{IN} = 5V			85	
Fault Threshold Voltage	V_{TH_TTLF}	Negative	-18		-15	V
		Positive	+15		+18	
DIGITAL INPUT RECEIVERS (DI2, DI3, RxY, RxZ)						
Input High Voltage	V_{IH_DI}	DI mode, HITH is high or low	8		40	V
Input Low Voltage	V_{IL_DI}	DI mode, HITH is high or low	-40		5.5	V
Input Hysteresis	V_{HY_DI}	DI mode, HITH is high or low		1.2		V
Current Sink	I_{DI}	DI mode, 0V ≤ V_{DI} ≤ 5V	0		2.6	mA
		DI mode, 8V ≤ V_{DI} ≤ 40V	2	2.5	3.3	
Fault Threshold Voltage	V_{TH_DIF}	DI mode	-18		-15	V
LOGIC INTERFACE (AO, $\overline{AFAULT}$, BO, $\overline{BFAULT}$, ZO, $\overline{ZFAULT}$, YO, $\overline{YFAULT}$, LO2, $\overline{D2FAULT/IRQ}$, LO3, $\overline{D3FAULT}$/SDO, DI/TTLY, DI/TTL2, DI/TTL3, SPI, TTL/SDI, SNGL/CLK, HITH/$\overline{CS}$)						
Input High Voltage	V_{IH}	DI/TTLY, DI/TTL2, DI/TTL3, SPI, TTL/SDI, SNGL/CLK, HITH/$\overline{CS}$	2/3 x V_L			V
Input Low Voltage	V_{IL}	DI/TTLY, DI/TTL2, DI/TTL3, SPI, TTL/SDI, SNGL/CLK, HITH/$\overline{CS}$			1/3 x V_L	V
Input Current	I_{IN}	DI/TTLY, DI/TTL2, DI/TTL3, SPI, TTL/SDI, SNGL/CLK, HITH/$\overline{CS}$	-1		+1	µA
Output High Voltage	V_{OH}	AO, BO, ZO, YO, LO2, LO3, AO, BO, ZO, YO, LO2, LO3, $\overline{D2FAULT}$/$\overline{IRQ}$, $\overline{D3FAULT}$/SDO, I_{OUT} = -3mA (Note 4)	V_L - 0.4V			V
Output Low Voltage	V_{OL}	AO, BO, ZO, YO, LO2, LO3, $\overline{D3FAULT}$/SDO, $\overline{AFAULT}$, $\overline{BFAULT}$, $\overline{ZFAULT}$, $\overline{YFAULT}$, $\overline{D2FAULT}$/$\overline{IRQ}$, I_{OUT} = +3mA			0.4	V
PROTECTION						
Thermal-Shutdown Threshold	T_{SHDN}	Temperature rising		+160		°C
Thermal-Shutdown Hysteresis	T_{HYST}			10		°C
Fault-Protected Input Voltage Range (A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$, DIY, $\overline{Y}$, DI2, DI3)	V_{IN_F}		-40		+40	V
ESD Protection (A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$, DIY, $\overline{Y}$, DI2, DI3)		IEC 61000-4-2 Air-Gap Discharge to GND		±7		kV
		IEC 61000-4-2 Contact Discharge to GND		±10		
		Human body model		±25		
ESD Protection (all other pins)		Human body model		±2		kV

Switching Characteristics

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (RxA, RxB, RxZ) (Note 3)						
RS-422 Maximum Data Rate	DR_{MAX422}	RS-422 mode	35			Mbps
RS-422 Receiver Propagation Delay	t_{DPLH_422}	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2			25	ns
	t_{DPHL_422}				25	
RS-422 Receiver Propagation Delay Skew $\|t_{DPLH\_422} - t_{DPHL\_422}\|$	$t_{HL-SKEW\_422}$	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2	0		5	ns
RS-422 Receiver Channel-to-Channel Skew	$\|t_{C-SKEW\_422}\|$	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2	0		8	ns
Differential HTL (D-HTL) Maximum Differential Data Rate	DR_{DHTL}	D-HTL mode	1			Mbps
D-HTL Receiver Propagation Delay	t_{DPLH_DHTL}	D-HTL mode, C_L = 15pF, V_{ID} = ±24V, Figures 1, 2			100	ns
	t_{DPHL_DHTL}				100	
D-HTL Differential Receiver Propagation Delay Skew $\|t_{DPLH\_DHTL} - t_{DPHL\_DHTL}\|$	t_{HLSKEW_DHTL}	D-HTL mode, C_L = 15pF, V_{ID} = ±24V, Figures 1, 2	0		20	ns
D-HTL Differential Receiver Channel-to-Channel Skew	$\|t_{CSKEW\_DHTL}\|$	D-HTL mode, C_L = 15pF, V_{ID} = ±24V, Figures 1, 2	0		8	ns
Single-Ended (SE-HTL) Maximum Switching Rate	SR_{SEHTL}	SE-HTL mode, HITH is high or low	400			kHz
SE-HTL Receiver Propagation Delay	t_{DPLH_SEHTL}	SE-HTL mode, HITH is high or low, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2	0		100	ns
	t_{DPHL_SEHTL}		0		100	
SE-HTL Receiver Propagation Delay Skew $\|t_{DPLH\_SEHTL} - t_{DPHL\_SEHTL}\|$	t_{HLSKEW_SEHTL}	SE-HTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V: HITH is low	0		28	ns
		SE-HTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V: HITH is high	0		20	
SE-HTL Receiver Channel-to-Channel Skew	$\|t_{CSKEW\_SEHTL}\|$	SE-HTL mode, HITH is high or low, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2	0		11	ns
TTL Maximum Switching Rate	SR_{TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V	5			MHz
TTL Receiver Propagation Delay	t_{DPLH_TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2			100	ns
	t_{DPHL_TTL}				100	
TTL Receiver Propagation Delay Skew ($t_{DPLH\_TTL} - t_{DPHL\_TTL}$)	t_{HLSKEW_TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2	0		52	ns

Switching Characteristics (continued)

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TTL Receiver Channel-to-Channel Skew	$\lvert t_{CSKEW\_TTL} \rvert$	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2	0		11	ns
Digital Input (DI) Maximum Switching Rate	SR_{DZ}	RxZ only, DI mode, SPI = high	400			kHz
DI Propagation Delay	t_{DPLH_DZ}	RxZ only, DI mode, SPI = high, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2			300	ns
	t_{DPHL_DZ}				300	
DI Receiver Propagation Delay Skew $\lvert t_{DPLH\_DZ} - t_{DPHL\_DZ} \rvert$	t_{RSKEW_DZ}	RxZ only, DI mode, SPI = high, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2	0		28	ns
DI Maximum Glitch Duration for Glitch Rejection	t_{GL}	RxZ only, DI mode, SPI = high			80	ns
DI Admitted Pulse Duration	t_{PASS}	RxZ only, DI mode, SPI = high	300			ns
RECEIVER (RxY) (Note 4)						
RS-422 Maximum Data Rate	DR_{MAX422}	RS-422 mode	35			Mbps
RS-422 Receiver Propagation Delay	t_{DPLH_422}	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2			25	ns
	t_{DPHL_422}				25	ns
RS-422 Receiver Propagation Delay Skew $\lvert t_{DPLH\_422} - t_{DPHL\_422} \rvert$	$t_{HL\text{-}SKEW\_422}$	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2	0		5	ns
RS-422 Receiver Channel-to-Channel Skew	$\lvert t_{C\text{-}SKEW\_422} \rvert$	RS-422 mode, C_L = 15pF, V_{ID} = ±3V, Figures 1, 2	0		8	ns
TTL Maximum Switching Rate	SR_{TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V	5			MHz
TTL Receiver Propagation Delay	t_{DPLH_TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2			100	ns
	t_{DPHL_TTL}				100	
TTL Receiver Propagation Delay Skew $\lvert t_{DPLH\_TTL} - t_{DPHL\_TTL} \rvert$	t_{HLSKEW_TTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2	0		52	ns
Digital Input (DI) Maximum Switching Rate	SR_{DY}	DI mode	400			kHz
DI Propagation Delay	t_{DPLH_DY}	DI mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2			300	ns
	t_{DPHL_DY}				300	

Switching Characteristics (continued)

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DI Receiver Propagation Delay Skew $\|t_{DPLH\_DY} - t_{DPHL\_DY}\|$	t_{RSKEW_DY}	DI mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2	0		100	ns
DI Maximum Glitch Duration for Glitch Rejection	t_{GL}	DI/TTLY is high or low			80	ns
DI Admitted Pulse Duration	t_{PASS}	DI/TTLY is high or low	300			ns
RECEIVER (DI2, DI3) (Note 4)						
Digital Input (DI) Maximum Switching Rate	SR_{DI}	DI mode	20			kHz
DI Propagation Delay	t_{DPLH_DI}	DI mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +24V, Figures 1, 2			5	µs
	t_{DPHL_DI}				5	
DI Receiver Propagation Delay Skew ($t_{DPLH\_DI} - t_{DPHL\_DI}$)	t_{RSKEW_DI}	DI mode, C_L = 15pF		60		ns
Maximum Glitch Duration for Glitch Rejection	t_{GL}	DI mode, DI/TTL_ is high or low			80	ns
Admitted Pulse Length	t_{PASS}	DI mode, DI/TTL_ is high or low	350			ns
TTL Maximum Switching Rate	SR_{DI_TTL}	TTL mode	20			kHz
TTL Receiver Propagation Delay	t_{DPLH_DITTL}	TTL mode, C_L = 15pF, 0V ≤ V_{IN} ≤ +5V, Figures 1, 2			5	µs
	t_{DPHL_DITTL}				5	
TTL Receiver Propagation Delay Skew ($t_{DPLH\_DITTL} - t_{DPHL\_DITTL}$)	t_{HLSKEW_DITTL}	TTL mode, C_L = 15pF, Figures 1, 2		80		ns
FAULT DETECTION ($\overline{\text{AFAULT}}$, $\overline{\text{BFAULT}}$, $\overline{\text{ZFAULT}}$, $\overline{\text{D2FAULT}}$/IRQ, $\overline{\text{D3FAULT}}$/SDO) (Note 4)						
Differential Fault Propagation Delay to $\overline{\text{\_FAULT}}$ Output Active	t_{DFLH}	R_{FAULT} = 5kΩ, C_{FAULT} = 15pF, RS-422 and DHTL modes, Figures 1, 4; FLTR = 0			18	µs
		FLTR = 1			1400	
	t_{DFHL}	FLTR = 0			6	
		FLTR = 1			1400	
Differential Slew Rate to Avoid Fault Alarm Output		R_{FAULT} = 5kΩ, C_{FAULT} = 15pF, FLTR = 0, RS-422 and D-HTL modes, Figures 1, 4	1			V/µs
Single Ended Propagation Delay to $\overline{\text{\_FAULT}}$ Output Active	t_{SEFLH}	R_{FAULT} = 5kΩ, C_{FAULT} = 15pF, all modes			1.4	ms
	t_{SEFHL}				1.4	

Switching Characteristics (continued)

(V_{CC} = 5V±10%, V_L = 1.62V to V_{CC}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SPI TIMING (Figure 5)							
SNGL/CLK Clock Period	t_{CH+CL}			80			ns
SNGL/CLK Pulse-Width High	t_{CH}			25			ns
SNGL/CLK Pulse-Width Low	t_{CL}			25			ns
HITH/$\overline{CS}$ Fall to SNGL/CLK Rise Time	t_{CSS}			15			ns
TTL/SDI Hold Time	t_{DH}			15			ns
TTL/SDI Setup Time	t_{DS}			15			ns
Output Data Propagation Delay	t_{DO}	C_L = 10pF, SNGL/CLK falling-edge to $\overline{D3FAULT}$/SDO stable.	V_L ≥ 1.62V			32	ns
			V_L ≥ 3.3V			28	
$\overline{D3FAULT}$/SDO Rise and Fall Times	t_{FT}	Rising	V_L = 1.62V		24		ns
			V_L = 3.3V		2		
		Falling	V_L = 1.62V		11		
			V_L = 3.3V		1		
HITH/$\overline{CS}$ Hold Time	t_{CSH}	V_L =1.62V or 3.3V		10			ns
		V_L = 5.5V		5			
HITH/$\overline{CS}$ Pulse-Width High	t_{CSPW}	V_L = 1.62V or 3.3V		10			ns
		V_L = 5.5V		5			

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Currents into the device are positive; all currents out the device are negative. All voltages are referenced to ground, unless otherwise noted.

Note 3: In pin-control mode, $\overline{D3FAULT}$/SDO is open-drain. In SPI mode, $\overline{D3FAULT}$/SDO is a push-pull output.

Note 4: Capacitive load includes test probe and fixture capacitance.

Test Circuits and Waveforms

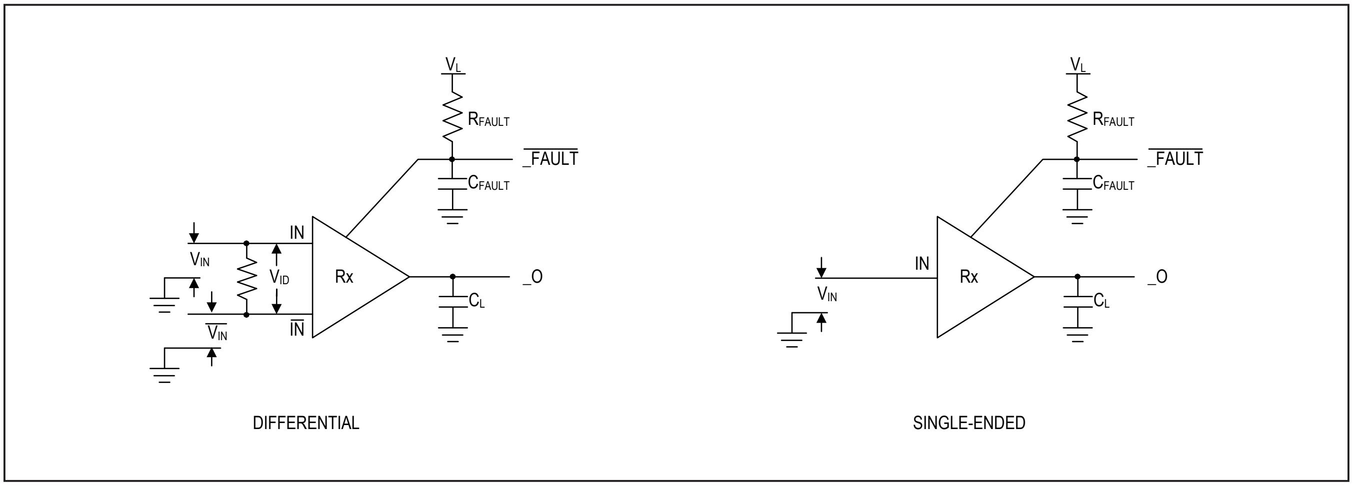


Figure 1. Receiver Test Circuit

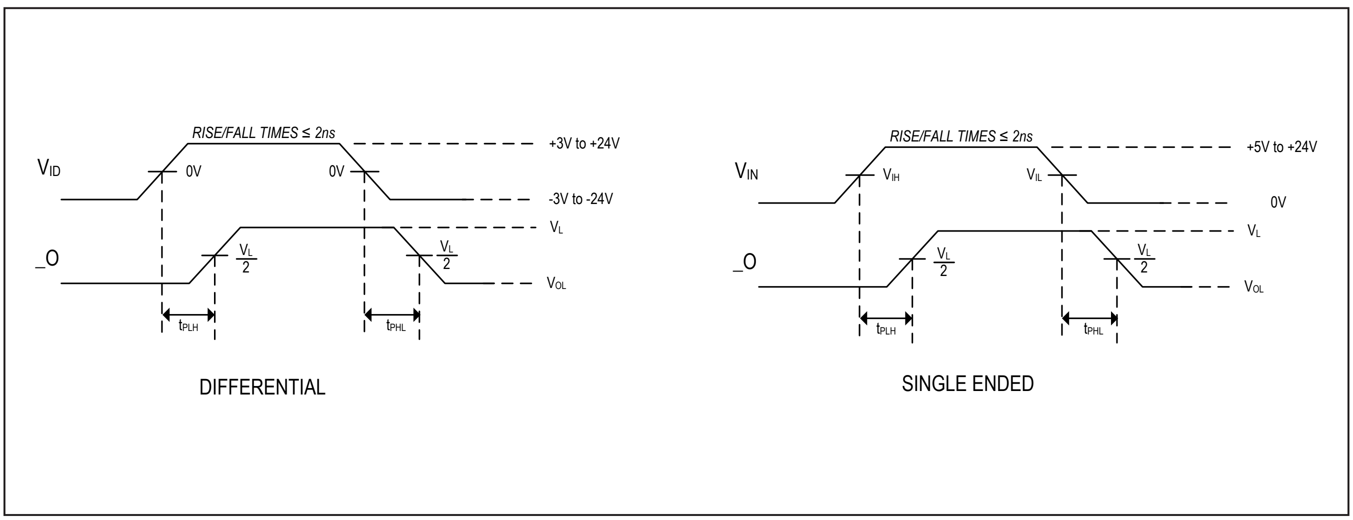


Figure 2. Receiver Propagation Delay

Test Circuits and Waveforms (continued)

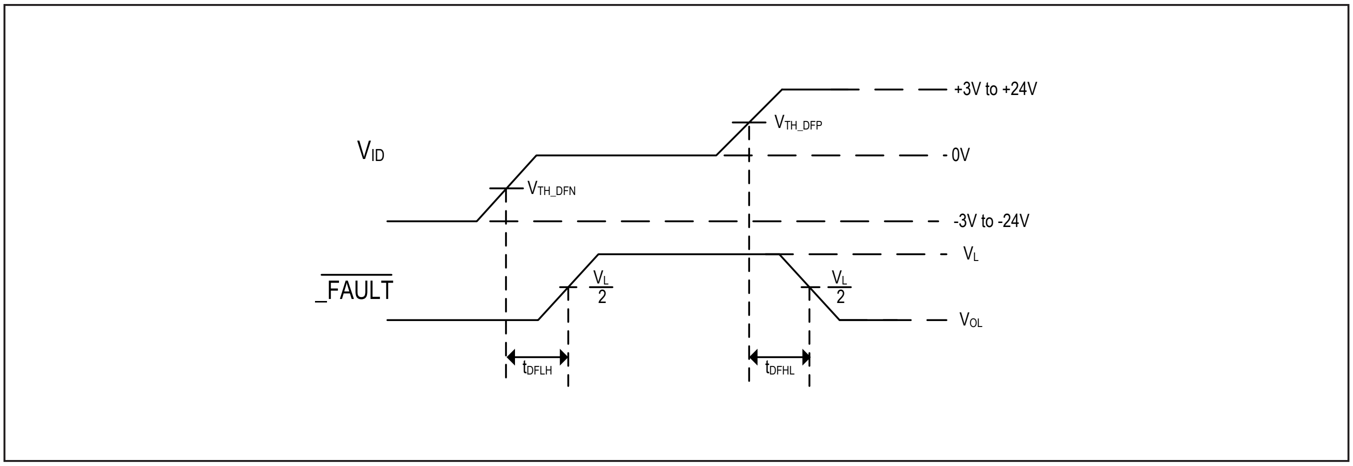


Figure 3. Fault Detection Timing

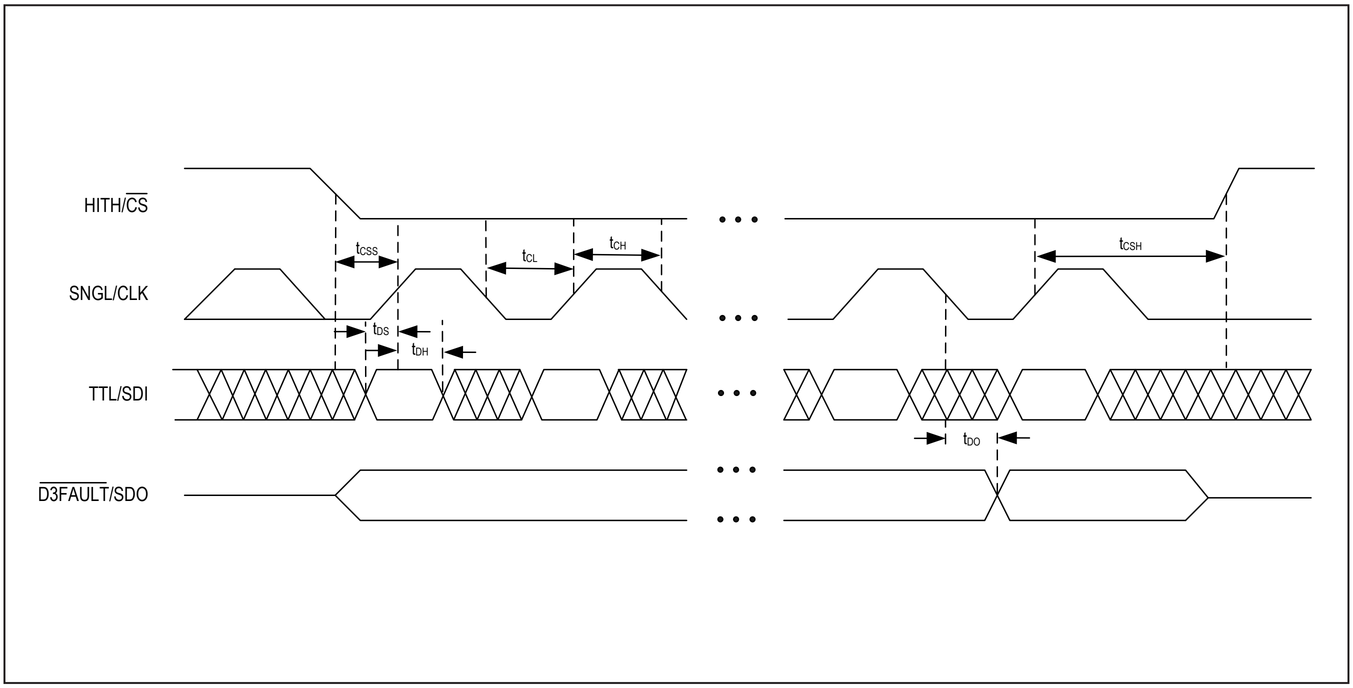
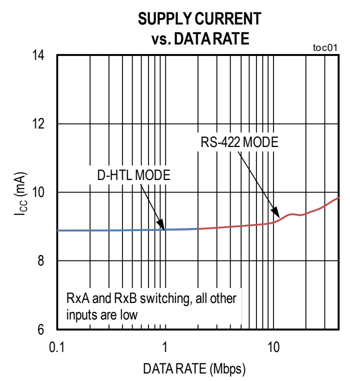
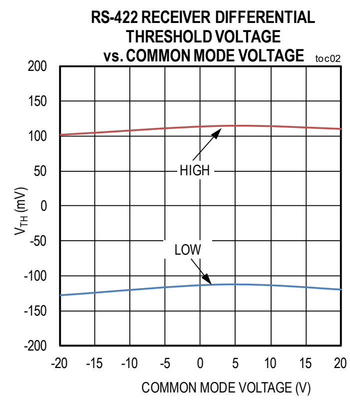


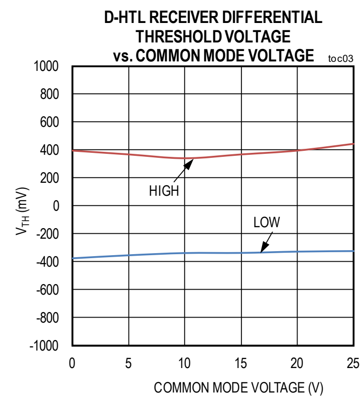
Figure 4. SPI Timing Diagram

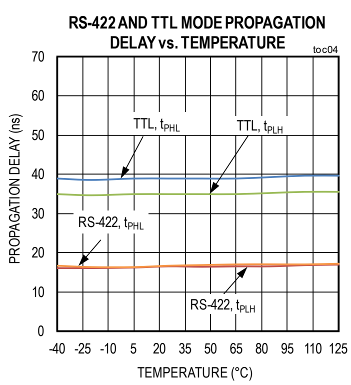
Typical Operating Characteristics

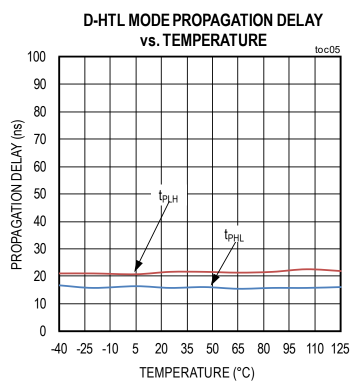
(V_{CC} = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.)

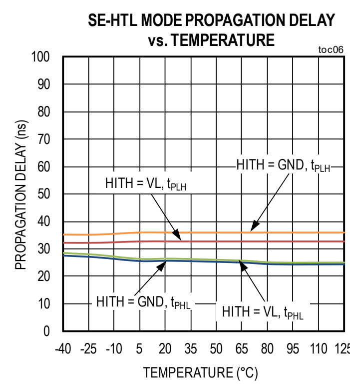


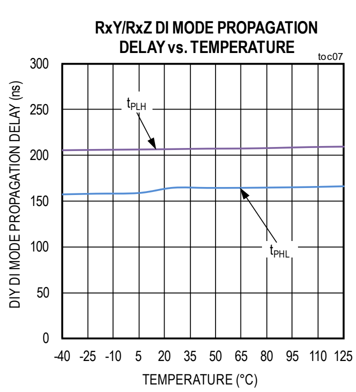


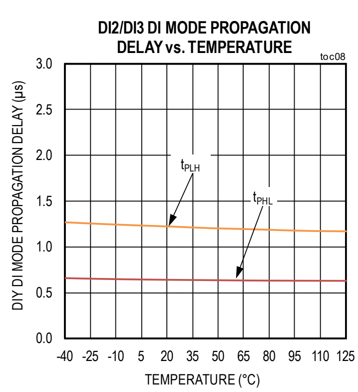


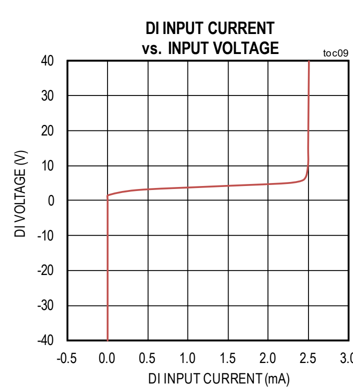








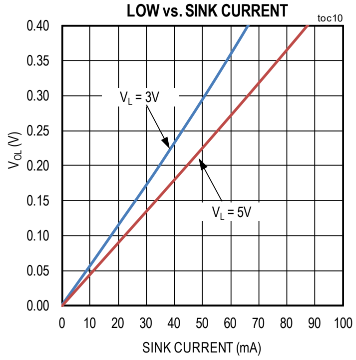




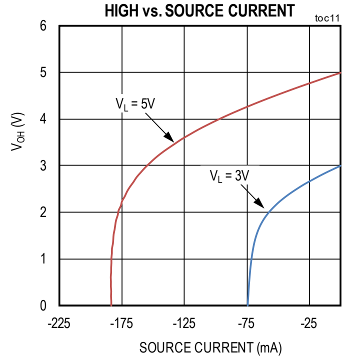
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.)

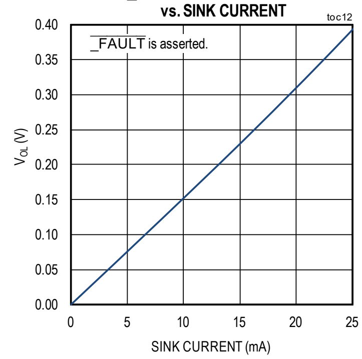
RECEIVER OUTPUT VOLTAGE LOW vs. SINK CURRENT



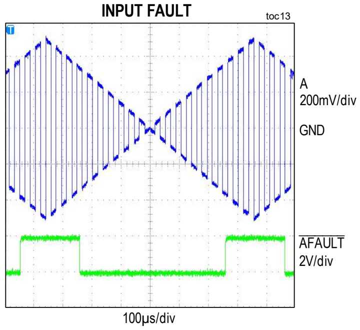
RECEIVER OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



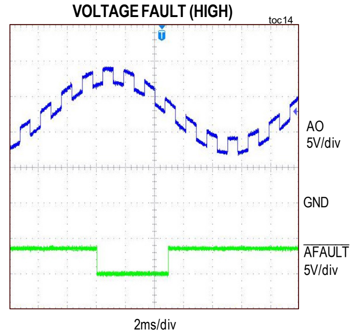
_FAULT OUTPUT VOLTAGE vs. SINK CURRENT



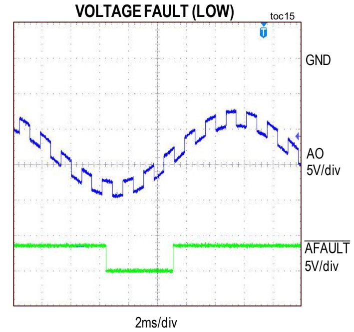
LOW DIFFERENTIAL INPUT FAULT



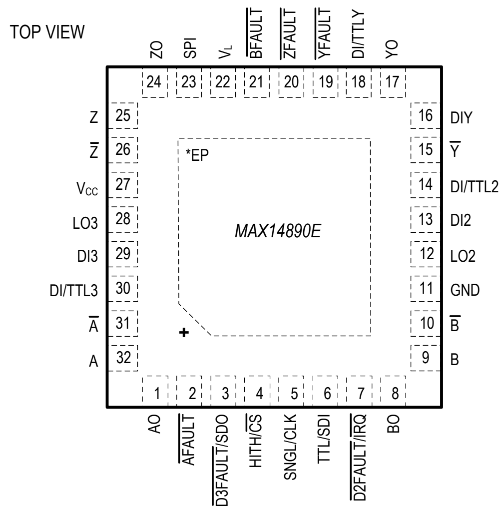
RS-422 MODE COMMON-MODE VOLTAGE FAULT (HIGH)



RS-422 MODE COMMON MODE VOLTAGE FAULT (LOW)



Pin Configuration



TQFN
5mm x 5mm

** Exposed Pad. Connect to GND.*

Pin Description

PIN	NAME	FUNCTION
1	AO	Noninverting RS-422/HTL/TTL Receiver Input A.
2	$\overline{\text{AFAULT}}$	Open-Drain Fault Output for Receiver A. $\overline{\text{AFAULT}}$ asserts low during a fault condition on receiver A (RxA) . See the *Detecting Faults* section for more information.
3	$\overline{\text{D3FAULT}}$/ SDO	Receiver D3 Open-Drain Fault Output/SPI Serial Data Out. In pin mode (SPI is low), $\overline{\text{D3FAULT}}$/SDO asserts low during a fault condition on the D3 receiver. See the *Detecting Faults* section for more information. In SPI mode (SPI is high), $\overline{\text{D3FAULT}}$/SDO is the SPI serial data output and is in a push-pull configuration. $\overline{\text{D3FAULT}}$/SDO is high-impedance in SPI mode with HITH/$\overline{\text{CS}}$ is high.
4	HITH/$\overline{\text{CS}}$	Single-Ended HTL Threshold Select Input/SPI Chip Select. In pin mode (SPI is low), HITH/$\overline{\text{CS}}$ sets the input thresholds for the single-ended HTL signals. In this mode, drive HITH/$\overline{\text{CS}}$ high to enable the 12V (typ) thresholds or drive HITH/$\overline{\text{CS}}$ low to enable the 7V (typ) thresholds. In SPI mode (SPI is high), HITH/$\overline{\text{CS}}$ is the SPI chip select input.
5	SNGL/CLK	Single-Ended Receiver Input Select/SPI Clock Input. In pin mode (SPI is low), SNGL/CLK selects the mode for the inputs of receivers A,B, and Z. In this mode, drive SNGL/CLK high to enable the receivers for single-ended TTL or HTL operation. Drive SNGL/CLK low for differential (RS-422 or DHTL) operation. See the *Truth Tables* for more information. In SPI mode (SPI is high), SNGL/CLK is the SPI clock input.
6	TTL/SDI	TTL Mode Select Input/SPI Serial Data Input. In pin mode (SPI is low), enables TTL operation for receivers A, B, and Z. In this mode, drive TTL/SDI high to enable TTL or RS-422 operation. Drive TTL/SDI low to select DHTL or SEHTL operation for those receivers. In SPI mode (SPI is high), TTL/SDI is the serial data input.
7	$\overline{\text{D2FAULT}}$/ $\overline{\text{IRQ}}$	Receiver D2 Open-Drain Fault Output/SPI IRQ Output. In pin mode (SPI is low), $\overline{\text{D2FAULT}}$/$\overline{\text{IRQ}}$ asserts low during a fault condition on the D2 receiver (RxD2). In SPI mode (SPI is high), $\overline{\text{D2FAULT}}$/$\overline{\text{IRQ}}$ asserts low when a fault bit is set. See the *Serial SPI Control* section for more information.

Pin Description (continued)

PIN	NAME	FUNCTION
8	BO	Receiver B Output.
9	B	Non-Inverting RS-422/HTL/TTL Input for Receiver B.
10	$\overline{B}$	Inverting Input for Receiver B. $\overline{B}$ is only used when differential mode is enabled.
11	GND	Ground
12	LO2	Receiver DI2 Output.
13	DI2	Digital/TTL Input for DI2 Receiver.
14	DI/TTL2	Digital Input/TTL Select Input for DI2 Receiver. See the *Truth Tables* for more information. In SPI Mode, the DI mode current sink for the DI2 receiver can only be enabled or disabled using the DI/TTL2 pin. Set DI/TTL2 high to enable the current sink and set DI/TTL2 low to disable the current sink on DI2.
15	$\overline{Y}$	Inverting RS-422 Input for Receiver Y. $\overline{Y}$ is used only when differential mode is enabled.
16	DIY	Digital/TTL/Non-inverting RS-422 Input for Receiver Y.
17	YO	Receiver Y Output.
18	DI/TTLY	Digital Input/TTL/RS-422 Select Input for Receiver Y. See the *Truth Tables* for more information. In SPI Mode, the DI mode current sink for the DIY receiver, when the Y receiver is configured as a DI input, can only be enabled or disabled using the DI/TTLY pin. Set DI/TTLY high to enable the current sink and set DI/TTLY low to disable the current sink on DIY.
19	$\overline{\text{YFAULT}}$	Open-Drain Fault Output for Receiver Y. $\overline{\text{YFAULT}}$ asserts low during a fault condition on receiver Y. See the Fault Conditions section for more information.
20	$\overline{\text{ZFAULT}}$	Open-Drain Fault Output for Receiver Z. $\overline{\text{ZFAULT}}$ asserts low during a fault condition on receiver Z. See the Fault Conditions section for more information.
21	$\overline{\text{BFAULT}}$	Open-Drain Fault Output for Receiver B. $\overline{\text{BFAULT}}$ asserts low during a fault condition on receiver B. See the Fault Conditions section for more information.
22	V_L	Logic Interface Supply Input. V_{CC} must always be greater than or equal to V_L.
23	SPI	Serial/Parallel Select Input. Drive SPI low to enable pin-mode operation. Drive SPI high to enable SPI mode operation.
24	ZO	Receiver Z Output.
25	Z	Non-Inverting RS-422/HTL/TTL Input for Receiver Z.
26	$\overline{Z}$	Inverting Input for Receiver Z. $\overline{Z}$ is only used when the receiver is configured for differential mode.
27	V_{CC}	Supply Input. Bypass V_{CC} to ground through a 0.1µF capacitor as close to the device as possible. V_{CC} must always be greater than or equal to V_L.
28	LO3	Receiver D3 Output.
29	DI3	Digital/TTL Input for the D3 Receiver.
30	DI/TTL3	Digital Input/TTL Select Input for the D3 Receiver. See the *Truth Tables* for more information. In SPI Mode, the DI mode current sink for the DI3 receiver can only be enabled or disabled using the DI/TTL3 pin. Set DI/TTL3 high to enable the current sink and set DI/TTL3 low to disable the current sink on DI3.
31	$\overline{A}$	Inverting Input for Receiver A. $\overline{A}$ is used only when differential mode is enabled.
32	A	Non-inverting RS-422/HTL/TTL Input for Receiver A.
-	EP	Exposed pad. Connect EP to ground. Not intended as the primary ground connection.

Truth Tables

Table 1. RxA, RxB, RxZ and RxY Receiver Settings (Pin-Control Mode)

INPUTS			RECEIVER OPERATION	
SNGL/CLK	**TTL/SDI**	**DI/TTLY**	**RxA, RxB, RxZ**	**RxY**
L	L	L	D-HTL	TTL
L	L	H	D-HTL	DI
L	H	L	RS-422	RS-422
L	H	H	RS-422	DI
H	L	L	SE-HTL	TTL
H	L	H	SE-HTL	DI
H	H	L	TTL	TTL
H	H	H	TTL	DI

Table 2. RxD2 Receiver Settings (Pin-Control Mode)

DI/TTL2	RxD2 MODE OF OPERATION
L	TTL
H	DI

Table 3. RxD3 Receiver Input Settings (Pin-Control Mode)

DI/TTL3	RxD3 MODE OF OPERATION
L	TTL
H	DI

Table 4. DI Mode Receiver Logic (RxY, RxD2, RxD3)

DIY, DI2, DI3	YO, LO2, LO3	_$\overline{\text{FAULT}}$
$-40V < V_{IN} \leq -18V$	L	L
$-18V < V_{IN} < -15V$	L	Indeterminate
$-15V < V_{IN} < +6V$	L	H
$+6V < V_{IN} < +8V$	Indeterminate	H
$+8V \leq V_{IN} < +40V$	H	H

Table 5. Single-Ended TTL Mode Receiver Logic

INPUT (A, B, Z, DIY, DI2, DI3)	OUTPUT (AO, BO ZO, YO, LO2, LO3)	$\overline{\text{FAULT}}$	FAULT CONDITION
$-40V < V_{IN} < -18V$	L	L	Low Input Fault
$-18V < V_{IN} < -15V$	L	Indeterminate	Indeterminate
$-15V < V_{IN} < +0.8V$	L	H	No Fault
$+0.8V < V_{IN} < +2.0V$	Indeterminate	H	No Fault
$+2.0V \le V_{IN} < +15V$	H	H	No Fault
$+15V \le V_{IN} < +18V$	H	Indeterminate	Indeterminate
$+18V \le V_{IN} < +40V$	H	L	High Input Fault

Table 6. SE-HTL Mode Receiver Logic (RxA, RxB, RxZ)

HITH	INPUT VOLTAGE (A, B, Z)	OUTPUT STATE (AO, BO, ZO)	$\overline{\text{FAULT}}$	FAULT CONDITION
L	$-40V < V_{IN} < -18V$	L	L	Low Input Fault
L	$-18V < V_{IN} < -15V$	L	Indeterminate	Indeterminate
L	$-15V < V_{IN} < +6V$	L	H	No Fault
L	$+6V < V_{IN} < +8V$	Indeterminate	H	No Fault
L	$+8V \le V_{IN} < +40V$	H	H	No Fault
H	$-40V < V_{IN} < -18V$	L	L	Low Input Fault
H	$-18V < V_{IN} < -15V$	L	Indeterminate	Indeterminate
H	$-15V < V_{IN} < +11V$	L	H	No Fault
H	$+11V < V_{IN} < +13V$	Indeterminate	H	No Fault
H	$+13V \le V_{IN} < +40V$	H	H	No Fault

Table 7. D-HTL Mode Receiver Logic (RxA, RxB, RxZ)

DIFFERENTIAL INPUT VOLTAGE	SINGLE-ENDED INPUT VOLTAGE (A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$)	OUTPUT STATE (AO, BO, ZO)	$\overline{FAULT}$	FAULT CONDITION
V_{ID} > +2V	-10V < V_{SE}	H	H	No Fault
+1.2V < V_{ID} < +2V		H	Indeterminate	Indeterminate
-0.9V ≤ V_{ID} ≤ +0.9V		Indeterminate	L	Low Differential Input Voltage Fault
-2V ≤ V_{ID} ≤ -1.2V		L	Indeterminate	Indeterminate
V_{ID} ≤ -2V		L	H	No Fault
X	-18V < V_{SE} < -15V	VALID*	Indeterminate	Single-Ended Voltage Fault
X	-40V < V_{SE} < -18V	VALID*	L	Single-Ended Voltage Fault

X = Don't care

**Receiver operates normally, although thresholds may deviate from limits in Electrical Characteristics Table*

Table 8. RS-422 Mode Receiver Logic (RxA, RxB, RxZ, RxY)

DIFFERENTIAL INPUT VOLTAGE	SINGLE-ENDED INPUT VOLTAGE (A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$, Y, $\overline{Y}$)	OUTPUT STATE (AO, BO, ZO, YO)	$\overline{FAULT}$	FAULT CONDITION
V_{ID} > +0.45V	-20V ≤ V_{SE} ≤ +20V	H	H	No Fault
+0.27V < V_{ID} < +0.45V +0.45V		H	Indeterminate	Indeterminate
-0.2V ≤ V_{ID} ≤ +0.2V		Indeterminate	L	Low Differential Input Voltage Fault
-0.45V ≤ V_{ID} ≤ -0.27V		L	Indeterminate	Indeterminate
V_{ID} ≤ -0.45V		L	H	No Fault
X	-40V < V_{SE} < -18V	VALID*	L	Single-Ended Voltage Fault
X	-18V < V_{SE} < -15V	VALID*	Indeterminate	Single-Ended Indeterminate Voltage
X	+15V < V_{SE} < +18V	VALID*	Indeterminate	Single-Ended Indeterminate Voltage
X	+18V < V_{SE} < +40V	VALID*	L	Single-Ended Voltage Fault

X = Don't care

**Receiver operates normally, although thresholds may deviate from limits in Electrical Characteristics Table*

Detailed Description

The MAX14890E is an incremental encoder receiver containing four differential receivers and two single-ended receivers. All four differential receivers support RS-422 and TTL operation. Three of these differential receivers can be configured for differential and single-ended HTL operation. In RS-422 mode, these receivers feature a wide common mode input range of -20V to +20V making it resilient to common mode noise.

The auxiliary IEC 61131-2 Type-1/Type-3 24V digital inputs allow connection of proximity sensors. The digital inputs can be individually configured for TTL operation.

All receiver input signals are fault protected to voltage shorts in the ±40V range. Per channel fault detection provides warning of irregular conditions, like small differential signals, shorts, opens, over- and undervoltages.

SPI or Pin-Control Mode Selection

The MAX14890E provides a selectable SPI or pin interface to set the input thresholds and functionality of the receivers. Drive SPI high to use the SPI interface. Drive SPI low to use the pin interface.

SPI mode allows for higher flexibility by allowing individual receiver configuration. See the *Serial SPI Control* section for more information.

TTL Operation

All 6 of the receivers can be configured for single-ended TTL operation. Complimentary/unused inputs can be left unconnected in all single-ended modes like TTL, DI, and SE-HTL.

In pin-control mode, drive the TTL/SDI and SNGL/CLK inputs high to enable TTL operation on the RxA, RxB, and RxZ receivers. To enable TTL operation on RxY receiver, set DI/TTLY low. To enable TTL operation on the RxD2 or RxD3 receivers, drive the DI/TTL2 or DI/TTL3 inputs low. See the *Truth Tables* section for more information.

In SPI mode, each receiver can be enabled for TTL operation individually. Set the associated _SNGL and _TTL bits to enable TTL mode for each receiver. See the *Serial SPI Control* section for more information.

Single-Ended HTL Operation (SE-HTL)

The RxA, RxB, and RxZ receivers can be configured for single-ended HTL operation. Complimentary/unused inputs can be left unconnected in all single-ended modes (TTL, DI, and SE-HTL).

In pin-control mode, drive the TTL/SDI input low and the SNGL/CLK input high to enable SE-HTL mode on the RxA, RxB, and RxZ receivers.

In SPI mode, each of the RxA, RxB, and RxZ receivers can be individually enabled for SE-HTL functionality. See the *Serial SPI Control* section for more information.

Differential HTL (D-HTL) Operation

The RxA, RxB, and RxZ receivers can be configured for D-HTL operation. Input signals up to ±40V can be accepted in D-HTL mode.

In pin-control mode, set the SNGL/CLK and TTL/SDI inputs low to enable D-HTL functionality for the RxA, RxB, and RxZ receivers. See the *Truth Tables* section for more information.

In SPI mode, each of the RxA, RxB, and RxZ receivers can be individually enabled for D-HTL functionality. See the *Serial SPI Control* section for more information.

RS-422 Operation

The RxA, RxB, RxZ, and RxY receivers can be configured for RS-422 operation. These receivers include a wide common-mode input range (-20V to +20V) in this mode.

In pin-control mode, set the SNGL/CLK input low and the TTL/SDI input high to enable RS-422 functionality for the RxA, RxB, RxZ, and RxY receivers. See the *Truth Tables* section for more information.

In SPI mode, each receiver can be individually enabled for RS-422 functionality. See the *Serial SPI Control* section for more information.

Equivalent Input Circuit

In RS-422, TTL, SE-HTL, and D-HTL modes, the inputs pins have the equivalent circuit shown in Figure 5. When the RxA, RxB, RxZ, and/or RxY inputs are configured for TTL mode and are open/not connected, the input is pulled up to 2.64V (typ), resulting in a logic high on the receiver output.

RxD2 and RxD3 have high impedance inputs in TTL mode (Figure 6). Leaving DI2 or DI3 unconnected in this mode will result in an unknown logic state on the receiver output .

Detecting Faults

Signal integrity from the encoder is essential for reliable system operation. Degraded signals could cause problems ranging from simple miscounts to loss of position. The MAX14890E detects common RS-422/HTL/TTL/DI faults. These faults include low differential input signals, open-wire, short-circuits and input voltages that are outside normal operating voltage ranges (below -18V and above +18V). See the *Truth Tables* for more information.

Detecting Small Differential Signals

In RS-422 and differential HTL (D-HTL) modes, the receivers detect small DC and AC signals. Small DC signals can occur due to open wires or shorts, both of which are explained in the following sections. Small differential AC signals can result due to cable attenuation of long or inadequate cables, or due to poor wiring.

Detecting Short Circuit and Open-Circuit Faults (RS-422 and D-HTL Operation)

The MAX14890E receivers detect short circuits on the inputs in RS-422 and D-HTL modes. When the A and $\overline{A}$ inputs are shorted together, the differential input voltage is 0V, generating a low differential input voltage fault (Figure 7). Open-circuit detection is similar to detecting a short-circuit condition and relies on the differential termination resistor across the receiver inputs. When an input is open, the termination resistor pulls the non-inverting and inverting inputs to the same voltage, generating a fault condition.

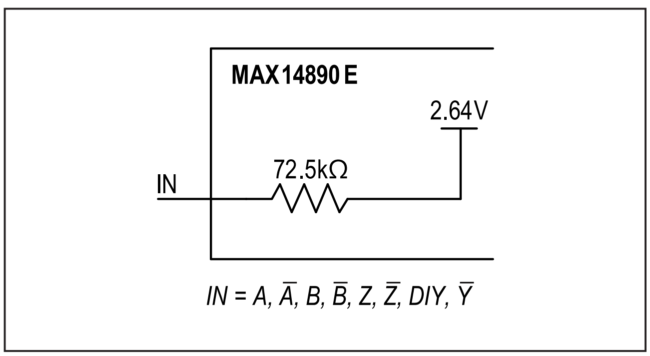


Figure 5. Equivalent Input Circuit for TTL, RS-422, SE-HTL and D-HTL Modes (RxA, RxB, RxZ, RxY)

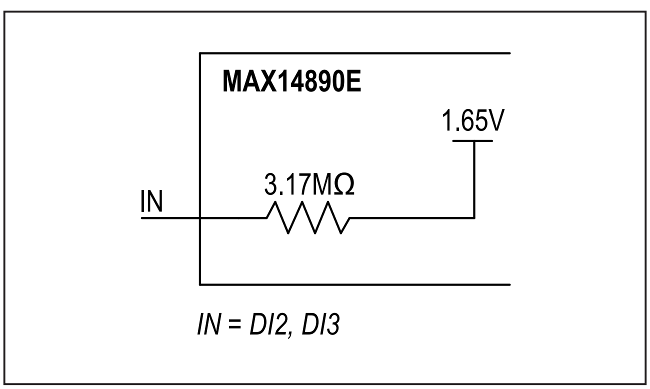


Figure 6. Equivalent Input Circuit for RxD2 and RxD3 in TTL Mode

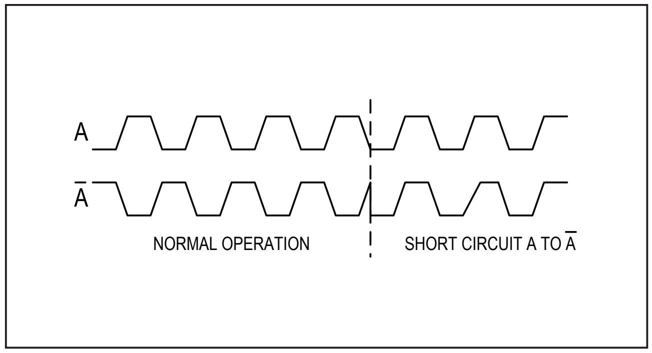


Figure 7. Short Circuit Detection

The $\overline{\text{\_FAULT}}$ output asserts when either a short-circuit or open-circuit conditions is detected.

Thermal Shutdown

The MAX14890E enters thermal shutdown when the chip temperature rises to above 160°C (typ). Receiver outputs are undefined and the $\overline{\text{\_FAULT}}$ outputs are off when the device is in thermal shutdown.

Serial SPI Control

SPI Interface

The MAX14890E can be configured and monitored through an SPI interface. The SPI interface allows for greater flexibility for independent receiver mode configuration.

Drive the SPI input high to enable SPI functionality. The $\overline{\text{AFAULT}}$, $\overline{\text{BFAULT}}$, $\overline{\text{ZFAULT}}$, $\overline{\text{YFAULT}}$ and receiver outputs (AO, BO, ZO, YO, LO2 and LO3) are operational in SPI mode. All configuration bits are 0 (default) when SPI is pulled high, setting RxA, RxB, and RxZ in D-HTL mode, RxY in RS-422 mode, and RxD2 and RxD3 in TTL mode. After SPI is pulled high, all $\overline{\text{D3FAULT}}$/SDO data is 0s during the first SPI cycle.

The MAX14890E samples the TTL/SDI input on the rising edge of the SNGL/CLK signal, while $\overline{\text{D3FAULT}}$/SDO is generated on the falling edge of the SNGL/CLK.

The HITH/$\overline{\text{CS}}$ SPI chip select input signal features a glitch filter that improves robustness against EMI, requiring a longer setup time.

The MAX14890E must receive at least 16 clock pulses on SNGL/CLK between the HITH/$\overline{\text{CS}}$ falling edge and the HITH/$\overline{\text{CS}}$ rising edge (SPI command transfer). If less than 16 pulses are received, the device ignores the TTL/SDI data received. If more than 16 pulses are received, only the last 16 bits of data before HITH/$\overline{\text{CS}}$ rises are utilized. Figure 8 shows a standard SPI cycle.

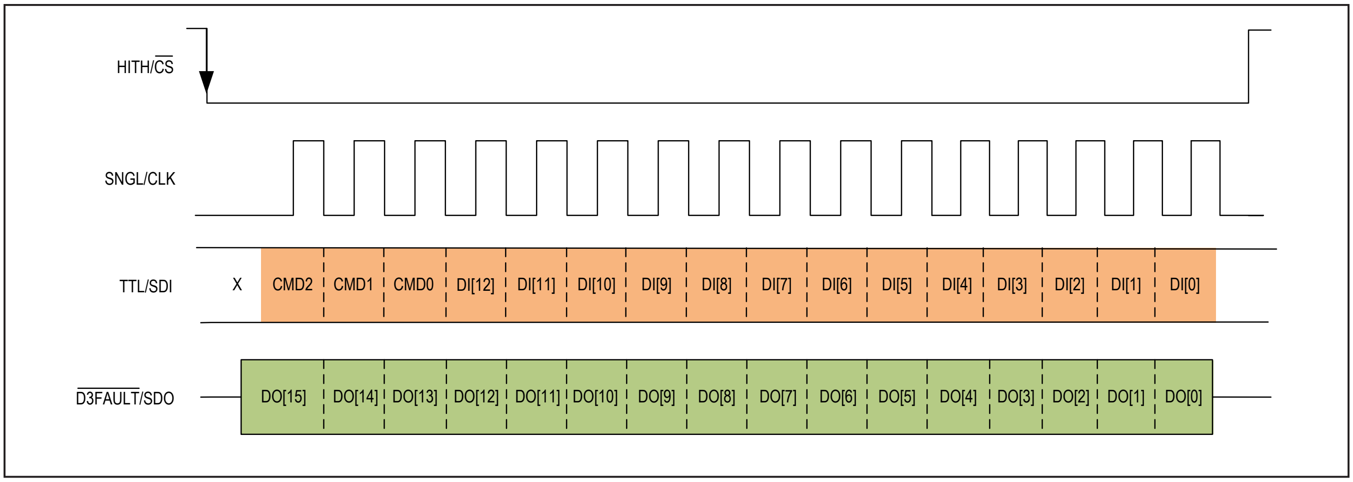


Figure 8. Standard SPI Cycle

The 16 bits of $\overline{D3FAULT}$/SDO data generated by the MAX14890E depend on the previously received SPI command. If more than 16 SNGL/CLK cycles are present during an SPI cycle, $\overline{D3FAULT}$/SDO will output the data received on TTL/SDI with a 16 bit latency, allowing for daisy-chain transfers.

Register Functionality

Three command bits (CMD[2:0]) and 13 mode selection bits control the individual receiver input thresholds and output behavior on the MAX14890E in SPI mode. Table 10 shows the functionality of the CMD[2:0] bits.

Change Configuration with Detailed Fault Readback Command (CMD[2:0] = 101)

Write 101 to bits CMD[2:0] to enable configuring the individual receivers through the SPI interface (Figure 9). Bit settings are equivalent to the hardware inputs, HITH/$\overline{CS}$, TTL/SDI, SNGL/CLK, and DI. See Tables 11-14 for more information.

The HITH bit enables/disables the single-ended HTL thresholds for all receivers set in HTL mode.

See the *Fault Filtering* section for more information on the FLTR bit.

The detailed fault readback consists of 16 $\overline{D3FAULT}$/SDO bits. The ADFLT, BDFLT, ZDFLT, YDFLT bits are set when a differential fault error occurs for each receiver. The AFLT, $\overline{AFLT}$, BFLT, $\overline{BFLT}$, ZFLT, $\overline{ZFLT}$, YFLT, DIYFLT, D2LFLT, D2HFLT, D3LFLT, D3HFLT bits are set when a single-ended voltage fault occurs for each input. See Table 15.

Table 10. SPI Command Bit Settings

CMD2	CMD1	CMD0	CHANGES CONFIGURATION?	FUNCTION
1	0	1	YES	Change configuration. New configuration is set by bits DI[13:0]. Read detailed fault status is the next SPI cycle. See the *Change Configuration with Detailed Fault Readback Command* section for more information.
0	1	0	NO	Read current fault output and receiver outputs in next SPI cycle. See the *Fault and Receiver Status Command* section for more information.
1	1	1	NO	Read current configuration in next SPI cycle. Do not change configuration. See the *Readback Current Receiver Command* section for more information.
000, 001, 011, 100,110			NO	Read detailed fault status in next SPI cycle. Do not change configuration. See the *Detailed Fault Readback* section for more information.

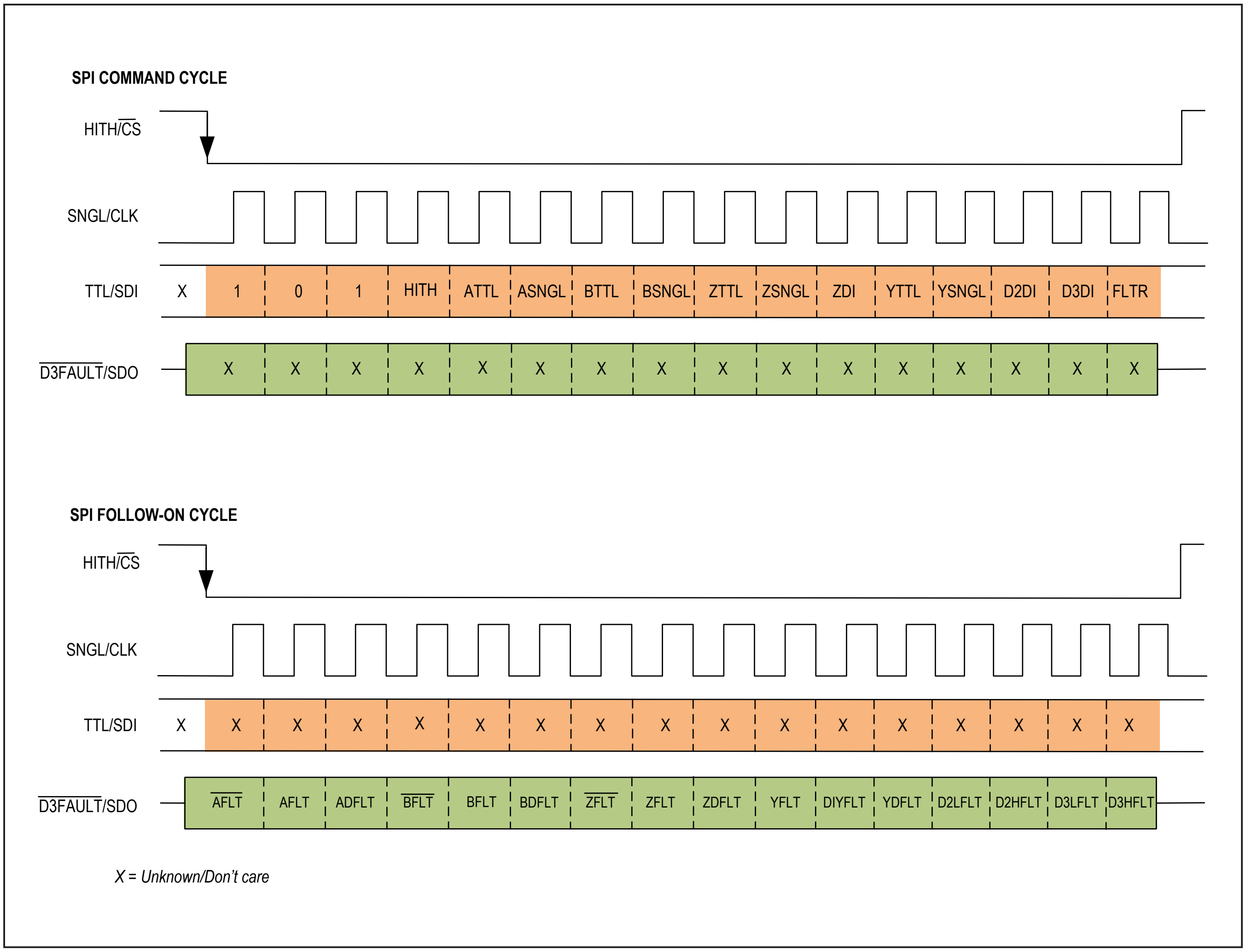


Figure 9. Change Configuration with Detailed Fault Readback SPI Command

Fault and Receiver Status Command (CMD[2:0] = 010)

Write 010 to bits CMD[2:0] to read the fault and receiver output status (Figure 10). The fault and receiver status is latched at the high-to-low transition on HITH/$\overline{CS}$ of the following SPI cycle and is output on that SPI cycle. The _FAULT bits are set when a differential or single-ended fault occurs on a receiver. See the *Fault Diagnostics* section for more information.

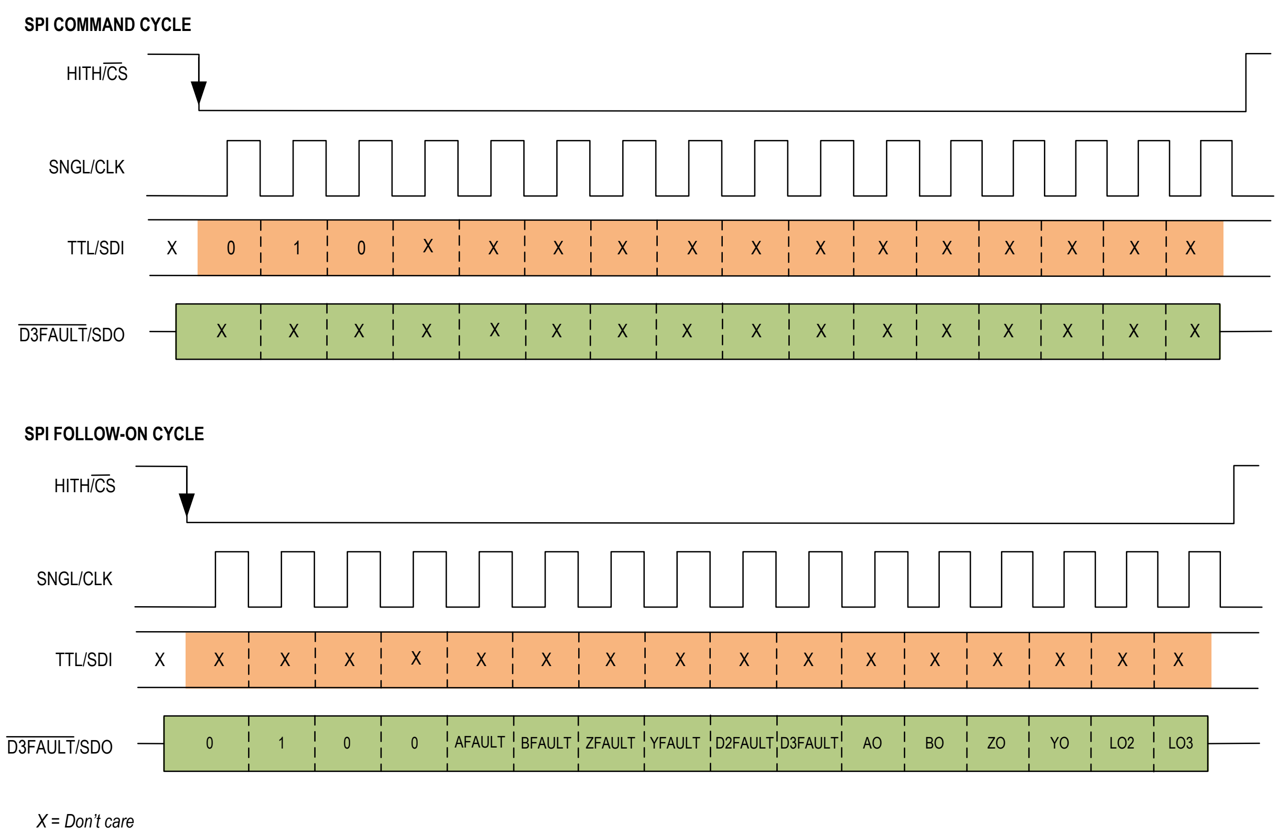


Figure 10. Current Fault and Receiver Status Readback SPI Command

Readback Current Receiver Command (CMD[2:0] = 111)

Write 111 to bits CMD[2:0] to read the current receiver configuration (Figure 11). See Table 11 thru Table 14 for more information.

Fault Filtering

In SPI mode, the interrupt output (D3FAULT/IRQ) asserts when a fault is detected on any receiver. D3FAULT/IRQ and the receiver's _FAULT output assert 1ms (typ) after the fault is detected.

The 1ms filter is always active for single-ended faults, but can be enabled or disabled for differential faults. Set the global configuration filter bit, FLTR, to 1 to enable the fault filter for differential (_DFLT) faults.

Set FLTR = 0 to disable the filter. D3FAULT/IRQ and _FAULT assert 10μs (typ) after the fault is detected when the filter is disabled.

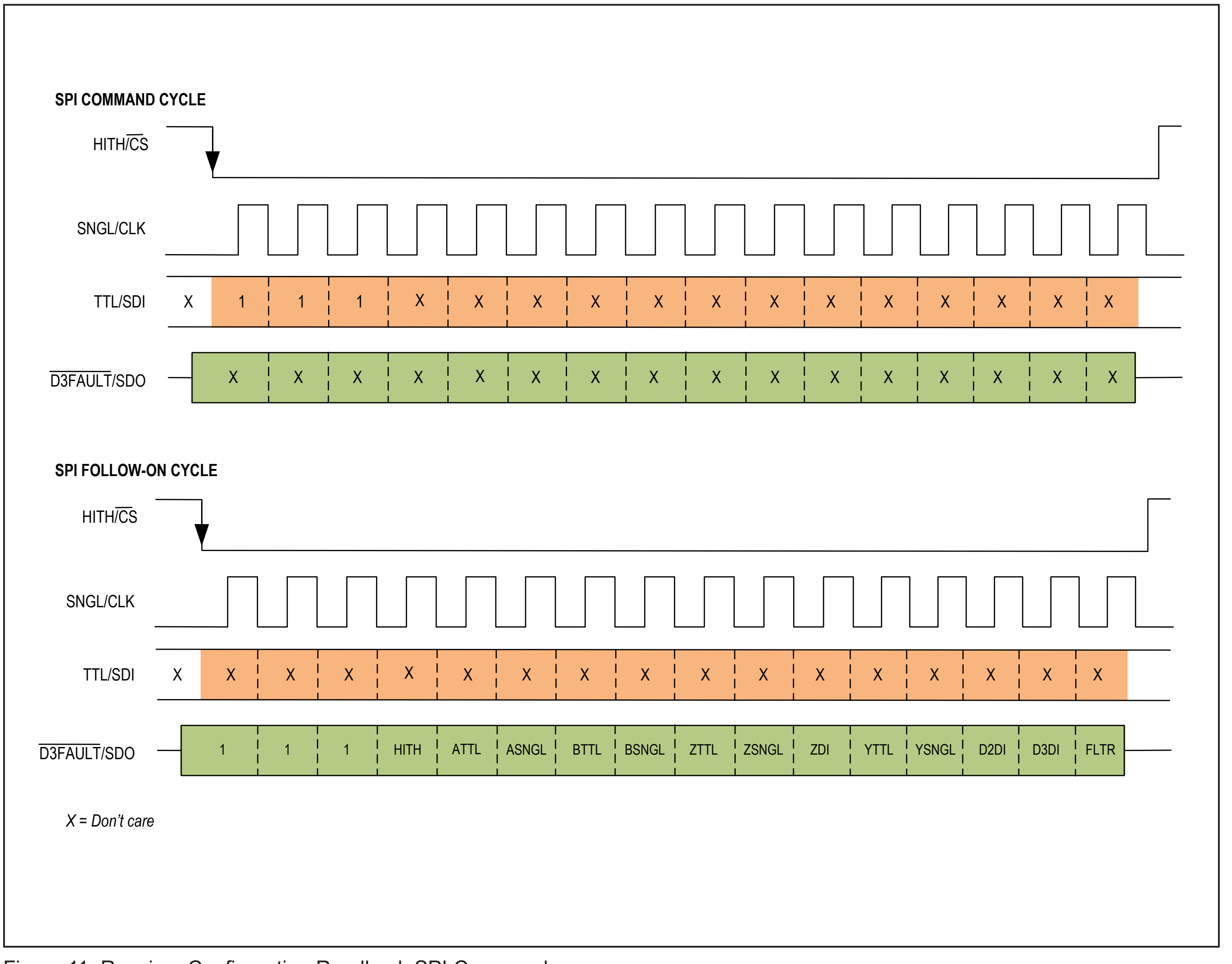


Figure 11. Receiver Configuration Readback SPI Command

Table 11. SPI Mode RxA, RxB Selection Bits

_SNGL	_TTL	RxA, RxB RECEIVER OPERATION
0	0	D-HTL
0	1	RS-422
1	0	SE-HTL
1	1	TTL

Table 12. SPI Mode RxZ Selection Bits

ZTTL	ZSNGL	ZDI	RxZ RECEIVER OPERATION
0	0	0	D-HTL
0	1	0	SE-HTL
1	0	0	RS-422
1	1	0	TTL
X	X	1	DI

X = Don't care

Table 13. SPI Mode RxY Selection Bits

YTTL	YSNGL	RxY RECEIVER OPERATION
0	0	RS-422
0	1	DI
1	0	RS-422
1	1	TTL

Table 14. SPI Mode RxD2, RxD3 Selection Bits

D_DI	RxD2, RxD3 RECEIVER OPERATION
0	TTL
1	DI

Fault Diagnostics

In SPI mode, the interrupt output ($\overline{\text{D3FAULT/IRQ}}$) and associated _$\overline{\text{FAULT}}$ output asserts when a fault is detected on any receiver. _$\overline{\text{FAULT}}$ deasserts when the fault is removed, but $\overline{\text{D3FAULT/IRQ}}$ remains latched until the fault status is read through the SPI interface.

If the fault is not cleared, $\overline{\text{D3FAULT/IRQ}}$ deasserts after the SPI read command, but the associated fault bit and _$\overline{\text{FAULT}}$ output remain asserted.

Applications Information

Cable Termination

Transmission line termination is required for RS-422, HTL, and TTL high-speed signals on long cables. For RS-422 and TTL signal levels, 120Ω termination is commonly used to match the characteristic impedance of the cable. For HTL signals, 270Ω/100pF AC-termination with a series RC can be applied to reduce power dissipation.

Figure 12 shows a sample circuit of a termination scheme to suit all of these operating modes. The 270Ω termination can be permanently left in for all operating modes. For high-speed RS-422 and TTL signals, the cable should be terminated by its characteristic impedance to reduce reflections. This can be done by switching in the parallel resistor in these modes using a beyond-the-rails switch like the MAX14777.

Surge Protection

The A, $\overline{A}$, B, $\overline{B}$, Z, $\overline{Z}$, DIY, $\overline{Y}$, DI2, and DI3 inputs are IEC61000-4-2 ESD protected against ±7kV air gap and ±10kV contact discharge strikes. For surge protection, an external voltage limiting element, like a TVS diode, is required. Select a diode with peak clamping voltage under 55V. Examples of suitable TVS diodes to protect against ±1kV/42Ω, 8μs/20μs surges are the SMAJ30CA and PDFN3-32.

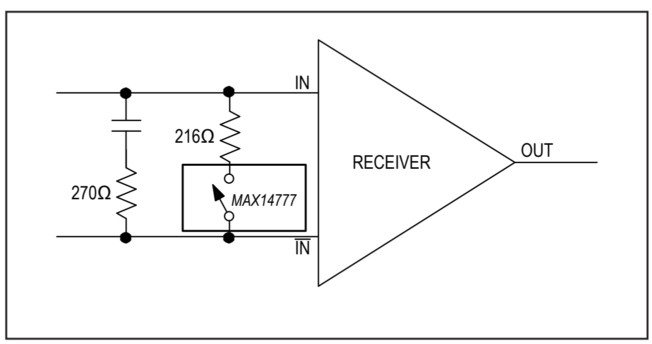


Figure 12. Sample Termination Scheme for HTL, RS-422, and TTL modes

Table 15. Detailed Fault Readback Bit Status

BIT	NAME	DESCRIPTION
15	$\overline{AFLT}$	0 = No fault asserted. 1 = Single-ended fault on $\overline{A}$ detected by the RxA receiver.
14	AFLT	0 = No fault asserted. 1 = Single-ended fault on A detected by the RxA receiver.
13	ADFLT	0 = No fault asserted. 1 = Differential fault detected on RxA.
12	$\overline{BFLT}$	0 = No fault asserted. 1 = Single-ended fault on $\overline{B}$ detected by the RxB receiver.
11	BFLT	0 = No fault asserted. 1 = Single-ended fault on B detected by the RxB receiver.
10	BDFLT	0 = No fault asserted. 1 = Differential fault detected on RxB.
9	$\overline{ZFLT}$	0 = No fault asserted. 1 = Single-ended fault on $\overline{Z}$ detected by the RxZ receiver.
8	ZFLT	0 = No fault asserted. 1 = Single-ended fault on Z detected by the RxZ receiver.
7	ZDFLT	0 = No fault asserted. 1 = Differential fault detected on RxZ.
6	$\overline{YFLT}$	0 = No fault asserted. 1 = Single-ended fault on $\overline{Y}$ detected by the RxY receiver.
5	DIYFLT	0 = No fault asserted. 1 = Single-ended fault on DIY detected by the RxY receiver.
4	YDFLT	0 = No fault asserted. 1 = Differential fault detected on RxY.
3	D2LFLT	0 = No fault asserted. 1 = Single-ended low-voltage fault on DI2 detected by the RxD2 receiver.
2	D2HFLT	0 = No fault asserted. 1 = Single-ended high-voltage fault on DI2 detected by the RxD2 receiver. Only in TTL mode.
1	D3LFLT	0 = No fault asserted. 1 = Single-ended low-voltage fault on DI3 detected by the RxD3 receiver.
0	D3HFLT	0 = No fault asserted. 1 = Single-ended high-voltage fault on DI3 detected by the RxD3 receiver. Only in TTL mode.

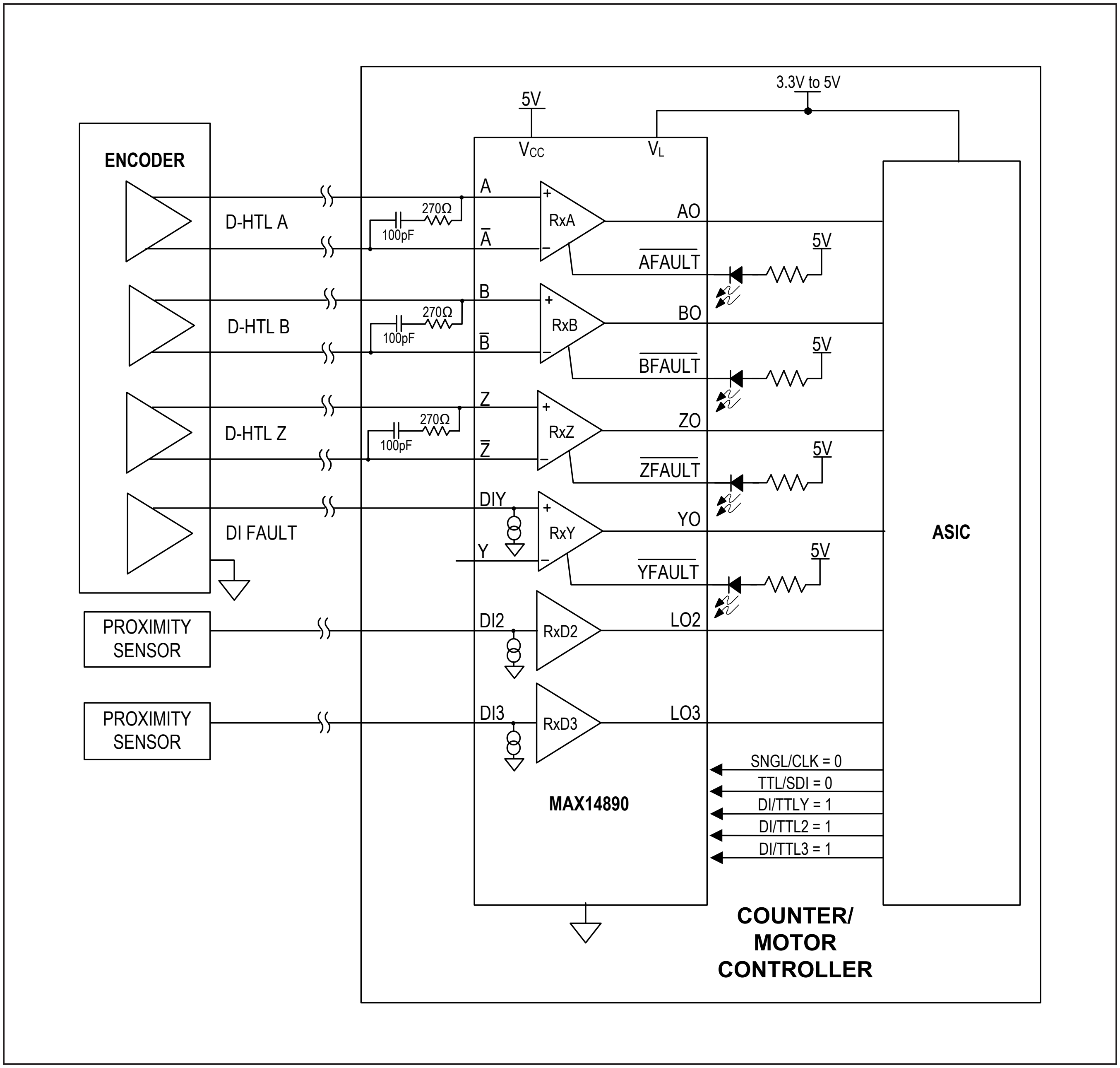


Figure 13. Encoder Circuit with Differential HTL (D-HTL) Signals and DI Alarm Signal

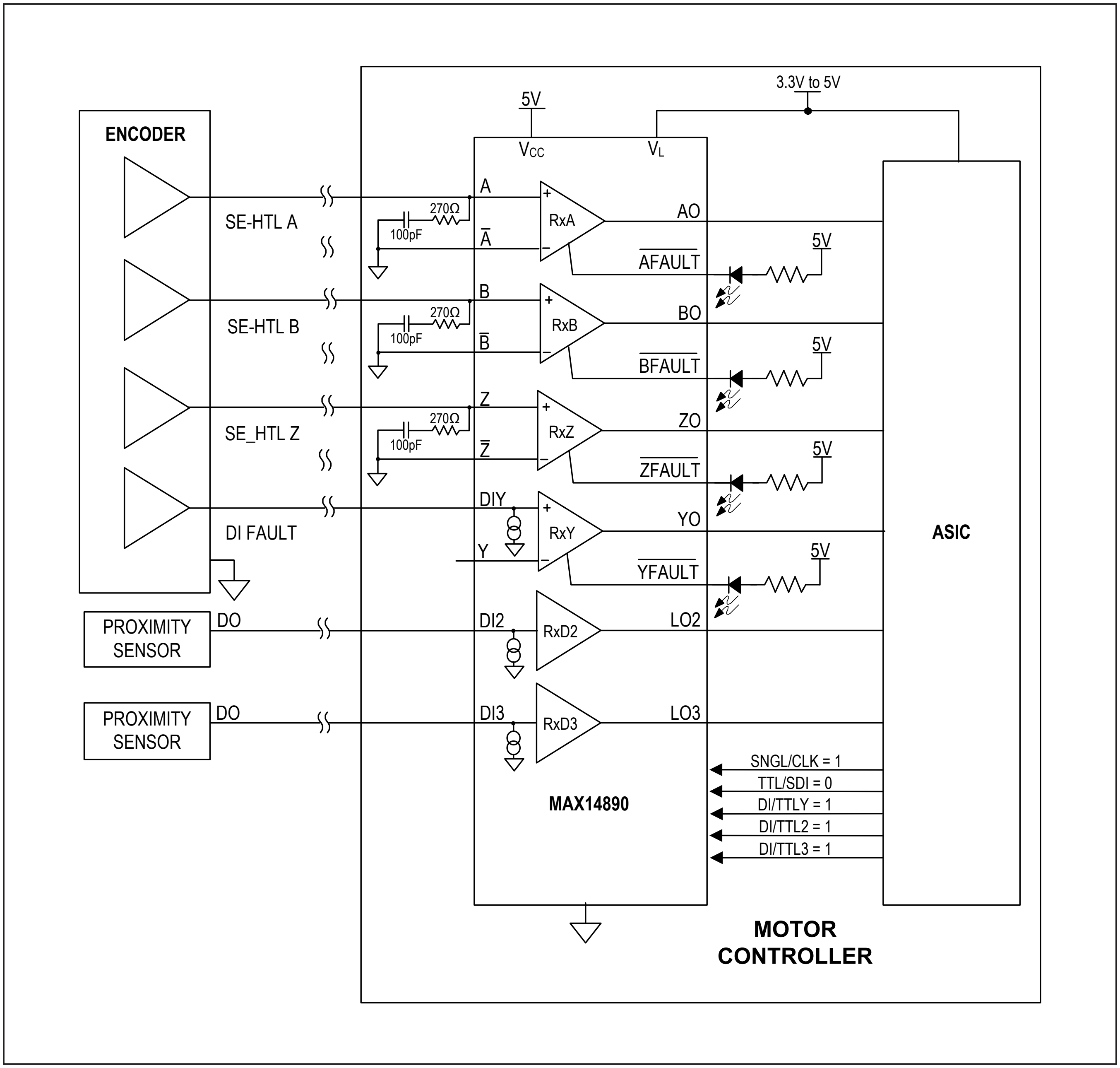


Figure 14. Encoder Circuit with Single-Ended HTL (SE-HTL) Signals and DI Alarm Signal

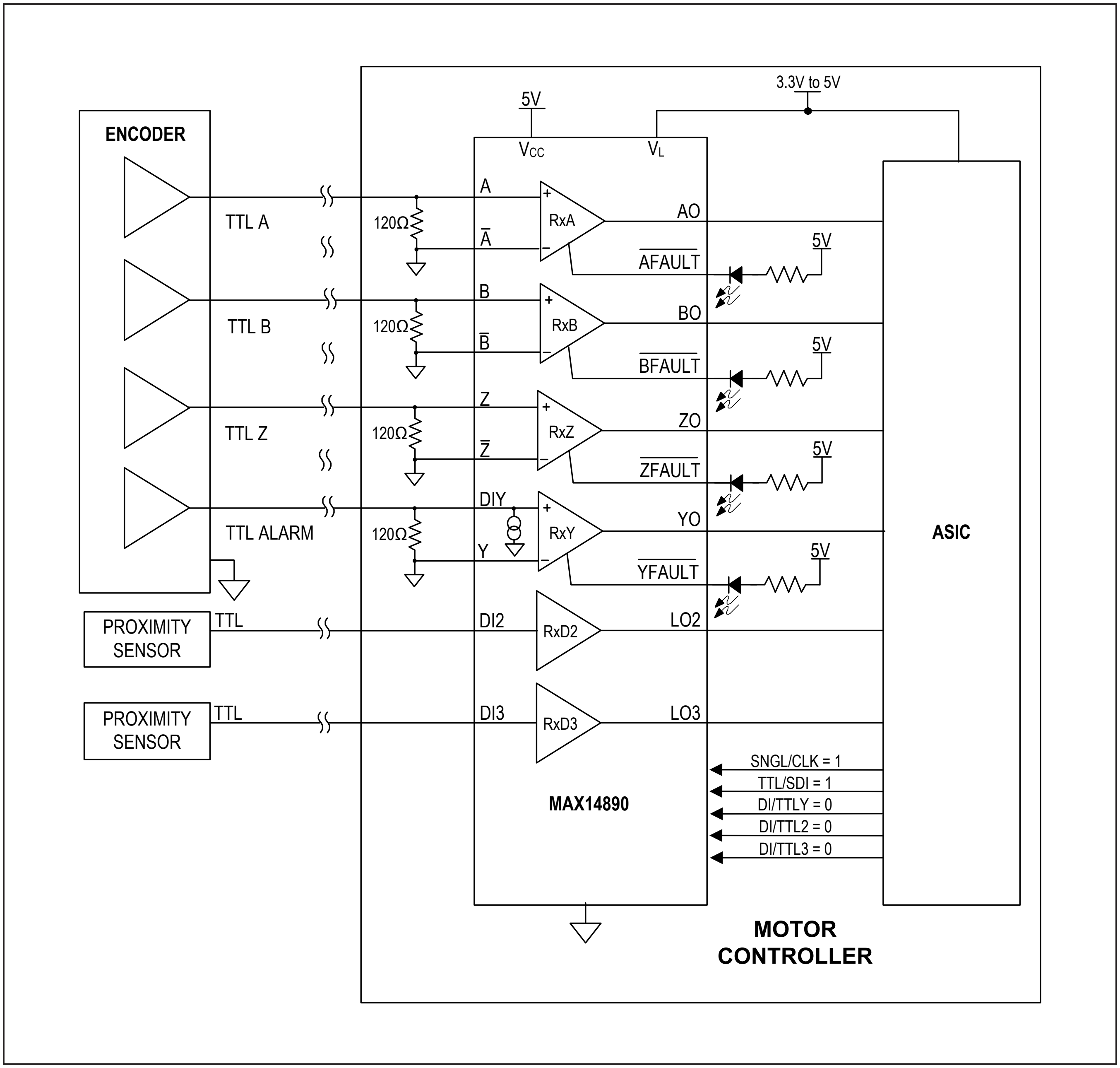
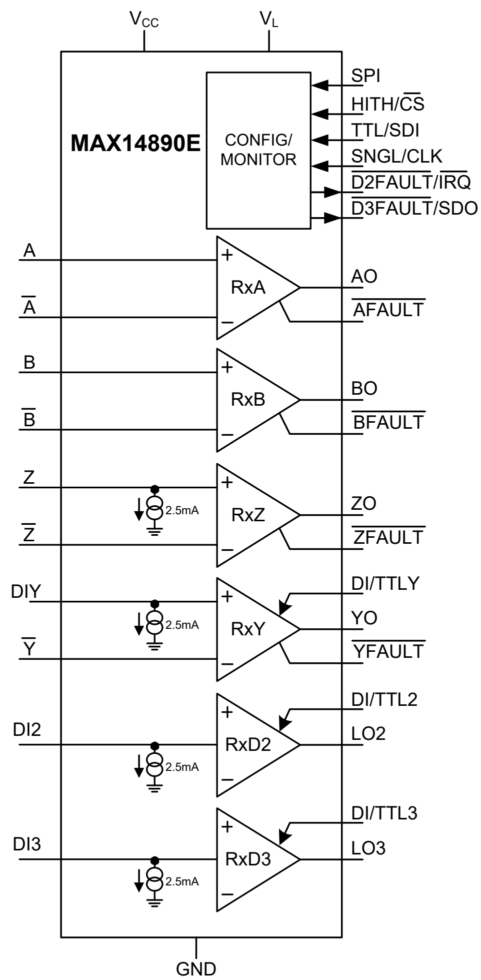


Figure 15. Encoder Circuit with TTL Signals and DI Alarm Signal

Functional Diagram



Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX14890EATJ+	-40°C to +125°C	32 TQFN *EP
MAX14890EATJ+T	-40°C to +125°C	32 TQFN *EP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	11/19	Added the *Surge Protection* section	24
2	5/20	Updated the *Benefits and Features, Switching Characteristics,* and *Pin Description* sections	1, 5–6, 14

