DS28E40 Deep Cover Automotive 1-Wire Authenticator

General Description

The DS28E40 is a secure authenticator that provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware-implemented cryptographic engines, the device integrates a FIPS/NIST True Random Number Generator (TRNG), 6Kb of One-Time Programmable (OTP) memory for user data, keys and certificates, one configurable General-Purpose Input/Output (GPIO), and a unique 64-bit ROM identification number (ROM ID).

The ECC public/private key capabilities operate from the NIST-defined P-256 curve and include FIPS 186 compliant ECDSA signature generation and verification to support a bidirectional asymmetric key authentication model. The SHA-256 secret-key capabilities are compliant with FIPS 180 and are usable flexibly either in conjunction with ECDSA operations or independently for multiple Hash-Based Message Authentication Code (HMAC) functions.

The GPIO pin is operated under command control and is configurable enabling support of authenticated and non-authenticated operation. The GPIO-authenticated operation supports ECDSA-based crypto-robust mode, enabling secure-boot of a host processor.

DeepCover embedded security solutions cloak sensitive data under multiple layers of advanced security to provide the most secure key storage possible. To protect against device-level security attacks, including invasive and non-invasive methods, countermeasures include active die shield, encrypted storage of keys, and algorithmic methods.

Applications

- Automotive Secure Authentication
- Identification and Calibration Automotive Parts/Tools/Accessories
- IoT Node Crypto-Protection
- Accessory and Peripheral Secure Authentication
- Secure Storage of Cryptographic Keys for a Host Controller
- Secure Boot or Download of Firmware and/or System Parameters

Benefits and Features

- ECC-P256 Compute Engine
  - FIPS 186 ECDSA P256 Signature and Verification
  - ECDH Key Exchange for Session Key Establishment
  - ECDSA Authenticated R/W of Configurable Memory
- SHA-256 Compute Engine
  - FIPS 198 HMAC for Bidirectional Authentication
- SHA-256 One-Time Pad Encrypted R/W of Configurable Memory Through ECDH Established Key
- One GPIO Pin with Optional Authentication Control
  - Open-Drain, 4mA/0.4V
  - Optional SHA-256 or ECDSA Authenticated On/Off and State Read
  - Optional ECDSA Certificate Verification to Set On/Off after Multiblock Hash for Secure Boot
- TRNG with NIST SP 800-90B Compliant Entropy Source with Function to Read Out
- Optional Chip-Generated Pr/Pu Key Pairs for ECC Operations
- 6Kb of One-Time Programmable (OTP) for User Data, Keys, and Certificates
- Unique and Unalterable Factory-Programmed 64-Bit Identification Number (ROM ID)
  - Optional Input Data Component to Crypto and Key Operations
- Single-Contact, 1-Wire Interface Communication with Host at 9.09kbps and 62.5kbps
- 3.3V ±10%, -40°C to +125°C Operating Range
- ±8kV HBM ESD protection of 1-Wire IO Pin
- 10-Pin, 3mm x 4mm TDFN Package
- AEC-Q100 Grade 1

Request DS28E40 Security User Guide

Ordering Information appears at end of data sheet.

19-100901; Rev 0; 9/20

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Simplified Block Diagram

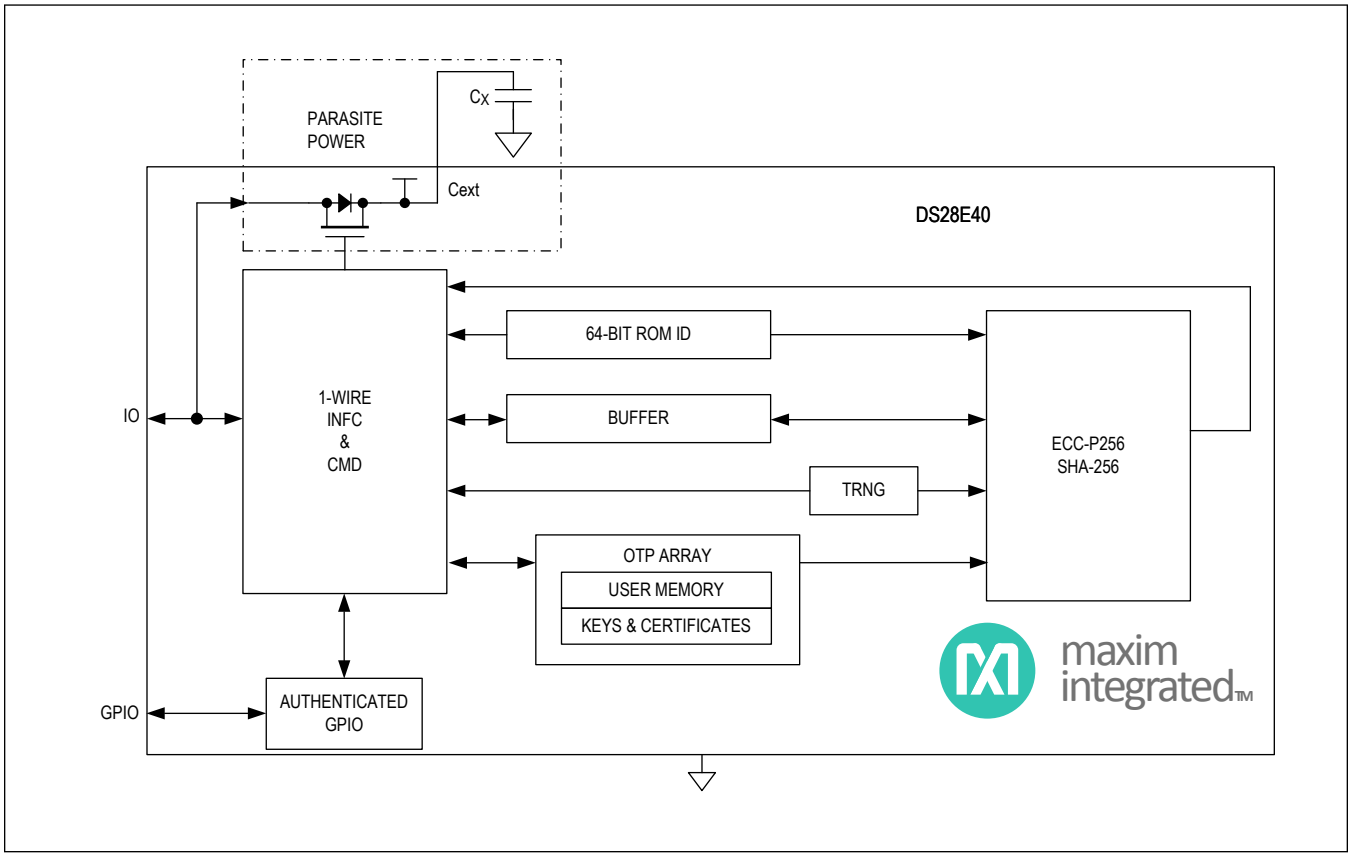


Figure 1. DS28E40 Block Diagram

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND ..... -0.5V to 4.0V
Maximum Current into Any Pin..... -20mA to 20mA
Operating Temperature Range ..... -40°C to 125°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-40°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 TDFN

Package Code	T1034+2
Outline Number	21-0268
Land Pattern Number	90-0247
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	60°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	30°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(*Note 1*)	2.97	3.3	3.63	V
1-Wire Pullup Resistance	R_{PUP}	(*Note 1*, *Note 2*)			500	Ω
Input Capacitance	C_{IO}	(*Note 3*)		0.1 + C_X		nF
Capacitor External	C_X	(*Note 1*)	1.27	1.5	1.73	µF
Input Load Current	I_L	IO pin at V_{PUP}		10	1400	µA
High-to-Low Switching Threshold	V_{TL}	(*Note 4*, *Note 5*, *Note 6*)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(*Note 4*, *Note 7*)			0.10 x V_{PUP}	V
Low-to-High Switching Threshold	V_{TH}	(*Note 4*, *Note 5*, *Note 8*)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(*Note 4*, *Note 5*, *Note 9*)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 8mA (*Note 10*)			0.6	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IO PIN: 1-Wire INTERFACE							
Recovery Time	t_{REC}	Standard speed, R_{PUP} = 1000Ω, (*Note 1*, *Note 11*, *Note 12*)		100			µs
			Directly prior to reset pulse	2000			
		Overdrive speed, R_{PUP} = 1000Ω, (*Note 1*, *Note 11*, *Note 12*)		20			
			Directly prior to reset pulse	100			
Rising-Edge Hold-Off	t_{REH}	(*Note 4*, *Note 13*)	Applies to standard speed only		1		µs
Time Slot Duration	t_{SLOT}	(*Note 1*, *Note 14*)	Standard speed	160			µs
			Overdrive speed	26			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE							
Reset Low Time	t_{RSTL}	(*Note 1*)	Standard speed	480		640	µs
			Overdrive speed	48		80	
Reset High Time	t_{RSTH}	(*Note 1*)	Standard speed	480			µs
			Overdrive speed	48			
Presence Detect Fall Time	t_{FPD}	(*Note 4*, *Note 15*)	Standard speed		1.25		µs
			Overdrive speed		0.15		
Presence-Detect Sample Time	t_{MSP}	(*Note 1*, *Note 16*)	Standard speed	65		75	µs
			Overdrive speed	7		10	
IO PIN: 1-Wire WRITE							
Write-Zero Low Time	t_{W0L}	(*Note 1*, *Note 17*)	Standard speed	60		120	µs
			Overdrive speed	6		15.5	
Write-One Low Time	t_{W1L}	(*Note 1*, *Note 17*)	Standard speed	0.25		15	µs
			Overdrive speed	0.25		2	
IO PIN: 1-Wire READ							
Read Low Time	t_{RL}	(*Note 1*, *Note 18*)	Standard speed	0.25		15 - δ	µs
			Overdrive speed	0.25		2 - δ	
Read Sample Time	t_{MSR}	(*Note 1*, *Note 18*)	Standard speed	t_{RL} + δ		15	µs
			Overdrive speed	t_{RL} + δ		2	
GPIO PIN							
GPIO Output Low	$PIOV_{OL}$	$PIOI_{OL}$ = 4mA (*Note 10*)				0.4	V
GPIO Input Low	$PIOV_{IL}$			-0.3		0.3 x V_{PUP}	V
GPIO Master Sample	$PIOV_{IH}$			0.70 x V_{PUP}		V_{PUP} + 0.3	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPIO Switching Hysteresis	$PIOV_{HY}$			0.3		V
GPIO Leakage Current	$PIOI_L$		-1		+1	µA
STRONG PULLUP OPERATION						
Strong Pullup Voltage	V_{SPU}	(*Note 19*)	2.8			V
Strong Pullup Current	I_{SPU}	(*Note 19*)		9	16	mA
Read Memory	t_{RM}				2	ms
Write Memory	t_{WM}				150	ms
Write State	t_{WS}				15	ms
Computation Time (HMAC)	t_{CMP}				4	ms
Generate ECC Key Pair	t_{GKP}				500	ms
Generate ECDSA Signature	t_{GES}				50	ms
Verify ECDSA Signature or Compute ECDH Time	t_{VES}				160	ms
TRNG Generation	t_{RNG}				50	ms
TRNG On-Demand Check	t_{ODC}				50	ms
OTP						
OTP Write Temperature	T_{OPTW}		0		50	ºC
Data Retention	t_{DR}	T_A = +125°C (*Note 20*)	10			Years

Note 1: System requirement.

Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

Note 3: Value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication. Typically, during normal communication, the internal parasite capacitance is effectively ~100pF.

Note 4: Guaranteed by design and/or characterization only. Not production tested.

Note 5: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 6: Voltage below which, during a falling edge on IO, a logic-zero is detected.

Note 7: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic-zero level.

Note 8: Voltage above which, during a rising edge on IO, a logic-one is detected.

Note 9: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.

Note 10: The I-V characteristic is linear for voltages less than 1V.

Note 11: Applies to a single device attached to a 1-Wire line.

Note 12: t_{REC} min covers operation at worst-case temperature V_{PUP}, R_{PUP}, C_X, t_{RSTL}, t_{WOL}, and t_{RL}. t_{RECMIN} can be significantly reduced under less extreme conditions. Contact the factory for more information.

Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.

Note 14: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.

Note 15: Time from $V_{(IO)}$ = 80% of V_{PUP} and $V_{(IO)}$ = 20% of V_{PUP} at the negative edge on IO at the beginning of the presence detect pulse.

Note 16: Interval after t_{RSTL} during which a bus master can read a logic 0 on IO if there is a DS28E40 present. The power-up presence detect pulse could be outside this interval but will be complete within 2ms after power-up. 1-Wire communication should not take place for at least 2ms after V_{PUP} reaches V_{PUP} min.

Note 17: ε in Figure 5 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}.

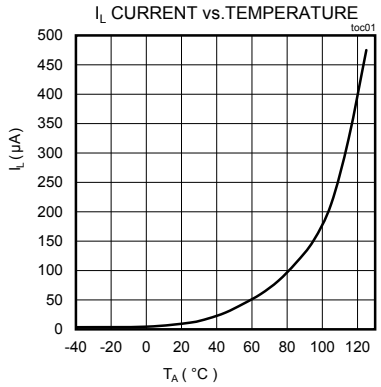
Note 18: δ in Figure 5 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master.

Note 19: I_{SPU} is the current drawn from IO during a strong pullup (SPU) operation. The pullup circuit on IO during the SPU operation should be such that the voltage at IO is greater than or equal to V_{SPUMIN}. A low-impedance bypass of R_{PUP} activated during the SPU operation is the recommended way to meet this requirement.

Note 20: Data retention is tested in compliance with JESD47G.

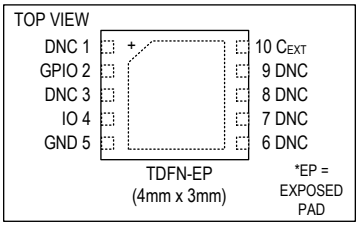
Typical Operating Characteristics

(V_{PUP} = +3.3V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)



Pin Configuration

10 TDFN



Pin Description

PIN	NAME	FUNCTION
1, 3, 6 - 9	DNC	Do Not Connect
2	GPIO	General-Purpose IO
4	IO	1-Wire IO
5	GND	Ground
10	C_{EXT}	Input for External Capacitor
—	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation. Refer to *Application Note 3273*: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS28E40 secure authenticator for automotive applications provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware-implemented cryptographic engines, the DS28E40 integrates a FIPS/NIST true random number generator (TRNG), 6Kb of secured OTP memory (3Kb User, 3Kb Keys/Secrets), one configurable GPIO pin, and a unique 64-bit ROM identification number (ROM ID).

Function Commands

After a 1-Wire reset/presence cycle and ROM function command sequence is successful, a command start can be accepted and then followed by a device function command. In general, these commands follow the state flow diagram (Figure 2). Within this diagram, the data transfer is verified when writing and reading by a CRC of 16-bit type (CRC-16). The CRC-16 is computed as described in *Application Note 27*: *Understanding and Using Cyclic Redundancy Checks with Maxim 1-Wire and iButton Products*.

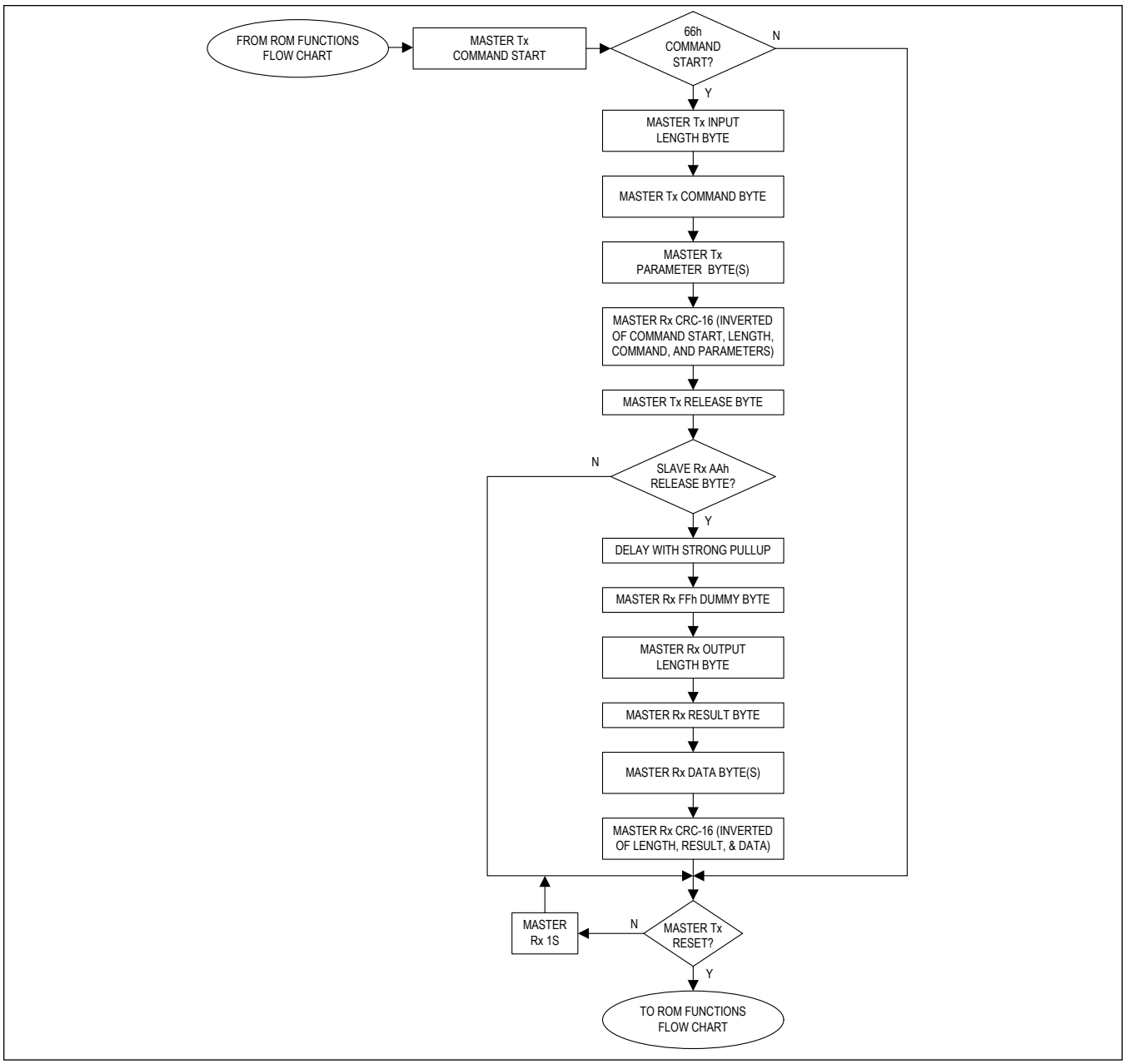


Figure 2. Device Function Flow Chart

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS28E40 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master.

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E40 is open drain with an internal circuit equivalent.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The DS28E40 supports both a standard and overdrive communication speed of 9.09kbps (max) and 62.5kbps (max), respectively. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E40 requires a pullup resistor of 1kΩ (max) at any speed.

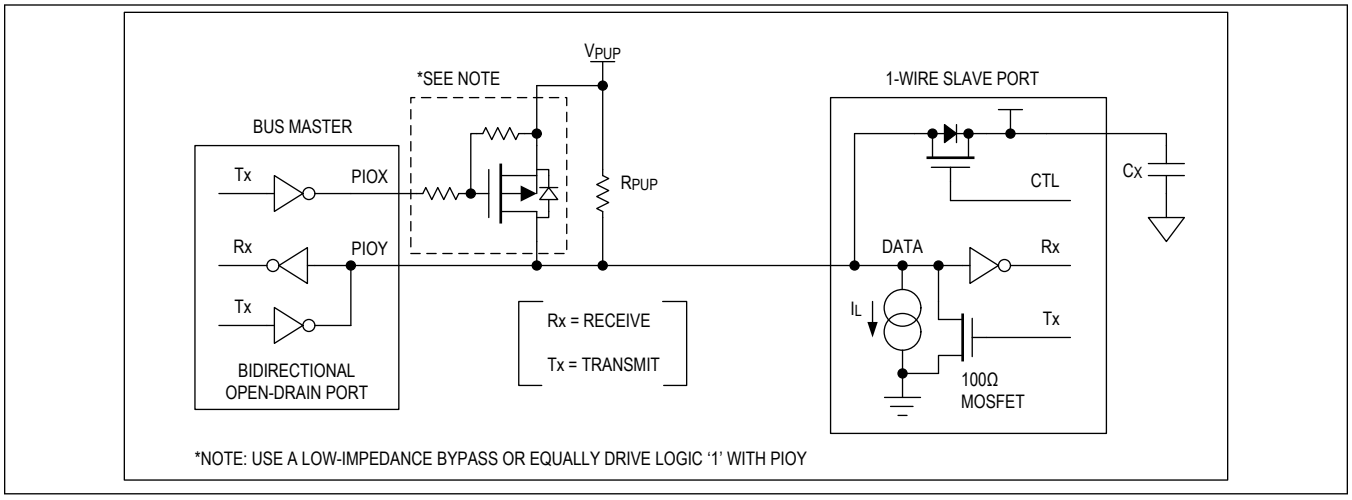


Figure 3. Hardware Configuration

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (overdrive speed) or more than 120µs (standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E40 through the 1-Wire port is as follows:

- Initialization
- ROM Function command
- Device Function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS28E40 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling and Timing* section.

1-Wire Signaling and Timing

The 1-Wire protocol consists of four types of signaling on one line: reset cycle with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the 1-Wire master initiates all falling edges. The 1-Wire master can communicate at two speeds: standard and overdrive. While in overdrive mode, the fast timing applies to all wave forms.

Figure 4 shows the initialization sequence required to begin any communication. A reset pulse followed by a presence pulse indicates that a slave is ready to receive data, given the correct ROM and device function command.

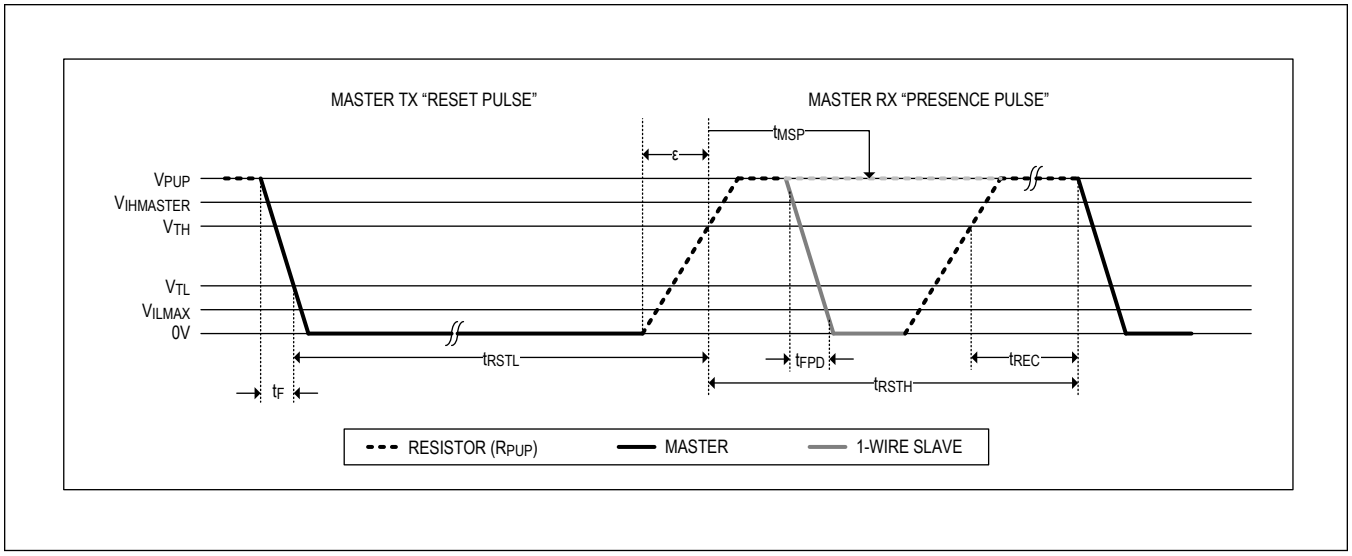


Figure 4. 1-Wire Reset/Presence-Detect Cycle

Read/Write Time Slots

Data communication on the 1-Wire bus takes place in time slots that carry a single bit each. Write time slots transport data from the 1-Wire master to a connected slave. Read time slots transfer data from slave to the 1-Wire master. Figure 5 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the slave starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window required by the slave. After the V_{TH} threshold has been crossed, the DS28E40 needs a recovery time t_{REC} before it is ready for the next time slot.

Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL}(read low time) is expired. During the t_{RL} window, when responding with a 0, the slave starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the slave does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over. Note that the slave t_{RL} during a logic 1 is adequately an approximation of the 1-Wire master t_{W1L} setting.

The slave t_{RL} plus the bus rise time on the near end and the internal timing generator of the slave on the far end define the 1-Wire master sampling window, in which the 1-Wire master performs a read from the data line. After reading from the data line, the 1-Wire master waits until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the slave to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single slave attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

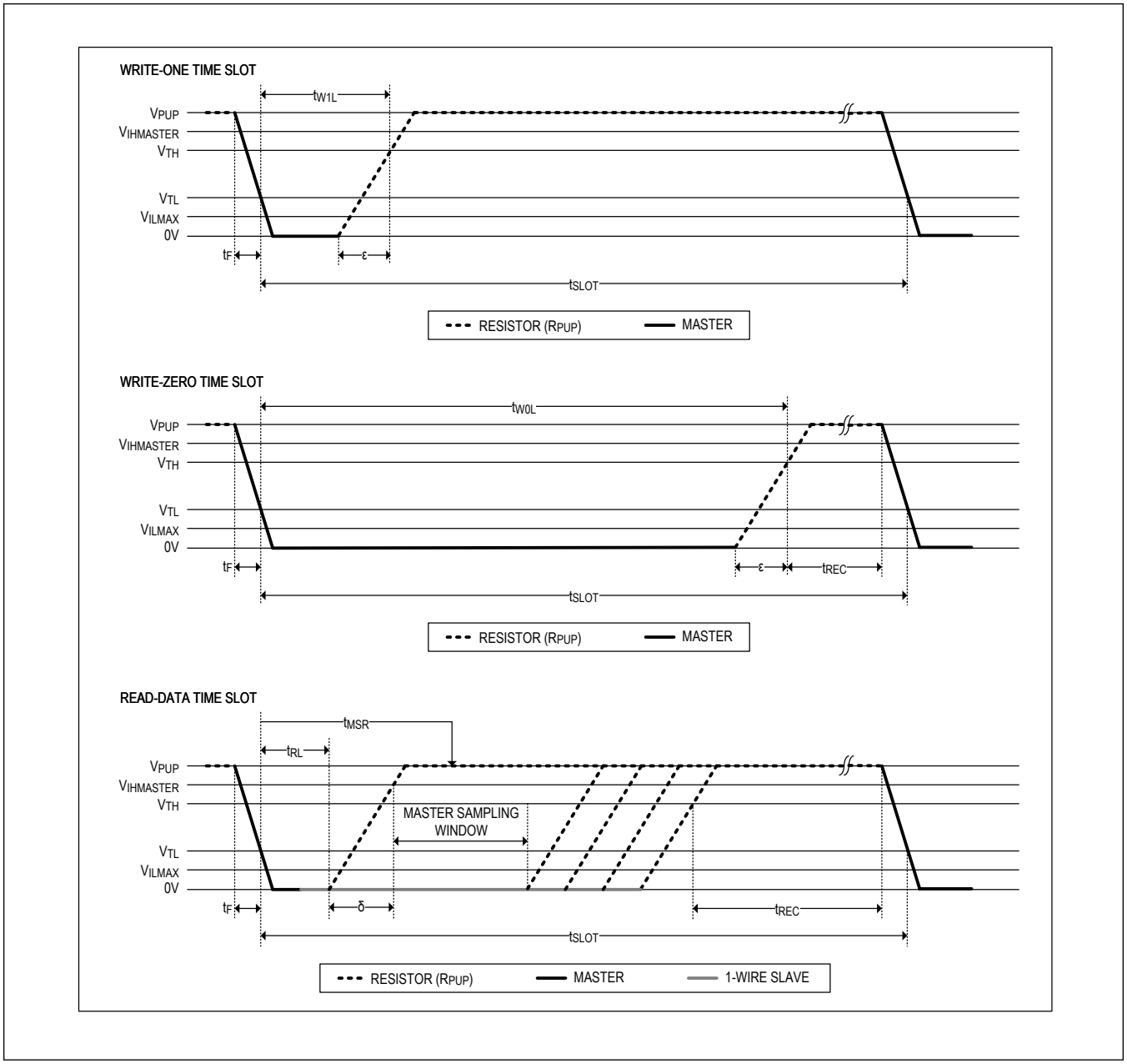


Figure 5. 1-Wire Read/Write Timing Diagrams

1-Wire ROM Commands

Once the bus master has detected a presence, it can issue one of the seven ROM function commands that the DS28E40 supports. All ROM function commands are 8 bits long. For operational details, see the flowchart description in Figure 6 and Figure 7. A descriptive list of these ROM function commands follows in the subsequent sections.

Table 1. 1-Wire ROM Commands Summary

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Search ROM	F0h	Search for a device

Table 1. 1-Wire ROM Commands Summary (continued)

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Read ROM	33h	Read ROM from device (single drop)
Match ROM	55h	Select a device by ROM number
Skip ROM	CCh	Select only device on 1-Wire
Resume	A5h	Select device with RC bit set
Overdrive Skip ROM	3Ch	Put all devices in overdrive
Overdrive Match ROM	69h	Put the device with the ROM in overdrive

Read ROM[33h]

The Read ROM command allows the bus master to read the DS28E40's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM[55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS28E40 on a multidrop bus. Only the DS28E40 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. All other slaves wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Search ROM[F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the ID of all slave devices. For each bit in the ID number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its ID number bit. On the second slot, each slave device participating in the search outputs the complemented value of its ID number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the search tree. After one complete pass, the bus master knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to *Application Note 187*: *1-Wire Search Algorithm* for a detailed discussion, including an example.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus master to access the device functions without providing the 64-bit ROM ID. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the device function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus, this command can save time by allowing the bus master to access the device functions without

providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E40 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued, followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired- AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus master to address a specific DS28E40 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E40 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. Slaves already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable slaves return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

ROM Command Flow

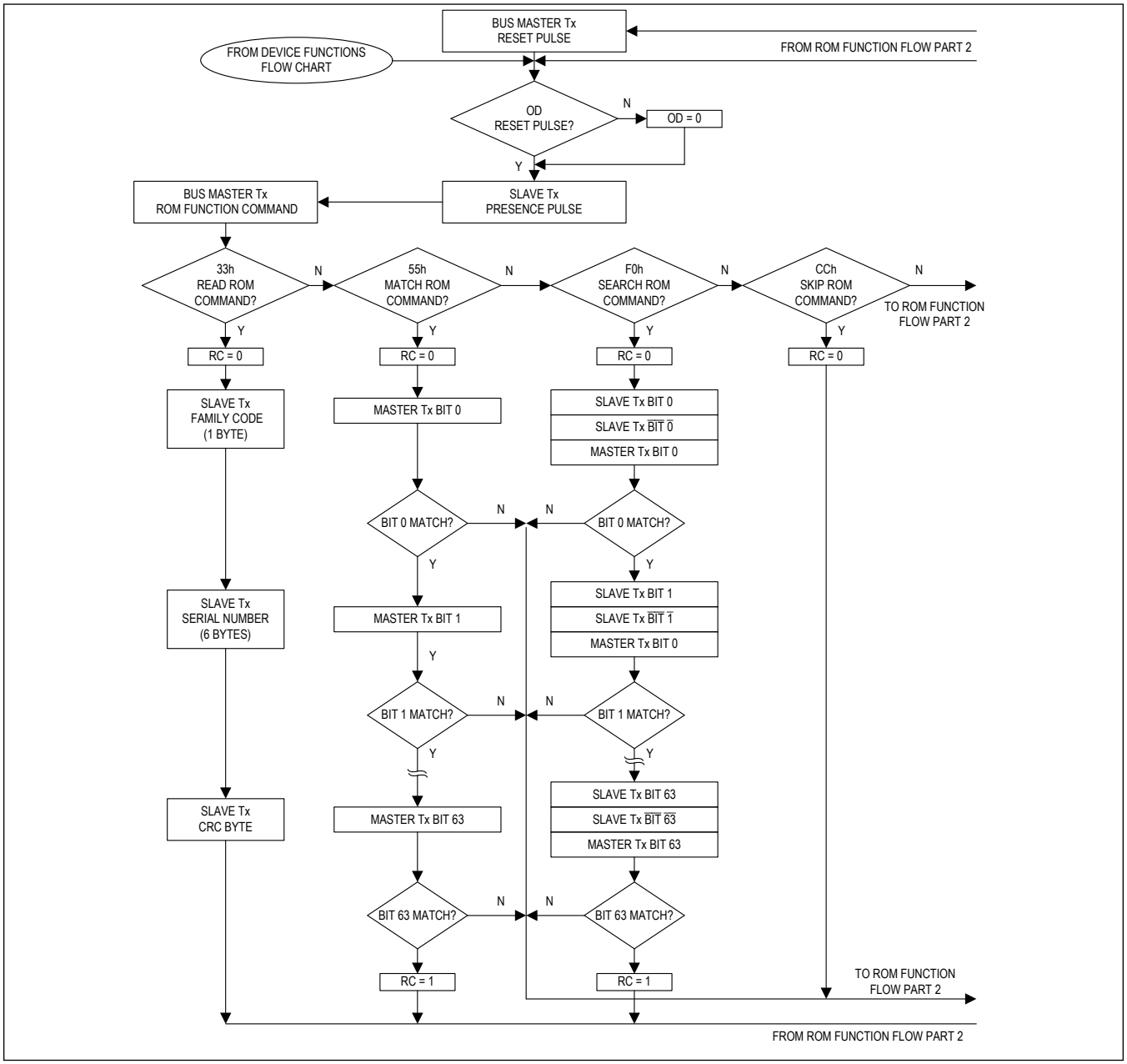


Figure 6. ROM Function Flow (Part 1)

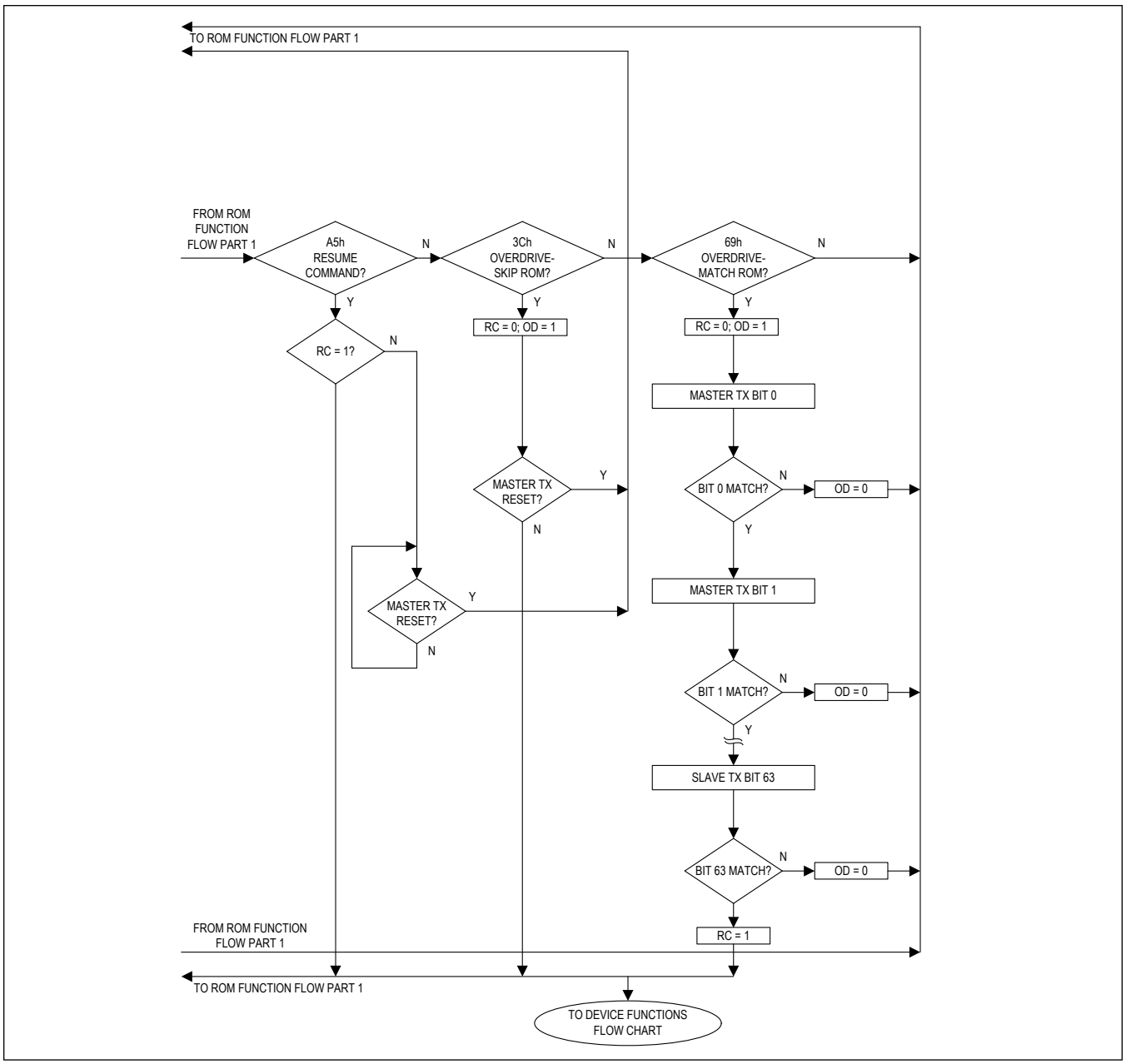


Figure 7. ROM Function (Part 2)

Improved Network Behavior

In a 1-Wire environment, line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E40 uses

a 1-Wire front end that is less sensitive to noise. The IO 1-Wire front end has hysteresis and a rising edge hold-off delay.

- On the low-to-high transition, if the line rises above V_{TH} but does not go below V_{TL}, the glitch is filtered (Figure 8, Case A.)
- The rising edge hold-off delay (nominally 100ns), t_{REH}, filters glitches that go below V_{TL} before t_{REH} has expired (Figure 8, Case B.) Effectively, the device does not see the initial rise, and the t_{REH} delay resets when the line goes below V_{TL}.
- If the line goes below V_{TL} after t_{REH} has expired, the glitch is not filtered and is taken as the beginning of a new time slot (Figure 8, Case C.)

Independent of the time slot, the falling edge of the presence pulse has a controlled slew rate to reduce ringing. The falling delay is specified by t_{FPD}.

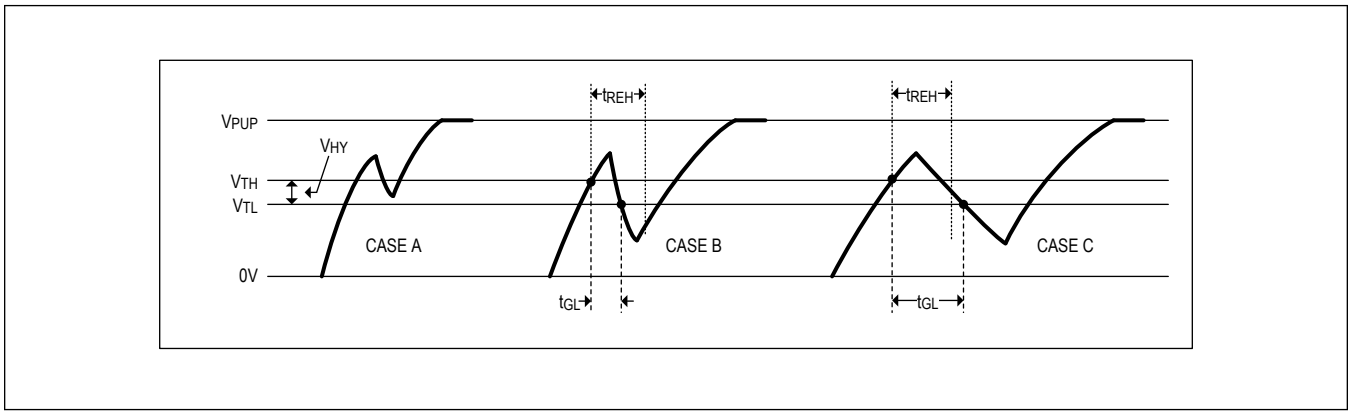


Figure 8. Noise Suppression Scheme

Typical Application Circuit

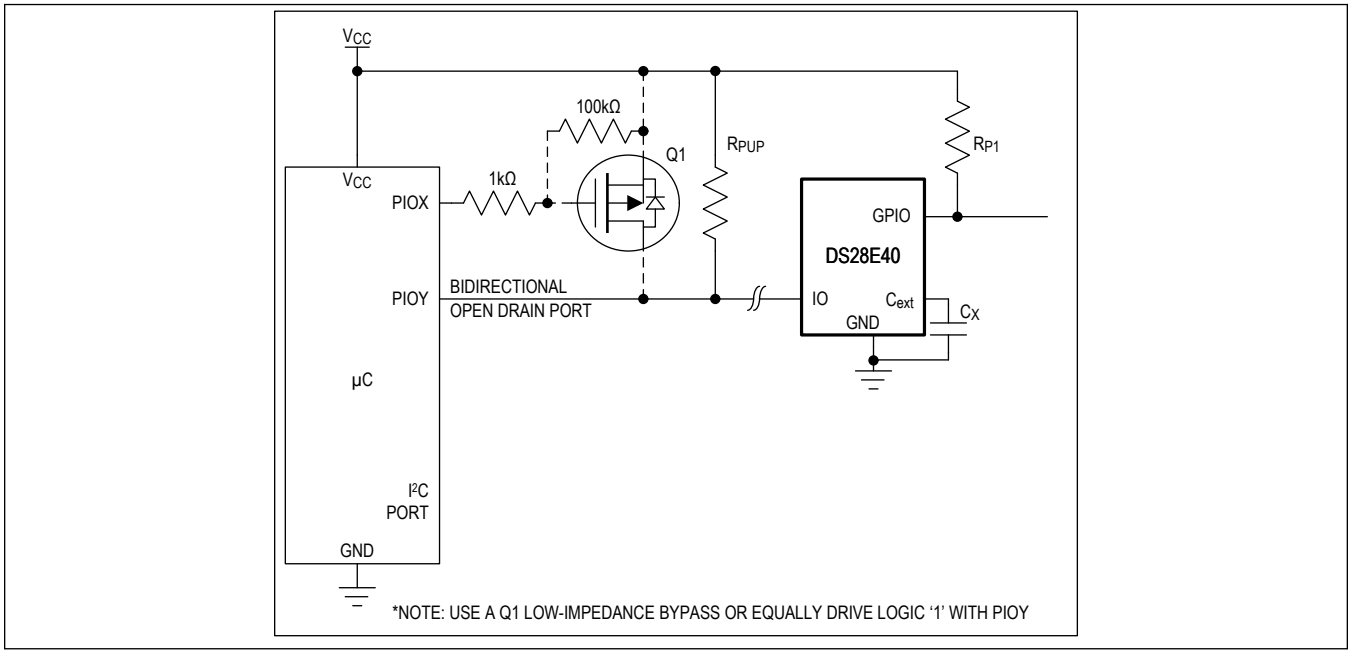


Figure 9. DS28E40 Typical Application Circuit

Ordering Information

Part Number	Temp Range	Pin-Package
DS28E40G/V+T	-40°C to +125°C	10 TDFN T1034+2 (2.5k pcs reel)

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V = Denotes an automotive qualified part.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/20	Initial release	—