

General Description

Maxim's redesigned DG444/DG445 analog switches now feature on-resistance matching (4Ω max) between switches and guaranteed on-resistance flatness over the signal range (9Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection (10pC max), low power consumption (35µW max), and an electrostatic discharge (ESD) tolerance of 2000V (min) per Method 3015.7. The new design offers lower off-leakage current over temperature (less than 5nA at +85°C).

The DG444/DG445 are quad, single-pole/single-throw (SPST) analog switches. The DG444 has four normally closed switches and the DG445 has four normally open switches. Switching times are less than 250ns for ton and less than 70ns for toff. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG444/DG445 continue to be fabricated with a 44V silicon-gate process.

Applications

Sample-and-Hold Circuits Test Equipment Heads-Up Displays Guidance and Control Systems Military Radios

Communication Systems **Battery-Operated Systems** PBX. PABX **Audio Signal Routing** Modems/Faxes

New Features

- ♦ Plug-In Upgrades for Industry-Standard DG444/DG445
- ♦ Improved Ron Match Between Channels (4Ω max)
- ♦ Guaranteed R_{FLAT}(ON) Over Signal Range (9Ω max)
- ♦ Improved Charge Injection (10pC max)
- **♦ Improved Off-Leakage Current Over Temperature** (< 5nA at +85°C)
- ♦ Withstand ESD (2000V min) per Method 3015.7

Existing Features

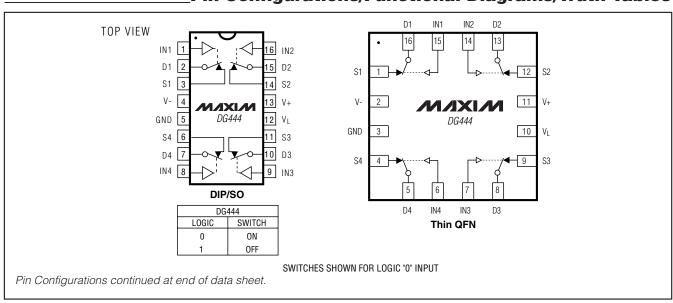
- ♦ Low RDS(ON) (85 Ω max)
- ♦ Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V
- ♦ Low Power Consumption (35µW max)
- ♦ Rail-to-Rail Signal Handling
- ♦ TTL/CMOS-Logic Compatible

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DG444CJ	0°C to +70°C	16 Plastic DIP
DG444CY	0°C to +70°C	16 Narrow SO
DG444C/D	0°C to +70°C	Dice*
DG444DJ	-40°C to +85°C	16 Plastic DIP
DG444DY	-40°C to +85°C	16 Narrow SO

Ordering Information continued at end of data sheet. *Contact factory for dice specifications.

Pin Configurations/Functional Diagrams/Truth Tables



MIXIM

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

(Voltage Referenced to V-)
V+44V
GND25V
V _L (GND - 0.3V) to (V+ + 0.3V)
Digital Inputs V _S , V _D (Note 1)(V 2V) to (V+ + 2V) or 30mA
(whichever occurs first)
Continuous Current (any terminal)30mA Peak Current, S or D (pulsed at 1ms, 10% duty cycle max).100mA

)°C)696mW
842mW
°C)2667mW
0°C to +70°C
0°C to +85°C
°C to +150°C
+300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITI	ONS	MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	Vanalog	(Note 3)	-15		+15	V		
Drain-Source	RDS(ON)	V+ = 13.5V, V- = -13.5V,	T _A = +25°C		50	85	Ω	
On-Resistance	1103(011)	$V_D = \pm 8.5 V$, $I_S = -10 \text{mA}$	$T_A = T_{MIN}$ to T_{MAX}			100	32	
On-Resistance Match	ΔRDS(ON)	$V_D = \pm 10V$,	T _A = +25°C			4	Ω	
Between Channels (Note 4)	ZINDS(ON)	$I_S = -10 \text{mA}$	$T_A = T_{MIN}$ to T_{MAX}			5	22	
	D=: .=:(0.1)	$V_D = \pm 5V$,	T _A = +25°C			9	Ω	
On-Resistance Flatness (Note 4)	nFLAT(ON)	Is = -10mA	$T_A = T_{MIN}$ to T_{MAX}			15		
Source Leakage Current	IO(OFF)	V+ = 16.5V, V- = -16.5V, $V_D = \pm 15.5V,$	T _A = +25°C	-0.50	+0.01	+0.50	nA	
(Note 5)	IS(OFF)	$V_S = \mp 15.5V$	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	IIA	
Drain Off-Leakage Current	In (oss)	V+ = 16.5V, V- = -16.5V, $V_D = \pm 15.5V,$	T _A = +25°C	-0.50	+0.01	+0.50	nA	
(Note 5)	ID(OFF)	$V_S = \pm 15.5V$	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	IIA	
Drain On-Leakage Current	I _{D(ON)}	V+ = 16.5V, V- = -16.5V, $VD = \pm 15.5V.$	T _A = +25°C	-0.50	+0.08	+0.50		
(Note 5)	or I _{S(ON)}	$V_S = \pm 15.5V$, $V_S = \pm 15.5V$	$T_A = T_{MIN}$ to T_{MAX}	-10		+10	nA	
INPUT								
Input Current with Input Voltage High	I _{INH}	$V_{IN} = 2.4V$, all others = 0	-0.5	-0.00001	+0.5	μΑ		
Input Current with Input Voltage Low	I _{INL}	$V_{IN} = 0.8V$, all others = 2	-0.5	-0.00001	+0.5	μΑ		

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued) (V+ = 15V, V- = -15V, V_L = 5V, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITI	ONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH				'			
Power-Supply Range	V+, V-		±4.5		±20.0	V	
Positive Supply Current	l+	All channels on or off, V+ = 16.5V, V- = -16.5V, V _{IN} = 0V	$T_A = +25^{\circ}C$	-1	-0.001	+1	μA
Tositive Supply Current	17	or 5V	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	μΛ
Negative Supply Current	I-	All channels on or off, $V+=$ 16.5 V , $V-=-16.5V$, $V_{IN}=0V$	T _A = +25°C	-1	-0.0001	+1	μA
Negative Supply Culterit	-	or 5V	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	μΑ
Logic Supply Current	IL	All channels on or off, V+ = 16.5V, V- = -16.5V, V _{IN} = 0V	T _A = +25°C	-1	-0.001	+1	μA
Logic Supply Current	'L	or 5V	TA = TMIN to TMAX	-5		+5	μΑ
Ground Current	lovis	All channels on or off, V+ =	T _A = +25°C	-1 -0.0001		+1	μA
Ground Current	IGND	16.5V, V- = -16.5V, V _{IN} = 0V or 5V	TA = TMIN to TMAX	-5		+5	μΑ
INPUT				•			
Turn-On Time	ton	$V_S = \pm 10V$, Figure 2	T _A = +25°C		150	250	ns
T O# Time -		DG444, V _S = ±10V, Figure 2	T _A = +25°C		90	120	ns
Turn-Off Time	toff	DG445, $V_S = \pm 10V$, Figure 2	T _A = +25°C		110	170	ns
Charge Injection (Note 3)	Q	$C_L = 1nF$, $V_{GEN} = 0$, $R_{GEN} = 0\Omega$, Figure 3	T _A = +25°C		5	10	рС
Off-Isolation Rejection Ratio (Note 6)	OIRR	$R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$, Figure 4	T _A = +25°C		60		dB
Crosstalk (Note 7)		R_L -50 Ω , C_L = 5pF, f = 1MHz, Figure 5	T _A = +25°C		100		dB
Source Off-Capacitance	C _{S(OFF)}	f = 1MHz, Figure 6	T _A = +25°C		4		рF
Drain Off-Capacitance	C _D (OFF)	f = 1MHz, Figure 6	T _A = +25°C		4		рF
Source On-Capacitance	C _{S(ON)}	f = 1MHz, Figure 7	T _A = +25°C		16		рF
Drain On-Capacitance	C _{D(ON)}	f = 1MHz, Figure 7	T _A = +25°C		16		pF

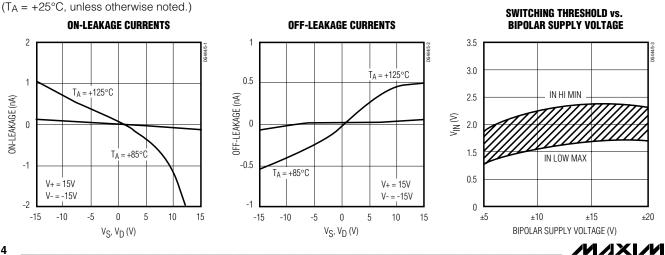
ELECTRICAL CHARACTERISTICS—Single Supply

 $(V+ = 12V, V- = 0, V_L = 5V, GND = 0, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITI	CONDITIONS			MAX	UNITS	
SWITCH								
Analog Signal Range	VANALOG	(Note 3)		0		12	V	
Drain-Source	_	V+ = 10.8V; V _L = 5.25V;	T _A = +25°C		100	160		
On-Resistance	R _{DS} (ON)	$V_D = 3V, 8V; I_S = -10mA$	$T_A = T_{MIN}$ to T_{MAX}			200	Ω	
SUPPLY								
Power-Supply Range	V+, V-			10.8		24.0	V	
Dower Cupply Current	1.	All channels on or off,	T _A = +25°C	-1	+0.001	+1		
Power-Supply Current	l+	$V_{IN} = 0V \text{ or } 5V$	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	μΑ	
Negative Cumply Current	I-	All channels on or off,	T _A = +25°C	-1 -0.0001		+1	μΑ	
Negative Supply Current	1-	$V_{IN} = 0V \text{ or } 5V$	TA = TMIN to TMAX	-5		+5	μΑ	
Logic Supply Current	ΙL	All channels on or off,	T _A = +25°C	-1	+0.001	+1	1	
Logic Supply Current	'L	$V_{IN} = 0V \text{ or } 5V$	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	μA	
Ground Current	lovo	All channels on or off,	T _A = +25°C	-1	-0.0001	+1	μΑ	
Circuita Current	IGND	$V_{IN} = 0V \text{ or } 5V$	$T_A = T_{MIN}$ to T_{MAX}	-5		+5	μΑ	
DYNAMIC								
Turn-On Time	ton	V _S = 8V, Figure 2	T _A = +25°C		300	400	ns	
Turn-Off Time	toff	V _S = 8V, Figure 2	T _A = +25°C		60	200	ns	
Charge Injection (Note 3)	Q	$C_L = 1nF$, $V_{GEN} = 0$, $R_{GEN} = 0\Omega$, Figure 3	T _A = +25°C		5	10	рС	

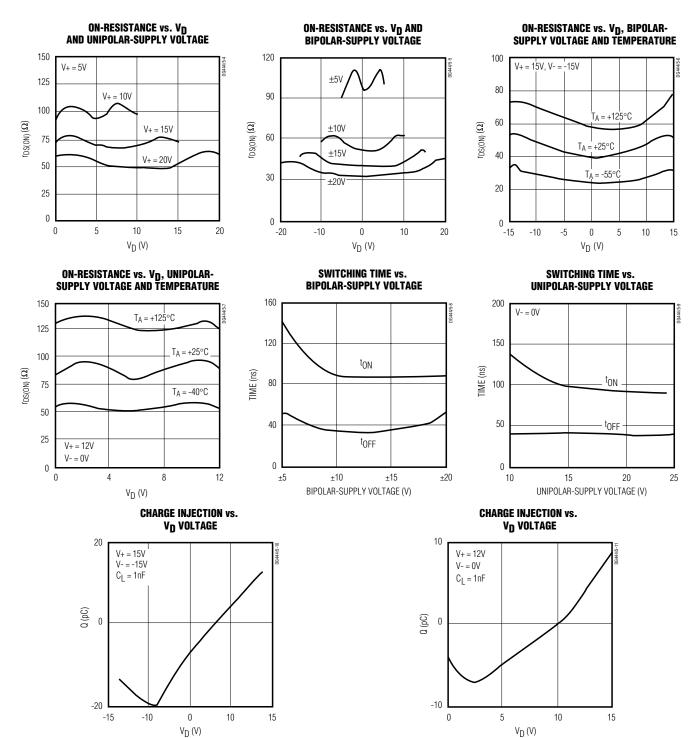
- Note 2: Typical values are for design aid only, are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
- Note 3: Guaranteed by design.
- Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the speci-
- Note 5: Leakage parameters Is(OFF), ID(OFF), ID(ON), and IS(ON) are 100% tested at the maximum rated hot temperature and guaranteed at +25°C.
- **Note 6:** Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.
- Note 7: Between any two switches.

Typical Operating Characteristics



Typical Operating Characteristics

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



Pin Description

PI	N	NAME	EUNCTION				
DIP/SO	THIN QFN	NAME	FUNCTION				
1, 16, 9, 8	15, 14, 7, 6	IN1-IN4	Logic Control Inputs				
2, 15, 10, 7	16, 13, 8, 5	D1-D4	Drain Outputs				
3, 14, 11, 6	1, 12, 9 4	S1–S4	Source Outputs				
4	2	V-	Negative-Supply Voltage Input				
5	3	GND	Ground				
12	10	VL	Logic-Supply Voltage Input				
13	11	V+	Positive-Supply- Voltage Input—Connected to Substrate				
_	EP	PAD	Exposed Pad Connect Pad to V+				

Applications Information

General Operation

- Switches are open when power is off.
- IN, D, and S should not exceed V+ or V-, even with the power off.
- Switch leakage is from each analog switch terminal to V+ or V-, not to other switch terminals.

Operation with Supply Voltages Other than ±15V

Using supply voltages other than $\pm 15V$ will reduce the analog signal range. The DG444/DG445 switches oper-

ate with $\pm 4.5 \text{V}$ to $\pm 20 \text{V}$ bipolar supplies or with a +10 V to +30 V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24 V and -5 V. V_L must be connected to +5 V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 20 \text{V}$, $\pm 15 \text{V}$, $\pm 10 \text{V}$, and $\pm 5 \text{V}$ supplies. (Switching times increase by a factor of two or more for operation at $\pm 5 \text{V}$.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL , V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V-should not exceed +44V.

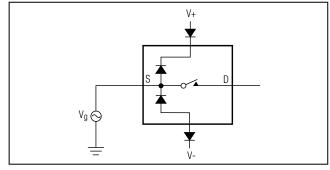


Figure 1. Overvoltage Protection Using External Blocking Diodes

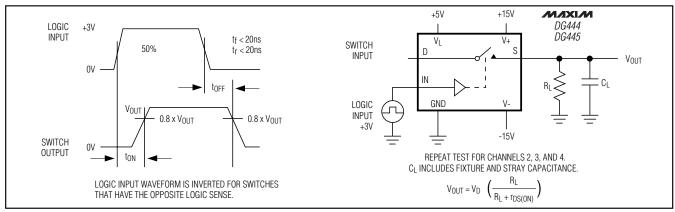


Figure 2. Switching Time

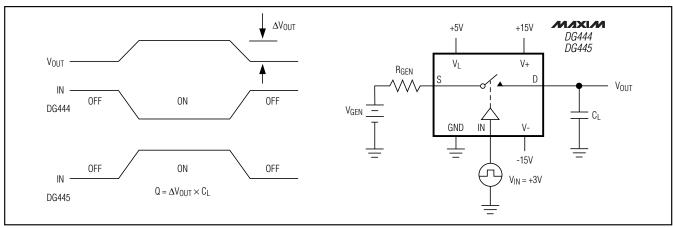


Figure 3. Charge Injection

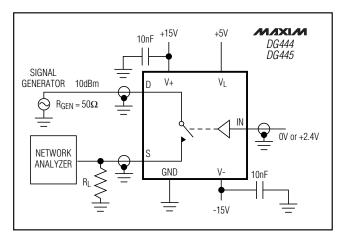


Figure 4. Off-Isolation Rejection Ratio

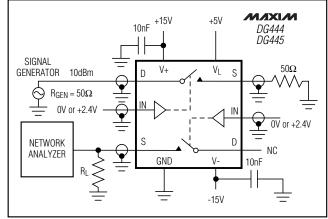


Figure 5. Crosstalk

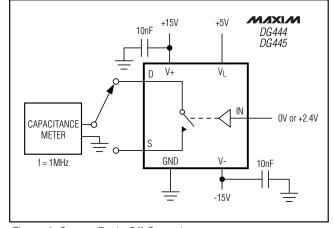


Figure 6. Source/Drain Off-Capacitance

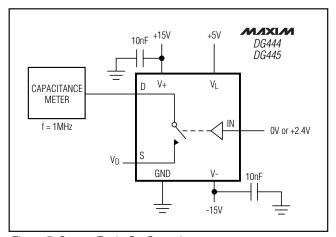
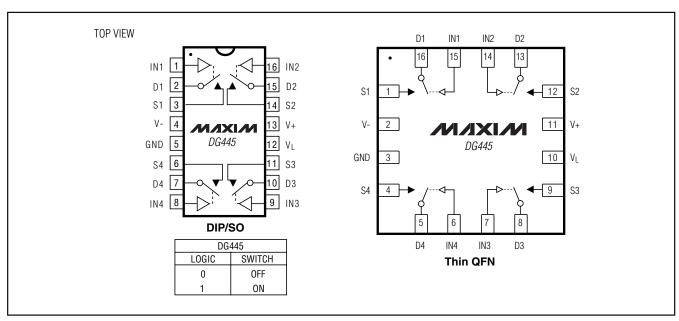


Figure 7. Source/Drain On-Capacitance

Pin Configurations/Functional Diagrams (continued)



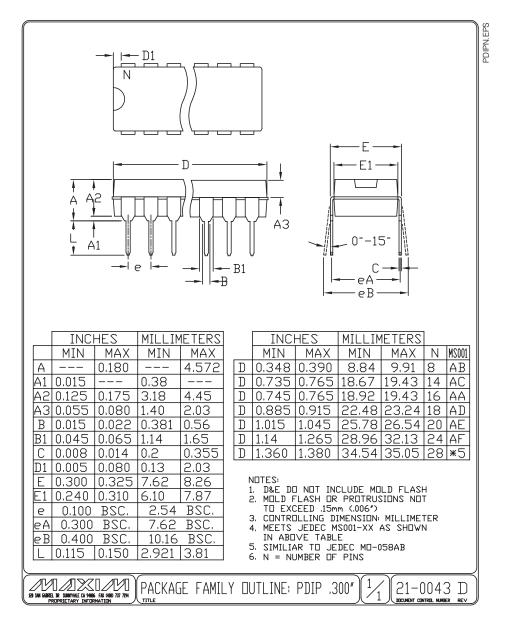
_Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG444ETE	-40°C to +85°C	16 Thin QFN (5mm x 5mm)
DG445CJ	0°C to +70°C	16 Plastic DIP
DG445CY	0°C to +70°C	16 Narrow SO
DG445C/D	0°C to +70°C	Dice*
DG445DJ	-40°C to +85°C	16 Plastic DIP
DG445DY	-40°C to +85°C	16 Narrow SO
DG445ETE	-40°C to +85°C	16 Thin QFN (5mm x 5mm)

^{*}Contact factory for dice specifications.

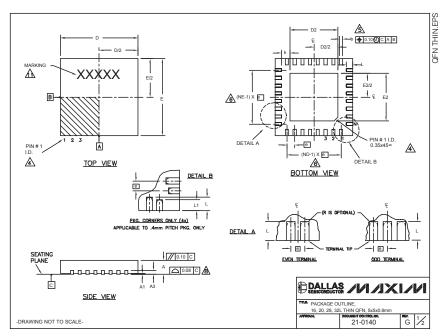
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



SYMBOL INIT NOM MAX MIN ROM MAX MIN MAX MIN ROM MAX MIN ROM MAX MIN MAX MIN ROM MAX MIN ROM MAX MIN MAX MI	SYMBOL MIN. NOM. MAX. 2 to 1 ALLOWER A 0.70 0.75 0.80 0.75 0.90 0.75 0.90 0.70 0.75 0.80 A1 0 0.02 0.05 0 0.02 0.05 0 0.02 0.05 0.00 0.70 0.02 0.05 D 0.22 0.05 0 0.02 0.05 0 0.02 0.05 0.00 0.70 0.02 0.05 D 0.22 0.05 0 0.02 0.05 0 0.02 0.05 0.00 0.02 0.05 D 0.25 0.30 0.35 0.25 0.30 0.35 0.25 0.20 0.25 0.30 0.20 0.25 0.30 D 4.90 5.00 5.10 4.90 5.00 5.10 4.90 5.00 5.10 4.90 5.00 5.10 E 4.90 5.00 5.10 4.90 5.00 5.10 4.90 5.00 5.10 4.90 5.00 5.10 E 4.90 5.00 5.10 4.90 5.00 5.00 5.00 5.00 5.00 5.00 5.00 5	COMMON DIMENSIONS									EXPOSED PAD VARIATIONS													
SYMBOL INN. NOM. IMAX. IMN. N	SYMBOL INN. NOM MAX, MIN, NOM, MAX,	PKG.	SYMBOL MIN. NOM. MAX. MIN. NOM. MAX. MIN. NOM. MAX. MIN. NOM. MAX.			PKG.		D2		E2			L											
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A3	A3	Α	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80		T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
A3 0 20 REF. 0.20 NEF. 0.2	A3 0 20 REP. 0 20 MEP. 0 2	A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05					_		-		**	
B	D	A3	0	_		0			0		_	0:				T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
Table	Test	b	_	_	_	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30		T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
E 4.90 5.00 5.10 5.10 5.10 5.10 5.10 5.10 5.1	E	D	4 90	5.00					4 90	_			5.00	5.10		T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
E 0.80 BSC. 0.65 BSC. 0.50 BSC. 0.50 BSC. 1.205 C 0.50 BSC. 1.205	E	F	_					-			-					T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
K	R	е	0	80 BS	C	0	65 BS	SC.	0	50 BS	SC.	0	50 BS	SC.		T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
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L1 - - - - - - - - -	L1			0.40	0.50	_	0.55	0.65		0.55	0.65	_	0.40	0.50		. = 0 0 0 =						-		
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T2855-3 AND T2855-6. 1. WARPAGE SHALL NOT EXCEED 0.10 mm.	MARKING IS FOR PACKAGE ORITATION REFERENCE ONLY. MINUSER OF LEADS SHOWN ARE FOR REFERENCE ONLY. 16, 20, 28, 32. THIN OFN, 5x5x0.8mm	CONFO OPTIO IDENTI DIMEN FROM ND ANI 7. DEPOF COPLA 9. DRAWI	ORM TO NAL, B IFIER M SION II TERMI D NE F PULATI NARIT NG CO	O JESD UT MU: IAY BE APPLI NAL TII EFER: ON IS F Y APPL	95-1 S ST BE EITHE ES TO P. TO TH POSSIE JIES TO MS TO	SPP-01 LOCAT ER A M META E NUM BLE IN O THE	2. DETED WOOLD OLD OLD OLD OLD OLD OLD OLD OLD OLD	TAILS (ITHIN 1 R MAR) TERM F TERM IMETRI SED HE	OF TER THE ZO KED FI MINAL A MINALS ICAL FA	MINAL NE INE EATUR ND IS ON E ASHION NK SLU	#1 IDE DICATE E. MEASI ACH D N.	ENTIFIE D. THE URED I AND E	ER ARE E TERM BETWE E SIDE	EMINAL #1 EEN 0.25 m RESPECTI	VELY.	0.30 mm		8	DA:					
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