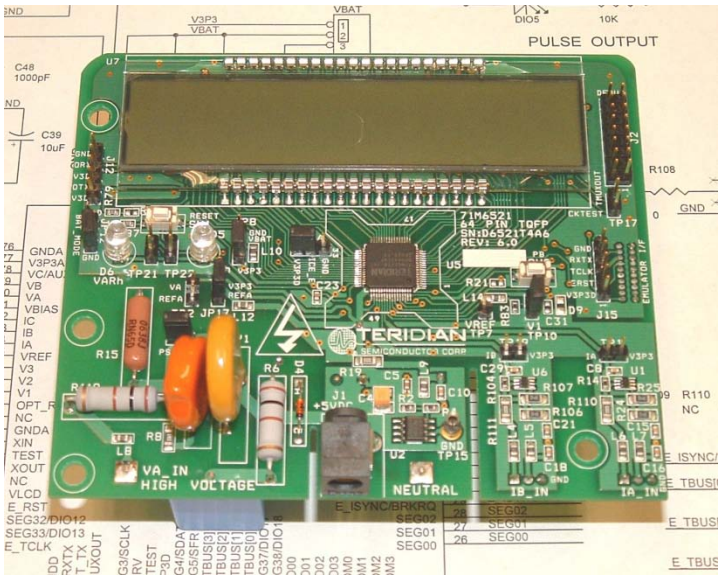

# 71M6521 Demo Board

## USER'S MANUAL

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**Revision 2.18**

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# 71M6521

Single-Phase Energy Meter IC

DEMO BOARD

# USER'S MANUAL

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# 1 GETTING STARTED

## 1.1 GENERAL

The TERIDIAN Semiconductor Corporation (TSC) 71M6521 Demo Board is an energy meter IC demonstration board for evaluating the 71M6521 device for single-phase electronic energy metering applications. It incorporates a 71M6521 integrated circuit, peripheral circuitry such as a serial EEPROM, emulator port, and on-board power supply as well as a companion Debug Board that allows a connection to a PC through a RS232 port. The Demo Board allows the evaluation of the 71M6521 energy meter controller chip for measurement accuracy and overall system use.

The board is pre-programmed with a Demo Program (file name 6521_demo.hex) in the FLASH memory of the 71M6521 IC. This embedded application is developed to exercise all low-level functions to directly manage the peripherals and CPU (clock, timing, power savings, etc.).

## 1.2 SAFETY AND ESD NOTES

Connecting live voltages to the Demo Board system will result in potentially hazardous voltages on the Demo Board.


**EXTREME CAUTION SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD ONCE IT IS CONNECTED TO LIVE VOLTAGES!**


**THE DEMO SYSTEM IS ESD SENSITIVE! ESD PRECAUTIONS SHOULD BE TAKEN WHEN HANDLING THE DEMO BOARD!**

## 1.3 DEMO KIT CONTENTS

- 71M6521 Demo Board containing 71M6521FE IC with preloaded Demo Program
- Shunt resistor with harness, connected to Demo Board
- Debug Board
- Two 5VDC/1,000mA universal wall transformers w/ 2.5mm plug (Switchcraft 712A)
- Serial cable, DB9, Male/Female, 2m length (Digi-Key AE1020-ND)
- CD-ROM containing documentation (data sheet, board schematics, BOM, layout), Demo Code, and utilities
- Adapter PCB (ICE connector to 6X1 header, D6521T4A10 only)
- Connector adapter for 5 VDC supply (D6521T4A10 only, optional)

## 1.4 COMPATIBILITY

This manual applies to the following hardware and software revisions:

- 71M6521FE, chip revision A06
- 71M6521 chip memory configurations 71M6521BE (8KB), 71M6521DE (16KB), 71M6521FE (32KB)
- Demo D6521T4A7 (64-pin, REV 7.0), D6521T4A8 (64-pin, REV 8.0), and D6521T4A10 (64-pin, REV 10.0) Demo Kit firmware revision 4.7 and later

## 1.5 SUGGESTED EQUIPMENT NOT INCLUDED

For functional demonstration:

- PC w/ MS-Windows® versions XP, ME, or 2000, equipped with RS232 port (COM port) via DB9 connector

For software development (MPU code):

- Signum ICE (In Circuit Emulator): ADM-51
  http://www.signum.com
- Keil 8051 "C" Compiler kit: CA51
  http://www.keil.com/c51/ca51kit.htm, http://www.keil.com/product/sales.htm

## 1.6 DEMO BOARD TEST SETUP

Figure 1-1 shows the basic connections of the Demo Boards plus Debug Boards with the external equipment.

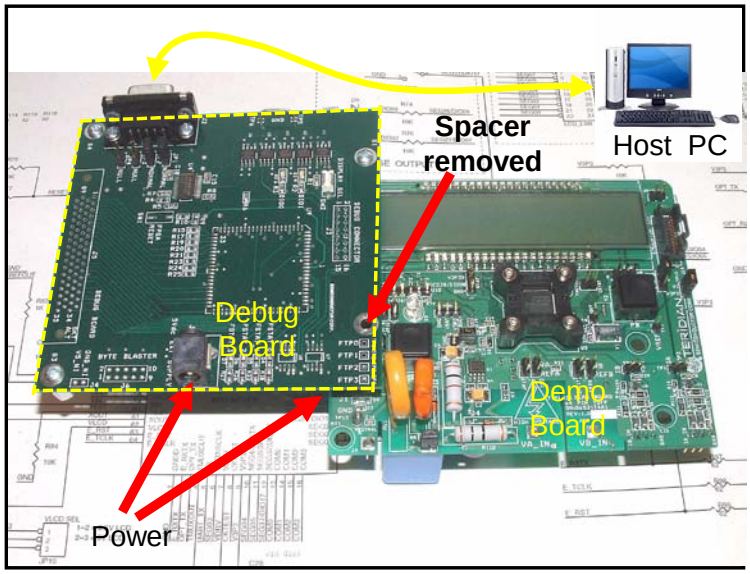



**Figure 1-1: Demo Board: Basic Connections**

The Debug Board can be plugged into J2 of the Demo Board. One spacer of the Debug Board should be removed, as shown in Figure 1-1. Alternatively, both boards can be connected using a flat ribbon cable, as shown in Figure 1-2. A male header has to be soldered to J3 of the Debug Board, and the female-to-female flat ribbon cable is not supplied with the Demo Kit (use Digi-Key P/N A3AKA-1606M-ND or similar).

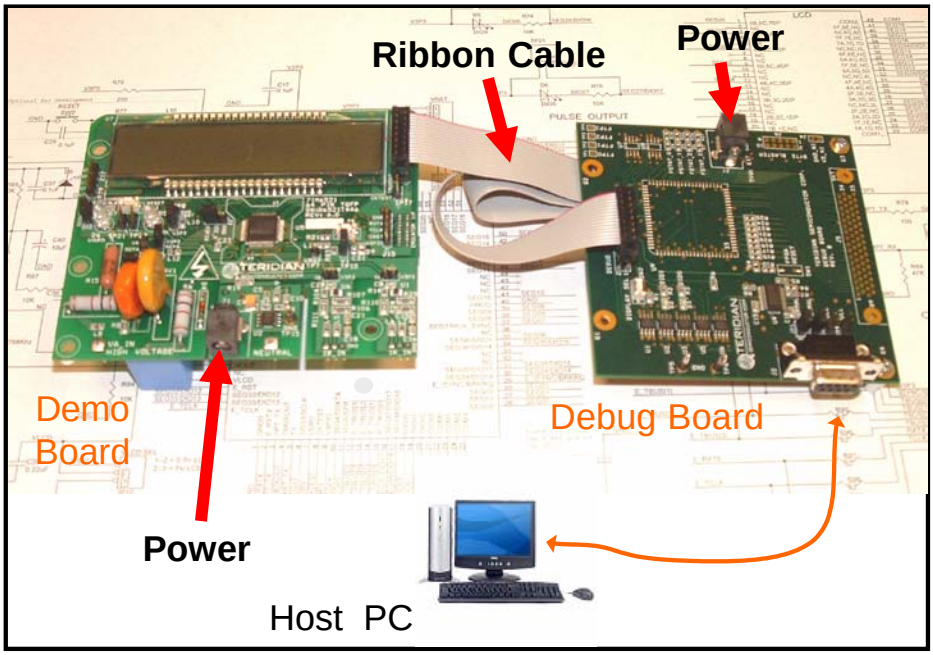



**Figure 1-2: Demo Board: Ribbon Cable Connections**

The 71M6521 Demo Board block diagram is shown in Figure 1-3. It consists of a stand-alone meter Demo Board and an optional Debug Board. The Demo Board contains all circuits necessary for operation as a meter, including display, calibration LED, and power supply. The Debug Board, when not sharing a power supply with the meter, is optically isolated from the meter and interfaces to a PC through a 9 pin serial port.

Connections to the external signals to be measured, i.e. scaled AC voltages and current signals derived from shunt resistors or current transformers, are provided on the rear side of the Demo Board.


**It is recommended to set up the Demo Board with no live AC voltage connected, and to connect live AC voltages only after the user is familiar with the demo system.**

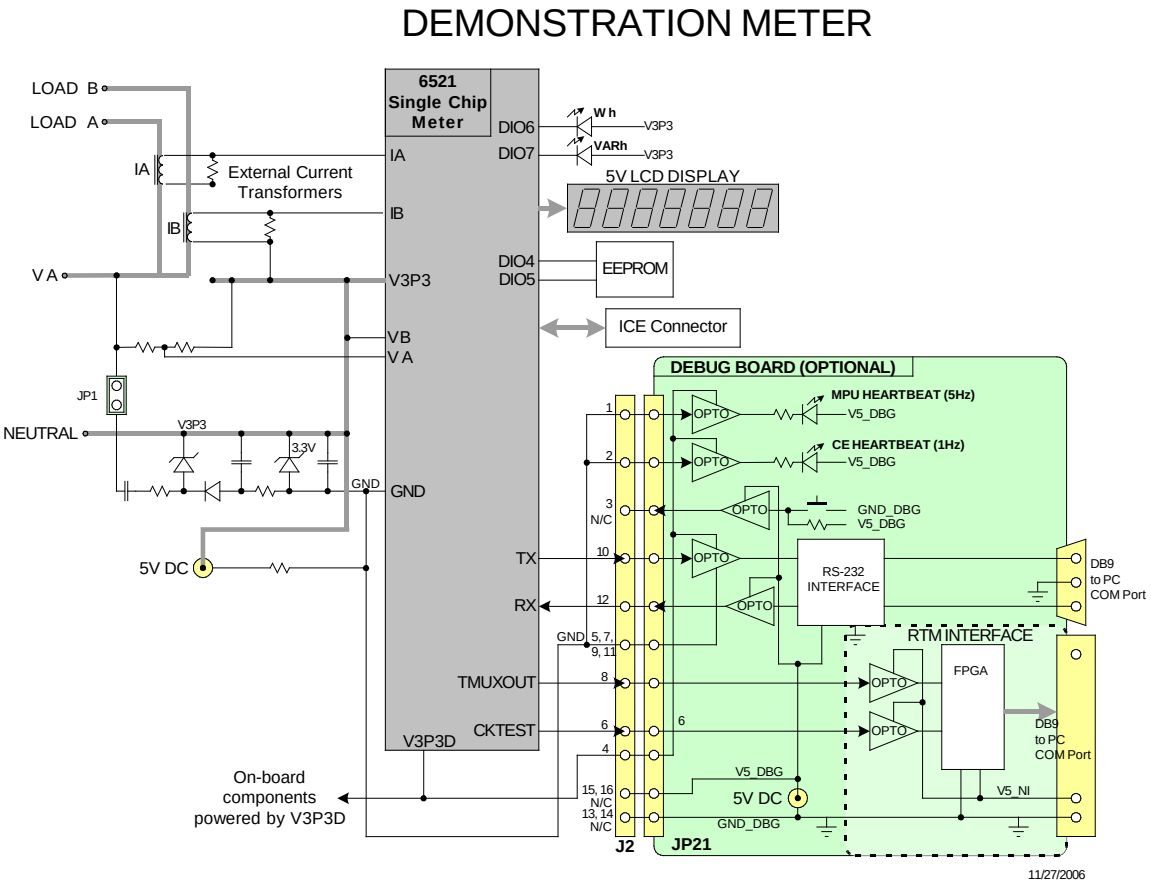



**Figure 1-3: The TERIDIAN 6521 Demo Board with Debug Board Block Diagram (CT Configuration)**

All analog input signals are referenced to the V3P3 (3.3V power supply to the chip).

## 1.6.1 POWER SUPPLY SETUP

There are several choices for meter power supply:

- Internal (using the AC line voltage). The internal power supply is only suitable when the line voltage exceeds 220V RMS.
- External 5VDC connector (J1) on the Demo Board
- External 5VDC connector (J1) on the Debug Board.


The power supply jumper, JP1, must be consistent with the power supply choice. JP1 connects the AC line voltage to the internal power supply. This jumper should usually be left in place.


An adapter may have to be used for the transition between the supplied 5 VDC power supply and the 5-VDC connector on the D6521T4A10 version of the Demo Board.

## 1.6.2 CABLE FOR SERIAL CONNECTION

For connection of the DB9 serial port to a PC, either a straight or a so-called "null-modem" cable may be used. JP1 and JP2 are plugged in for the straight cable, and JP3/JP4 are empty. The jumper configuration is reversed for the null-modem cable, as shown in Table 1-3.

| Cable Configuration | Mode | Jumpers on Debug Board | | | |
|---|---|---|---|---|---|
| | | JP1 | JP2 | JP3 | JP4 |
| Straight Cable | **Default** | Installed | Installed | -- | -- |
| Null-Modem Cable | Alternative | -- | -- | Installed | Installed |

**Table 1-1: Jumper settings on Debug Board**

JP1 through JP4 can also be used to alter the connection when the PC is not configured as a DCE device. Table 1-2 shows the connections necessary for the straight DB9 cable and the pin definitions.

| PC Pin | Function | Demo Board Pin |
|---|---|---|
| 2 | TX | 2 |
| 3 | RX | 3 |
| 5 | Signal Ground | 5 |

**Table 1-2: Straight Cable Connections**

Table 1-3 shows the connections necessary for the null-modem DB9 cable and the pin definitions.

| PC Pin | Function | Demo Board Pin |
|---|---|---|
| 2 | TX | 3 |
| 3 | RX | 2 |
| 5 | Signal Ground | 5 |

**Table 1-3: Null-Modem Cable Connections**

## 1.6.3 CHECKING OPERATION

A few seconds after power up, the LCD display on the Demo Board should briefly display the following welcome text:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | H | E | L | L | 0 | |

After the welcome text, the Demo Board should display the following information:

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3. | | | | 0. | 0 | 0 | 1 |

The number 3 in the leftmost digit indicates that accumulated Watt-hours are displayed. In the case shown above, 0.001 Wh were accumulated. The decimal dot in the leftmost segment will be blinking, indicating activity of the MPU inside the 71M6521.

In Mission Mode, the display can be cycled by pressing the pushbutton (PB).

If no information is stored in the EEPROM, Demo Boards with the 71M6521DE or 71M6521BE will only display the HELLO message and then wait for the user to transfer the CE default data via HyperTerminal.

**Demo Board revisions D6521T4A8 and later require the shunt resistor to be connected for proper operation.** See section 1.8.5 for details.

### 1.6.4 SERIAL CONNECTION SETUP FOR THE PC

After connecting the DB9 serial port to a PC, start the HyperTerminal application (or any other suitable communication program) and create a session using the communication parameters shown in Table 1-4.

| Setup Parameter | 71M6521FE (32KB) Default | 71M6521DE (16KB) | 71M6521BE (8KB) |
|---|---|---|---|
| | | Use only with Demo Codes for 71M6521BE/DE | |
| Port speed (baud) | 9600/300† | 9600/300† | 9600/300† |
| Data bits | 8 | 8 | 8 |
| Parity | none | None | None |
| Stop bits | 1 | 1 | 1 |
| Flow control | XON/XOFF | XON/XOFF | XON/XOFF |
| | † depending on the jumper setting at JP12 | | |

**Table 1-4: COM Port Setup Parameters**

HyperTerminal can be found by selecting Programs →Accessories → Communications from the Windows© start menu. The connection parameters are configured by selecting File → Properties and then by pressing the Configure button (see Figure 1-4).

A setup file (file name "Demo Board Connection.ht") for HyperTerminal that can be loaded with File → Open is also provided with the tools and utilities on the supplied CD-ROM.

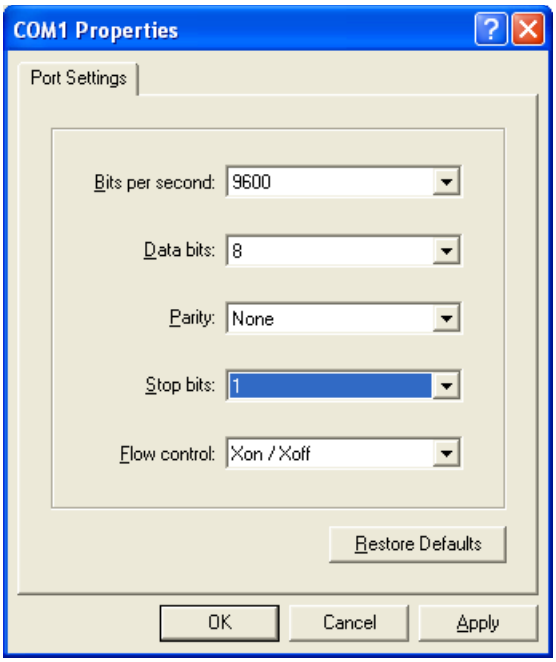



**Figure 1-4: Port Configuration Setup**

Note: Port parameters can only be adjusted when the connection is not active. The disconnect button, as shown in Figure 1-5 must be clicked in order to disconnect the port.

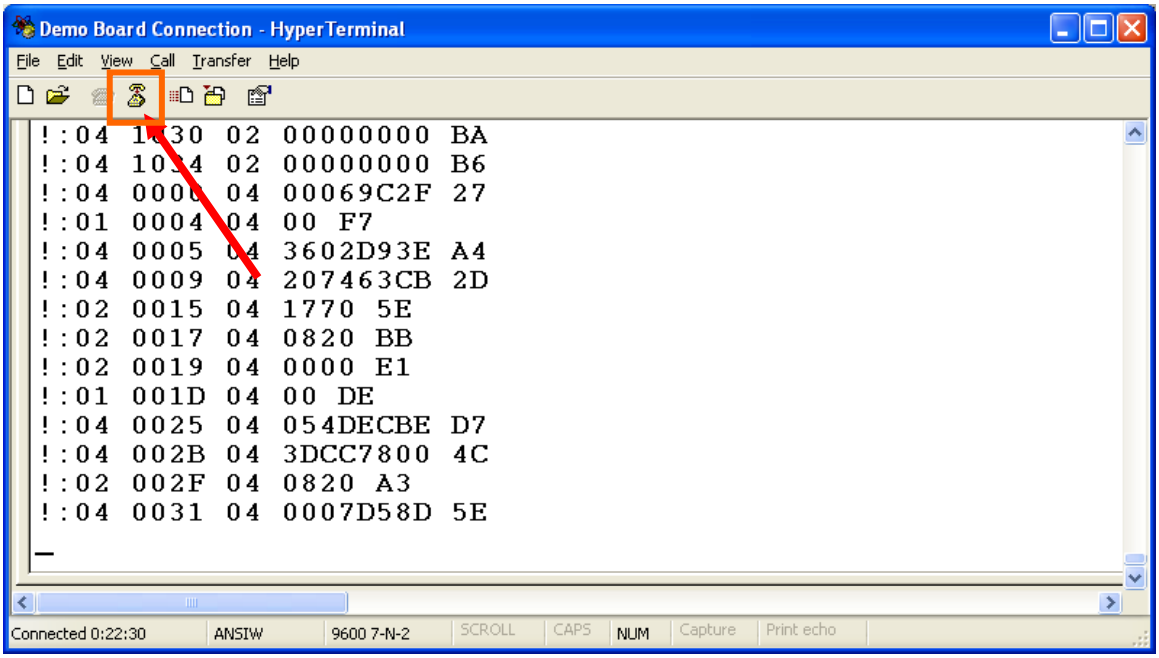



**Figure 1-5: Hyperterminal Sample Window with Disconnect Button**

## 1.7 USING THE DEMO BOARD

The 71M6521 Demo Board is a ready-to-use meter prepared for use with an external current transformer.

Using the Demo Board involves communicating with the Demo Code. An interactive command line interface (CLI) is available as part of the Demo Code (71M6521FE). The CLI allows all sorts of manipulations to the metering parameters, access to the EEPROM, initiation of auto-calibration sequences, selection of the displayed parameters, changing calibration factors and many more operations.

### 1.7.1 COMMUNICATION OPTIONS

Before evaluating the 71M6521 Demo Board, users should get familiar with the commands and responses of the CLI. A complete description of the CLI is provided in section 1.7.2.

The Demo Codes for the 16KB and 8KB flash versions (71M6521BE and 71M6521DE) can be controlled via a protocol that involves Intel Hex Records. This protocol is described in section 1.7.4.

A summary of the communication options is shown in Table 1-5.

| | 71M6521BE | 71M6521DE | 71M6521FE |
|---|---|---|---|
| **Flash size [KB]** | 8 | 16 | 32 |
| **Communication** | Hex records | Hex records | Command line interface |
| **Description in section** | 1.7.2 | 1.7.2 | 1.7.1 |
| **File transfer on power-up** | Not necessary | CE defaults | Not necessary |

**Table 1-5: Summary of Communication Options**

### 1.7.2 CYCLING THE LCD DISPLAY

The Demo Codes for all versions of the 71M6521 Demo Board allow cycling of the display using the PB button. By briefly pressing the button, the next available parameter from Table 1-6 is selected. This makes it easy to navigate various displays for Demo Boards that do not have the CLI.

| Step | Display in left-most digit(s) | Displayed Parameter | Available for 71M6521BE | Available for 71M6521DE | Available for 71M6521FE |
|---|---|---|---|---|---|
| 1 | 1 | Temperature difference from calibration temperature. Displayed in 0.1°C | X | X | X |
| 2 | 2 | Frequency at the VA_IN input [Hz] | X | X | X |
| 3 | 3 | Accumulated real energy [Wh]. The default display setting after power-up or reset. | X | X | X |
| 4 | 9 | Time of day (hh.mm.ss) | X | X | X |
| 5 | - - | Date (yyyy.mm.dd) | X | X | X |
| 6 | 1. 3 | Count of zero crossings in the last accumulation interval | X | X | X |
| 7 | 1. 5 | RMS current at phase A input [A] | X | X | X |
| 8 | 1. 6 | RMS voltage at the VA_IN input [V] | X | X | X |

**Table 1-6: Selectable Display Options**

### 1.7.3 SERIAL COMMAND LINE INTERFACE (CLI)

Once, communication to the Demo Board is established, press <CR> and the Demo Program prompt ("**>**") should appear. Type **>i1** to verify that the Demo Program version is revision 4.7 or later.

Users should familiarize themselves with the Demo Program commands described in the tables below. Due to limited memory space, there is no help menu.

The Demo Program (Demo Code) is compiled with EEPROM specified as the non-volatile memory. This means that the default calibration factors are stored in flash memory whereas the calibration factors resulting from an actual calibration are stored in EEPROM.

The tables below describe the commands in detail.

***Commands for CE Data Access:***

| **]** | **CE DATA ACCESS** | |
|---|---|---|
| Description: | Allows user to read from and write to CE data space. | |
| Usage: | ] [Starting CE Data Address] [option]…[option] | |
| Command combinations: | ]??? | Read consecutive 16-bit words in Decimal |
| | ]$$$ | Read consecutive 16-bit words in Hex |
| | ]U | Update default version of CE Data in EEPROM.<br>**Important: The CE must be stopped (CE0) before issuing this command!** |
| Example: | ]40$$$ | Reads CE data words 0x40, 0x41 and 0x42. |
| | ]7E=12345678=9876ABCD | Writes two words starting @ 0x7E |

CE data space is the address range for the CE DRAM (0x1000 to 0x13FF). All CE data words are in 4-byte (32-bit) format. The offset of 0x1000 does not have to be entered when using the ] command, thus typing ]A? will access the 32-bit word located at the byte address 0x1000 + 4 * A = 0x1028.

***Commands for MPU/XDATA Access:***

| **)** | **MPU DATA ACCESS** | |
|---|---|---|
| Description: | Allows user to read from and write to MPU data space. | |
| Usage: | ) [Starting MPU Data Address] [option]…[option] | |
| Command combinations: | )??? | Read three consecutive 32-bit words in Decimal |
| | )$$$ | Read three consecutive 32-bit words in Hex |
| | )a=n=m | Write the values n and m to two consecutive addresses starting at a |
| Example: | )08$$$$ | Reads data words 0x08, 0x0C, 0x10, 0x14 |
| | )04=12345678=9876ABCD | Writes two words starting @ 0x04 |

MPU or XDATA space is the address range for the MPU XRAM (0x0000 to 0x07FF). All MPU data words are in 4-byte (32-bit) format. Typing ]A? will access the 32-bit word located at the byte address 4 * A = 0x28. The energy accumulation registers of the Demo Code can be accessed by typing two Dollar signs ("$$"), typing question marks will display negative decimal values if the most significant bit is set.

***Commands for DIO RAM (Configuration RAM) and SFR Control:***

| **R** | **DIO AND SFR CONTROL** | |
|---|---|---|
| Description: | Allows the user to read from and write to DIO RAM and special function registers (SFRs). | |
| Usage: | R [option] [register] … [option] | |
| Command combinations: | RIx… | Select I/O RAM location x (0x2000 offset is automatically added) |
| | Rx… | Select internal SFR at address x |
| | Rx???... | Read consecutive SFR registers in decimal |
| | Rx$$$... | Read consecutive registers in hex notation |
| Example: | RI60$$$$ | Read all four RTM probe registers |

DIO or Configuration RAM space is the address range 0x2000 to 0x20FF. This RAM contains registers used for configuring basic hardware and functional properties of the 71M6521 and is organized in bytes (8 bits). The 0x2000 offset is automatically added when the command RI is typed. The SFRs (special function registers) are located in internal RAM of the 80515 core, starting at address 0x80.

***Commands for EEPROM Control:***

| **EE** | **EEPROM CONTROL** | |
|---|---|---|
| Description: | Allows user to enable read and write to EEPROM. | |
| Usage: | EE [option] [arguments] | |
| Command combinations: | EECn | EEPROM Access (1 → Enable, 0 → Disable) |
| | EERa.b | Read EEPROM at address 'a' for 'b' bytes. |
| | EEE | Erase the EEPROM |
| | EESabc..xyz | Write characters to buffer (sets Write length) |
| | EETa | Transmit buffer to EEPROM at address 'a'. |
| | EEWa.b...z | Write values to buffer |
| Example: | EEShello; EET$0210 | Writes 'hello' starting at EEPROM address 0x210. |

The EEC1 command must be issued before the EEPROM interface can be used. The execution of the EEE command takes several seconds. During this time, no other commands can be entered.

***Auxiliary Commands:***

| | **AUXILIARY** | |
|---|---|---|
| Description: | Various | |
| Commands: | , | Typing a comma (",") repeats the command issued from the previous command line. This is very helpful when examining the value at a certain address over time, such as the CE DRAM address for the temperature. |
| | / | The slash ("/") is useful to separate comments from commands when sending macro text files via the serial interface. All characters in a line after the slash are ignored. |
| | BT | Commands execution of a battery test. |

***Commands controlling the CE:***

| **C** | **COMPUTE ENGINE CONTROL** | |
|---|---|---|
| Description: | Allows the user to enable and configure the compute engine. | |
| Usage: | C [option] [argument] | |
| Command combinations: | CEn | Compute Engine Enable (1 → Enable, 0 → Disable) |
| | CTn | Select input n for TMUX output pin. Enter n in hex notation. |
| | CREn | RTM output control (1 → Enable, 0 → Disable) |
| | CRSa.b.c.d | Selects CE addresses for RTM output (maximum of four) |
| Example: | CE0 | Disables the CE |
| | CT1E | Selects the CE_BUSY signal for the TMUX output pin |

***Calibration Commands:***

| **CL** | **CALIBRATION CONTROL** | |
|---|---|---|
| Description: | Calibration-related commands. A full auto-calibration can be implemented by compiling the Demo Code with auto-calibration selected as an option. Due to space restrictions, the auto-calibration is not implemented in the Demo Code supplied with the Demo Boards. | |
| Usage: | CL [option] | |
| Command combinations: | CLC | Switches the CLI to Intel hex format, e.g. for loading calibration data via the serial port |
| | CLD | Restores calibration to defaults |
| | CLR | Restores calibration from EEPROM |
| | CLS | Saves calibration to EEPROM |

***Commands for Identification and Information:***

| **I** | **INFORMATION MESSAGES** | |
|---|---|---|
| Description: | Allows user to display information messages. | |
| Usage: | I | |
| Example: | I | Returns the Demo Code version |

The I command is used to identify the revisions of Demo Code and the contained CE code.

***Commands for Controlling the Metering Values Shown on the LCD Display:***

| **M** | **METER DISPLAY CONTROL (LCD)** | |
|---|---|---|
| Description: | Allows user to select internal variables to be displayed. | |
| Usage: | M [option]. [option] | |
| Command combinations: | M | kWh Total Consumption (display wraps around at 999.999) |
| | M1 | Temperature (C° delta from nominal) |
| | M2 | Frequency (Hz) |
| | M3. [phase] | kWh Total Consumption (display wraps around at 999.999) |
| | M4. [phase] | kWh Total Inverse Consumption (display wraps around at 999.999) |
| | M5. [phase] | kVARh Total Consumption (display wraps around at 999.999) |
| | M6. [phase] | kVAh Total Inverse Consumption (display wraps around at 999.999) |
| | M7. [phase] | VAh Total (display wraps around at 999.999) |
| | M9 | Real Time Clock |
| | M10 | Calendar Date |
| | M13. n | Main edge count (n = 0: accumulated, n = 1: last second) |
| | M17 | Battery voltage. Display will return to M3 after a few seconds. |
| Example: | M3.1 | Displays Wh total consumption of phase A. |

**Displays for total consumption wrap around at 999.999kWh (or kVARh, kVAh) due to the number of available display digits. Internal registers (counters) of the Demo Code are 64 bits wide and do not wrap around.**

**The internal accumulators in the Demo Code use 64 bits and will neither overflow nor wrap around under normal circumstances. The restriction to only six digits is due to the requirement to provide one digit showing the display mode that is separated by a blank digit from the displayed values.**

***Commands for Controlling the RMS Values Shown on the LCD Display:***

| **MR** | **METER RMS DISPLAY CONTROL (LCD)** | |
|---|---|---|
| Description: | Allows user to select meter RMS display for voltage or current. | |
| Usage: | MR [option]. [option] | |
| Command combinations: | MR1. [phase] | Displays instantaneous RMS current |
| | MR2. [phase] | Displays instantaneous RMS voltage |
| Example: | MR1.2 | Displays phase b RMS current. |

***Commands for Controlling the MPU Power Save Mode:***

| PS | POWER SAVE MODE | |
|---|---|---|
| Description: | Enters power save mode | Disables CE, ADC, CKOUT, ECK, RTM, TMUX VREF, and serial port, sets MPU clock to 38.4KHz. |
| Usage: | PS | |

Return to normal mode is achieved by issuing a hardware reset.

***Commands for Controlling the RTC:***

| RT | REAL TIME CLOCK CONTROL | |
|---|---|---|
| Description: | Allows the user to read and set the real time clock. | |
| Usage: | RT [option] [value] … [value] | |
| Command combinations: | RTDy.m.d.w: Day of week | (year, month, day, weekday [1 = Sunday]) |
| | RTR | Read Real Time Clock. |
| | RTTh.m.s | Time of day: (hr, min, sec). |
| | RTAs.t | Real Time Adjust: (speed, trim) |
| Example: | RTD05.03.17.5 | Programs the RTC to Thursday, 3/17/2005 |

***Reset Commands:***

| Z | RESET | |
|---|---|---|
| Description: | Allows the user to cause soft resets | |
| Usage: | Z | Soft reset |
| | W | Simulates watchdog reset |

The Z command acts like a hardware reset. The energy accumulators in XRAM will retain their values.

***Commands for Controlling the LCD and Sleep Modes (when in Brownout Mode):***

| **B** | **POWER MODE CONTROL** | |
|---|---|---|
| **Description:** | Allows the user switch to LCD and Sleep mode when the 71M6521 is in Brownout mode. | |
| **Usage:** | B [option] [value] | |
| **Command combinations:** | BL | Enters LCD mode |
| | BS | Enters Sleep mode |
| | BWSn | Prepares Sleep mode with the wakeup timer set to n seconds |
| | BWMm | Prepares Sleep mode with the wakeup timer set to m minutes |
| **Example:** | BWS8<br>BS | Enters Sleep mode with the wakeup timer set to 8 seconds. The 71M6521 will enter Sleep mode and return to Brownout mode after 8 seconds. |

## 1.7.4 COMMUNICATING VIA INTEL HEX RECORDS

Due to memory restrictions, the text-based command line interface contained in the 71M6521FE Demo Code is not available for the 71M6521BE and 71M6521DE Demo Codes. In addition, the 16KB version of the Demo Code stores the CE data in EEPROM (this saves valuable flash memory space). The 8KB version of the Demo Code avoids the code-intensive storage on EEPROM and uses flash memory, instead.

Communication with the Demo Codes written for the 71M6521BE and 71M6521DE ICs is accomplished using a simplified protocol based on Intel Hex records. These records can still be sent and received with an ordinary terminal, and coding and decoding of commands and responses is straightforward.

These differences of implementation result in slightly different behavior of the Demo Code. These differences are listed in chapters 1.7.4.1 and 1.7.4.2.

In the command line interface of the 71M6521FE Demo Code, a transition to Intel hex format can be initiated by typing "CLC". To revert to the regular CLI, the reset button must be pushed.

### 1.7.4.1 71M6521DE (16KB)

On start-up, the 16KB version of the Demo Code transfers the CE data from EEPROM into the CE DRAM. If, for some reason, the EEPROM is erased, or CE data is compromised, the CE will be halted and the HELLO prompt will be displayed until the user supplies CE data via the UART.

When receiving a <CR> <LF> character combination from the terminal, the 16KB Demo Code will send an asterisk ("*"). This character serves as a feedback to the user, signaling that the Demo Board is functional and that the serial connection is set up properly.

### 1.7.4.2 71M6521BE (8KB)

On start-up, the 8KB version of the Demo Code transfers the CE data from flash memory into the CE DRAM. The flash memory contains default settings when the Demo Board is used for the first time. After the HELLO prompt, the Demo Board will display the last stored energy value on its LCD.

When receiving a <CR> <LF> character combination from the terminal, the 16KB Demo Code will send a line-feed character followed by an asterisk ("*"). This character serves as a feedback to the user, signaling that the Demo Board is functional and that the serial connection is set up properly.

Sending the semicolon character from the terminal to the 8KB Demo Code will cause the Demo Code to repeat the last command. This is useful when examining the same memory location several times, as sometimes required when checking the development of temperature, voltage, or energy values over time.

### 1.7.4.3 Using the Hex-Record Format

Intel's Hex-record format allows program or data files to be encoded in a printable (ASCII) format, allowing editing of the object file with standard tools and easy file transfer between a host and target. An individual Hex-record is a single line in a file composed of one or several Hex-records.

Hex-Records are character strings made of several fields which specify the record type, record length, memory address, data, and checksum. Each byte of binary data is encoded as a 2-character hexadecimal number: the first ASCII character representing the high-order 4 bits, and the second the low-order 4 bits of the byte. The six fields that comprise a Hex-record are defined in Table 1-7.

| Field | Name | Characters | Description |
|---|---|---|---|
| 1 | Start code | 1 | An ASCII colon (":") |
| 2 | Byte count | 2 | The count of the character pairs in the data field. |
| 3 | Address | 4 | The 2-byte address at which the data field is to be loaded into memory. This is the physical XRAM or I/O RAM address, not the 4-byte address used by the command-line interface (CLI). |
| 4 | Type | 2 | 00, 01, or 02. |
| 5 | Data | 0-2n | From 0 to n bytes of executable code, or memory loadable data.<br>n is normally 20 hex (32 decimal) or less. |
| 6 | Checksum | 2 | The least significant byte of the two's complement sum of the values represented by all the pairs of characters in the record except the start code and checksum. |

**Table 1-7: Fields of a Hex Record**

Each record may be terminated with a CR/LF/NULL character. Accuracy of transmission is ensured by the byte count and checksum fields. This is important when series of values such as calibration constants are transmitted to a meter, e.g. by ATE equipment in a factory setting. When entering hex records manually, the user may also choose "FF" ("wild card") as the checksum. In this case, the Demo Code omits comparing the checksum with the received record(s).

This is how the checksum is calculated manually (if necessary):

1) The hex values of all bytes (except start code and checksum itself) are added up.
2) The last two hex digits are subtracted from 0xFF.
3) The value 0x01 is added.

As opposed to the standardized Hex-records that offer three possible types (data, termination, segment base), six different types are supported for communicating with the 71M6521BE and 71M6521DE Demo Codes. These data types basically encode command types (read/write) along with the data source or destination, as listed in Table 1-8.

| Code | Function |
|---|---|
| 00, 02 | Write CE data record, contains data and 16-bit CE address (CE data RAM is located at 0x1000). |
| 01 | End Of File (Quit) record, a file termination record. Contains no data. This record has to be the last line of the file, and only one record per file is permitted. The byte pattern is always ':00000001FF'. Upon receipt of this record, the Demo Code will transfer the received data into non-volatile memory (EEPROM). |
| 03 | Read CE data record, contains empty data field and 16-bit CE address (optional). CE data RAM is located at 0x1000. |
| 04 | Write MPU or I/O RAM data record, contains data and 16-bit MPU address. |
| 05 | Read MPU or I/O RAM data record, contains empty data field and 16-bit MPU address (optional). I/O RAM is located at 0x2000. |
| 06 | Write RTC data record, contains data and 16-bit RTC address. |
| 07 | Read RTC data record, contains empty data field and 16-bit RTC address (optional). |
| 08 | Write SFR data record, contains data and 16-bit SFR address (optional). The MSB is always zero (0). |
| 09 | Read SFR data record, contains empty data field and 16-bit SFR address (optional). |

**Table 1-8: Data (Command) Types**

Table 1-9 lists a few examples of hex records.

| Hex Record | Function |
|---|---|
| `:08 0000 06 00 00 0C 03 18 05 06 00 ff` | Writes (06) eight bytes (08) to RTC, setting the RTC to zero seconds (00), minutes (00), 12 hours (0C), Wednesday (03), 24th (18) of May (05), 2006 (06). Uses the wild card checksum. |
| `:10 0008 00 00004000 00004000 00004000 00004000 E8`<br>`:00 0000 01 FF` | Writes the default values (0x4000) for the calibration constants CAL_IA, CAL_IB, CAL_VA, and CAL_VC to the CE data RAM (00), starting at address 0x08 (0008).<br>The second command causes the Demo Code to write the data to permanent storage. |
| `:10 1020 03 FF` | Causes the Demo Board to display the CE data from address 0x1020 to 0x102F |

**Table 1-9: Hex Record Examples**

The Demo Board will not echo any inputs from the terminal (they screen will stay blank except for the asterisk (*****) issued after the user enters <CR><LF>). It is useful to configure Hyperterminal for "auto-echo". This can be done by selecting "Properties" from the "File" menu, then clicking on the "Settings" tab and clicking the "ASCII Setup" button.

No <ENTER> key is necessary at the end of a manually entered record.

Spaces in between the fields (to increase readability), as in the example above, are ignored by the Demo Boards.

If a hex record is accepted, the Demo Board returns a "**!**". If the hex record is not accepted, the Demo Board sends a "**?**" and other text, depending on the context (only the 16KB Demo Code will send text).

When only a partial record is entered, the Demo Board will time out after around 30 seconds and then send <CR>< LF>.

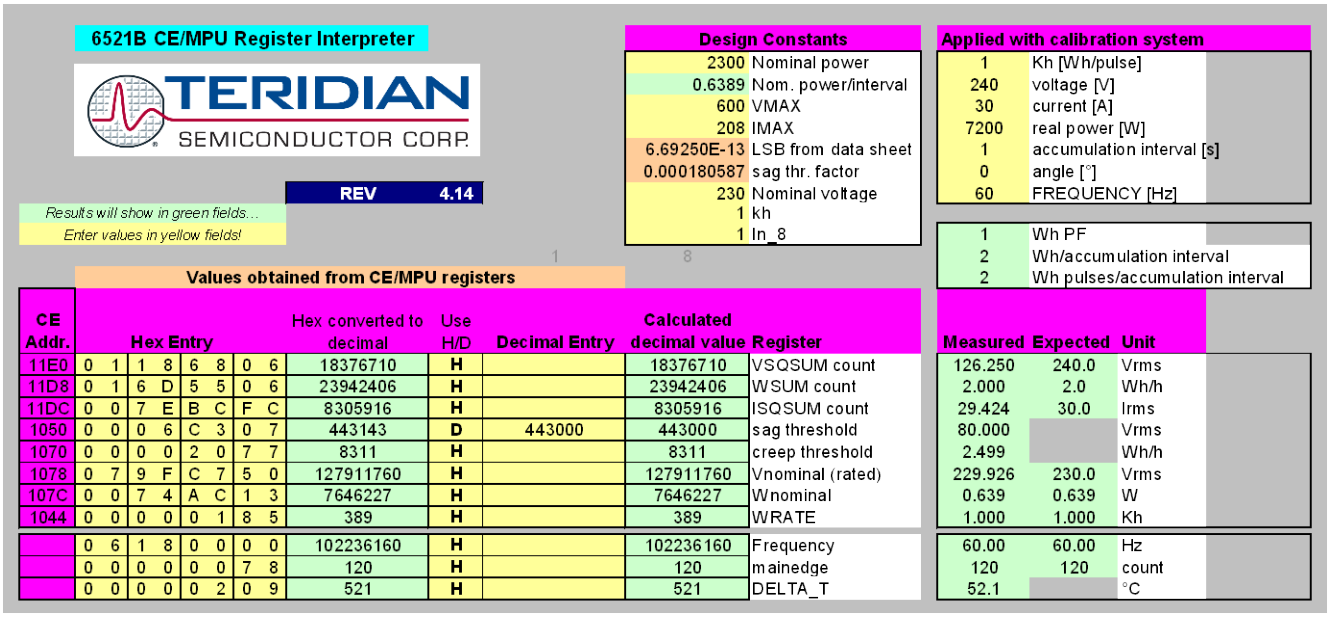
A number of pre-assembled hex records is supplied with the Demo Code. It is easier to send a pre-assembled record using the "send text file" feature in the "Transfer" menu of Hyperterminal, than assembling hex record from scratch.

The pre-assembled hex records are contained in a ZIP file named 6521D_scripts.zip on the CD-ROM supplied with the Demo Kits. Table 1-10 shows the records available and their function.

| Hex Record Name | Function |
|---|---|
| `set_6521D_defaults.txt` | Sets the default configuration, including all CE variables. Transferring this record is necessary when data in the EEPROM is lost or compromised. |
| `read_6521D_temp.txt` | Displays the current temperature reading from the CE |
| `set_6521D_temp.txt` | This record can be edited to set the nominal (calibration) temperature |
| `read_6521D_power.txt` | Displays the valid power data |
| `read_6521D_ce.txt` | Displays CE data from memory locations 0x1020 to 0x10FF |
| `read_6521D_config.txt` | Displays configuration data. This hex record includes comment text helping to interpret the received data. |
| `set_6521D_rtm.txt` | Sets up the real-time monitor |

**Table 1-10: Pre-Assembled Hex Records**

A worksheet named "6521B Register Interpreter" in the Calibration Utility Excel file (651X Calibration Worksheet.XLS or 65XX Calibration Spreadsheets.XLS) supports entry of data directly obtained from the 71M6521BE as Hex Records (see Figure 1-6). Entering a hex value, e.g. for V2SQSUM in the yellow fields will automatically calculate and display the corresponding RMS value in the green field in column "Y", based on the design constants *VMAX*, *IMAX*, LSB, etc.



6521B CE/MPU Register Interpreter

TERIDIAN SEMICONDUCTOR CORP.

REV 4.14

*Results will show in green fields...*
*Enter values in yellow fields!*

**Design Constants**

| | |
|---|---|
| 2300 | Nominal power |
| 0.6389 | Nom. power/interval |
| 600 | VMAX |
| 208 | IMAX |
| 6.69250E-13 | LSB from data sheet |
| 0.000180587 | sag thr. factor |
| 230 | Nominal voltage |
| 1 | kh |
| 1 | In_8 |

**Applied with calibration system**

| | |
|---|---|
| 1 | Kh [Wh/pulse] |
| 240 | voltage [V] |
| 30 | current [A] |
| 7200 | real power [W] |
| 1 | accumulation interval [s] |
| 0 | angle [°] |
| 60 | FREQUENCY [Hz] |
| 1 | Wh PF |
| 2 | Wh/accumulation interval |
| 2 | Wh pulses/accumulation interval |

**Values obtained from CE/MPU registers**

| CE Addr. | Hex Entry | Hex converted to decimal | Use H/D | Decimal Entry | Calculated decimal value | Register | Measured | Expected | Unit |
|---|---|---|---|---|---|---|---|---|---|
| 11E0 | 01 18 68 06 | 18376710 | H | | 18376710 | VSQSUM count | 126.250 | 240.0 | Vrms |
| 11D8 | 01 6D 55 06 | 23942406 | H | | 23942406 | WSUM count | 2.000 | 2.0 | Wh/h |
| 11DC | 00 7E BC FC | 8305916 | H | | 8305916 | ISQSUM count | 29.424 | 30.0 | Irms |
| 1050 | 00 06 C3 07 | 443143 | D | 443000 | 443000 | sag threshold | 80.000 | | Vrms |
| 1070 | 00 00 20 77 | 8311 | H | | 8311 | creep threshold | 2.499 | | Wh/h |
| 1078 | 07 9F C7 50 | 127911760 | H | | 127911760 | Vnominal (rated) | 229.926 | 230.0 | Vrms |
| 107C | 00 74 AC 13 | 7646227 | H | | 7646227 | Wnominal | 0.639 | 0.639 | W |
| 1044 | 00 00 01 85 | 389 | H | | 389 | WRATE | 1.000 | 1.000 | Kh |
| | 06 18 00 00 | 102236160 | H | | 102236160 | Frequency | 60.00 | 60.00 | Hz |
| | 00 00 00 78 | 120 | H | | 120 | mainedge | 120 | 120 | count |
| | 00 00 02 09 | 521 | H | | 521 | DELTA_T | 52.1 | | °C |

**Figure 1-6: 71M6521BE CE/MPU Register Interpreter**

## 1.7.5 USING THE BATTERY MODES

The 71M6521 is in so-called Mission mode, as long as 3.3VDC is supplied to the V3P3SYS pin. If this voltage is below the minimum required operating voltage which is usually indicated by V1 < VBIAS, and if no battery is connected to the VBAT pin, the chip is powered off.

Battery modes can be used if a battery or other DC source supplying a DC voltage with in the operating limits for the battery input is applied to the battery pin (VBAT, pin 49) of the chip. On the Demo Board, the battery should be connected to pin 2 (+) and 3 (-) of JP8.

**In order to prevent corruption of external memory, which could occur when main power is removed from the Demo Board with no battery present, the Demo Code is shipped with the battery modes DISABLED. When the battery modes are disabled, the MPU will be halted once it enters brownout mode, even when a battery is present. See section 1.10.3 for instruction on how to enable battery modes.**

If the main power source (internal or external power supply) is removed while a battery is connected to JP8 as described above, and if the battery modes are enabled with header JP12, the 71M6521 automatically enters Brownout mode. The Demo Code will then automatically transition from Brownout mode to Sleep mode.

By pressing the pushbutton PB, the chip is temporarily brought back to LCD mode. After a few seconds in LCD mode, the chip returns to Sleep mode.

By pressing the RESET pushbutton while the chip is in Sleep mode, the chip will enter Brownout mode.

**Both the RESET and PB buttons are disabled in the Demo Board default configuration. Section 3 contains instructions on how to enable RESET and PB.**

In Brownout mode, the analog functions are disabled, and the MPU functions at very low speed. DIO pins and the UART are still functional. If the chip supports the command line interface, it will signal Brownout mode, and the command prompt "B" will be visible on the terminal connected to the Demo Board, followed by the ">" sign:

```
B>
```

The LCD displays a decimal dot in the left-most digit to indicate that it is in Brownout mode, as shown below:

| . | | H | E | L | L | O | |
|---|---|---|---|---|---|---|---|

The following commands can be entered via the CLI in Brownout mode:

- BL – enters LCD mode
- BS – enters Sleep mode.
- BWSn – enters sleep mode for n seconds, then returns to Brownout mode
- BWMm – enters sleep mode for m minutes, then returns to Brownout mode

In Sleep Mode, almost all functions are disabled. Only the RTC and the wakeup timer are still active. The wakeup signal from the timer and the pushbutton (SW2 on the Demo Board) take the 71M6521 back to Brownout mode.

A hardware reset, while in any battery mode, takes the 71M6521 back to Brownout mode.

**Precautions when adding a battery:** When a battery or other DC supply is added to a Demo Board that is powered down, the 71M6521 Demo Code will cause the chip to enter Brownout mode and stay in Brownout mode. It is possible that the VBAT pins of the chip draws up to 1mA in this state, since the I/O pins are not initialized when Brownout mode is entered from a state where the chip is powered down (if Brownout mode is entered from Mission mode, the I/O pins are properly initialized, and the chip will enter Sleep mode automatically causing much lower supply current into the VBAT).

**To prevent the battery from being drained at an excessive rate, the RESET button should be pressed right after inserting the battery. For this to work, the RESET button must be enabled by removing R91.**

**In general, the firmware for the 71M6521 has to be written to handle the case of connecting a battery to a powered-down board (since in a factory setting, batteries will most likely be added to meter boards that are powered down). The firmware must immediately enter sleep mode in this situation.**

# 1.8 USING THE DEMO BOARD FOR METERING FUNCTIONS

## 1.8.1 USING THE DEMO BOARD IN CT MODE

All versions of the Demo Board, **except for D6521T4A7 and D6521T4A8**, may immediately be used with current transformers having 2,000:1 winding ratio and is programmed for a Kh factor of 3.2 and (see Section 1.8.3 for adjusting the Demo Board for transformers with different turns ratio).

In order to be used with a calibrated load or a meter calibration system, the board should be connected to the AC power source using the spade terminals on the bottom of the board. The current transformers should be connected to the dual-pin headers on the bottom of the board.

**The Demo Boards D6521T4A7 and D6521T4A8 are shipped preconfigured for resistive shunt operation. Instructions for using these boards with a CT can be found in the schematics (see Appendix).**

Once, voltage is applied and load current is flowing, the red LED D5 will flash each time an energy sum of 3.2 Wh is collected. The LCD display will show the accumulated energy in Wh when set to display mode 3 (command >**M3** via the serial interface).

Similarly, the red LED D6 will flash each time an energy sum of 3.2 VARh is collected. The LCD display will show the accumulated energy in VARh when set to display mode 5 (command >**M5** via the serial interface).

## 1.8.2 ADJUSTING THE KH FACTOR FOR THE DEMO BOARD

The Kh value can be derived by reading the values for IMAX and VMAX (i.e. the RMS current and voltage values that correspond to the 250mV maximum input signal to the IC), and inserting them in the following equation for Kh:

$$Kh = IMAX * VMAX * 47.1132 / (In\_8 * WRATE * N_{ACC} * X) = 3.1875 \text{ Wh/pulse.}$$

Where *IMAX* is the current scaling factor, *VMAX* is the voltage scaling factor, *In_8* is the current shunt gain factor, *WRATE* is the CE variable controlling Kh, $N_{ACC}$ is the product of the I/O RAM variables *PRE_SAMPS* and *SUM_CYCLES*, and X is the pulse frequency factor derived from the CE variables *PULSE_SLOW* and *PULSE_FAST*.

The small deviation between the adjusted Kh and the ideal Kh of 3.2 is covered by calibration.

The default values used for the 71M6521 Demo Board are:

| | |
|---|---|
| *WRATE:* | 122 |
| *IMAX*: | 208 |
| *VMAX*: | 600 |
| In_8: | 1 |
| $N_{ACC}$: | 2520 |
| X: | 6 |

**Explanation of factors used in the Kh calculation:**

| | |
|---|---|
| *WRATE:* | The factor input by the user to determine Kh |
| *IMAX*: | The current input scaling factor, i.e. the input current generating 177mVrms at the IA/IB/IC input pins of the 71M6521. 177mV rms is equivalent to 250mV peak. |
| *VMAX*: | The voltage input scaling factor, i.e. the voltage generating 177mVrms at the VA/VB/VC input pins of the 71M6521 |
| In_8: | The setting for the additional ADC gain (8 or 1) determined by the CE register *IA_SHUNT* |
| $N_{ACC}$: | The number of samples per accumulation interval, i.e. *PRE_SAMPS *SUM_CYCLES* |
| X: | The pulse rate control factor determined by the CE registers *PULSE_SLOW* and *PULSE_FAST* |

Almost any desired Kh factor can be selected for the Demo Board by resolving the formula for WRATE:

$$WRATE = (IMAX * VMAX * 47.1132) / (Kh * In\_8 * N_{ACC} * X)$$

For the Kh of 3.2Wh, the value 122 (decimal) should be entered for *WRATE* at location 0x11 (using the CLI command >**]11=+122**).

### 1.8.3 ADJUSTING THE DEMO BOARDS TO DIFFERENT CURRENT TRANSFORMERS AND VOLTAGE DIVIDERS

Revisions D6521T4A7 D6521T4A8 and D6521T4A10 are wired for shunt operation and must be modified for CT operation. With a CT ratio of 2000:1, 208A on the primary side at 2000:1 ratio result in 104mA on the secondary side, causing 177mV at the 1.7Ω resistor pairs R24/R25, R36/R37, R56/R57 (2 x 3.4Ω in parallel).

In general, when *IMAX* is applied to the primary side of the CT, the voltage $V_{in}$ at the IA or IB input of the 71M6521 IC is determined by the following formula:

$V_{in} = R * I = R * IMAX/N$
where N = transformer winding ratio, R = resistor on the secondary side

If, for example, *IMAX* = 208A are applied to a CT with a 2500:1 ratio, only 83.2mA will be generated on the secondary side, causing only 141mV The steps required to adapt a 71M6521 Demo Board to a transformer with a winding ratio of 2500:1 are outlined below:

1) The formula $R_x = 177mV/(IMAX/N)$ is applied to calculate the new resistor $R_x$. We calculate Rx to 2.115Ω
2) **Changing the resistors R24/R25, R106/R107 to a combined resistance of 2.115Ω** (for each pair) will cause the desired voltage drop of 177mV appearing at the IA, or IB inputs of the 71M6521 IC.
3) *WRATE* should be adjusted to achieve the desired Kh factor, as described in 1.8.2.

Simply scaling *IMAX* is not recommended, since peak voltages at the 71M6521 inputs should always be in the range of 0 through ±250mV (equivalent to 177mV rms). If a CT with a much lower winding ratio than 1:2,000 is used, higher secondary currents will result, causing excessive voltages at the 71M6521 inputs. Conversely, CTs with much higher ratio will tend to decrease the useable signal voltage range at the 71M6521 inputs and may thus decrease resolution.

The 71M6521 Demo Board comes equipped with its own network of resistor dividers for voltage measurement mounted on the PCB. The resistor values result in a ratio of 1:3,393.933. This means that *VMAX* equals 276.78mV*3,393.933 = 600V. A large value for *VMAX* has been selected in order to have headroom for overvoltages. This choice need not be of concern, since the ADC in the 71M6521 has enough resolution, even when operating at 120Vrms or 240Vrms.

If a **different set of voltage dividers** or an external voltage transformer is to be used, scaling techniques similar to those applied for the current transformer should be used.

In the following example we assume that the line voltage is not applied to the resistor divider for VA formed by R15-R21, R26-R31, and R32, but to a voltage transformer with a ratio N of 20:1, followed by a simple resistor divider. We also assume that we want to maintain the value for *VMAX* at 600V to provide headroom for large voltage excursions.

When applying *VMAX* at the primary side of the transformer, the secondary voltage $V_s$ is:

$V_s = VMAX / N$

$V_s$ is scaled by the resistor divider ratio $R_R$. When the input voltage to the voltage channel of the 71M6521 is the desired 177mV, $V_s$ is then given by:

$V_s = R_R * 177mV$

Resolving for $R_R$, we get:

$R_R = (VMAX / N) / 177mV = (600V / 30) / 177mV = 170.45$

This divider ratio can be implemented, for example, with a combination of one 16.95kΩ and one 100Ω resistor.

### 1.8.4 CONNECTING DEMO BOARDS TO A SHUNT RESISTOR

Most Demo Kits are shipped with a pre-wired shunt resistor (400µΩ), as shown in Figure 1-7.

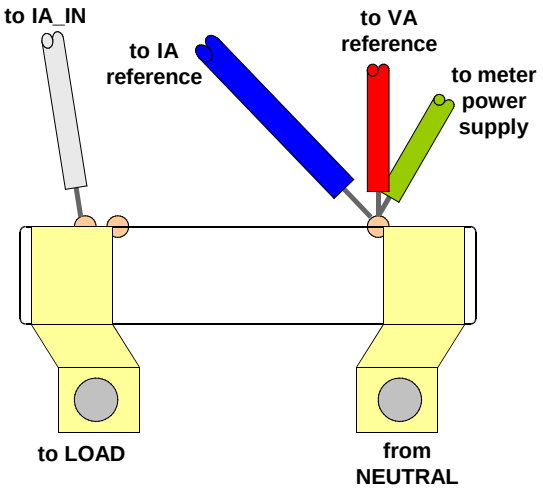



**Figure 1-7: Pre-Wired Shunt Resistor**

For proper operation and accuracy, the wiring instructions given in section 1.8.5 have to be observed. With proper shunt wiring, very accurate measurements can be achieved. The load line shown in **Figure 1-8** was obtained using a 400µΩ shunt resistor connected to a D6521T4A8 Demo Board.

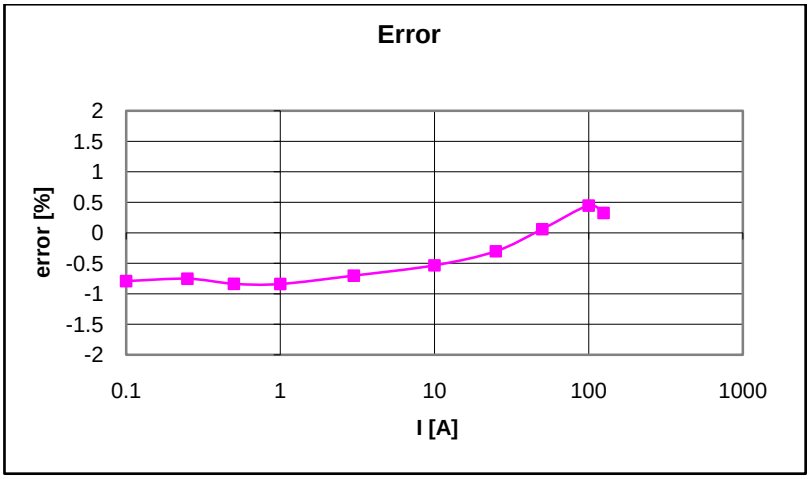



**Figure 1-8: Load Line with Shunt Resistor**

**Important safety precautions apply when operating the Demo Board in shunt mode:**

**In shunt configuration, the whole Demo Board will be at line voltage! Touching the board or any components must be avoided!**

**It is highly recommended to isolate Demo Board and Debug Board (when used) and to provide separate power supplies for the Demo Board and Debug Board.**

**Emulators or other test equipment should never be connected to a live meter without proper isolation! USB isolators are available from various vendors.**

**Only one shunt resistor can be used in a meter, since isolation cannot be maintained when using more than one shunt resistor.**

## 1.8.5 CONNECTING DEMO BOARD REVISIONS D6521T4A7, D6521T4A8, AND D6521T4A10 TO A SHUNT RESISTOR

The Demo Kits containing the Demo Board Revisions D6521T4A7, D6521T4A8, and D6521T4A10 are shipped with a pre-wired shunt resistor (400µΩ), as shown in Figure 1-7. This shunt resistor is connected to the Demo Boards, as shown in Figure 1-9.

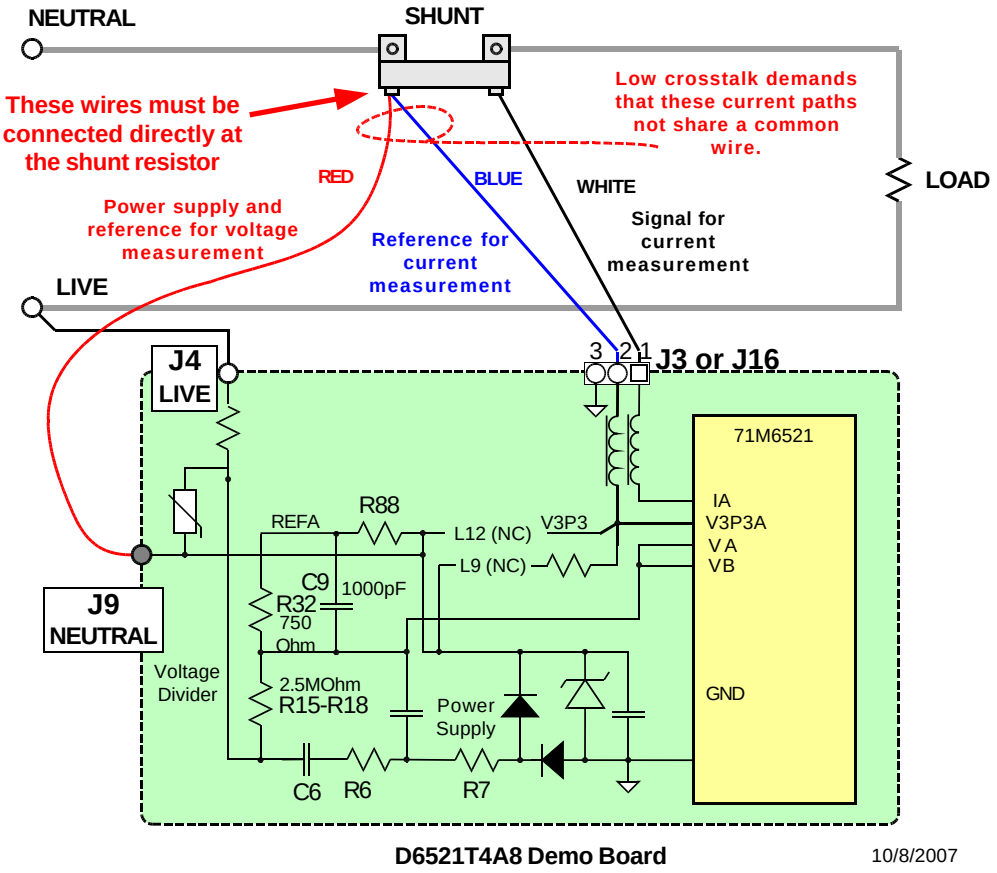



**Figure 1-9: Shunt Connection for D6521T4A7, D6521T4A8, and D6521T4A10**

In order to operate the **D6521T4A7** Demo Board with a current shunt sensor, the following measures must be taken:

a. Remove the jumper on JP17.

b. Make sure that L9 and L12 are removed and that R88 is installed

c. Make sure that R24 is a 10kΩ resistor if IA_IN is the input channel for the current shunt, and that R106 is a 10kΩ resistor if IB_IN is the input channel for the current shunt.

d. The LIVE line must be connected to the spade terminal J4 (bottom of the board).

e. The blue and white pair of wires from the shunt resistor must be connected to contacts 1 and 2 on J3 if IA_IN is the input channel or contacts 1 and 2 on J16 if IB_IN is the input channel. **The white wire must be connected to pin 1, the blue wire must be connected to pin 2**.

f. No connection is necessary for the green wire from the pre-wired shunt resistor.

### 1.8.6 ADAPTING DEMO CODE PARAMETERS TO OPERATION WITH SHUNT RESISTOR

The *IMAX* variable has to checked for current shunt mode using the formula:

$$IMAX = 177mV/R_{shunt}$$

The new value for IMAX (XRAM address 0x0A) should be entered, using the command line interface, as follows (using the shunt resistor provided by TERIDIAN, $R_{shunt} = 400\mu\Omega$, with resulting *IMAX* = 440A):

>**)A=+4400**

*IMAX* values have a LSB resolution of 0.1A, *VMAX* values have a LSB resolution of 0.1V.

Since *IMAX* has been changed, *WRATE* has to be recalculated to maintain the Kh of 3.2Wh per pulse, as shown in chapter 1.8.2. *WRATE* can be entered as follows:

**>]11=+258**

If desired, the CE of the Demo Code can be set to run with increased gain (8 instead of 1) of the current channels, as sometimes required in current shunt mode due to low currents and low shunt resistances. This can be done via the command line interface by the commands

**>]10=5004** setting IA_8 to 8 by controlling IA_SHUNT (bit 2 of CESTATE at CE address 0x10), if IA_IN is connected to the shunt, or

**>]2B=5008** setting IB_8 to 8 by controlling IB_SHUNT (bit 3 of CESTATE at CE address 0x10 if IB_IN is connected to the shunt.

The Demo Code will compensate for the increased gain, i.e. the energy and current readings do not have to be scaled.

## 1.9 CALIBRATION PARAMETERS

### 1.9.1 GENERAL CALIBRATION PROCEDURE

Any calibration method can be used with the 71M6521 chips. This Demo Board User's Manual presents calibration methods with three or five measurements as recommended methods, because they work with most manual calibration systems based on counting "pulses" (emitted by LEDs on the meter).

Naturally, a meter in mass production will be equipped with special calibration code offering capabilities beyond those of the Demo Code. It is basically possible to calibrate using voltage and current readings, with or without pulses involved. For this purpose, the MPU Demo Code can be modified to display averaged voltage and current values (as opposed to momentary values). Also, automated calibration equipment can communicate with the Demo Boards via the serial interface and extract voltage and current readings. This is possible even with the unmodified Demo Code.

A complete calibration procedure is given in section 2.1.3 of this manual.

Regardless of the calibration procedure used, parameters (calibration constants) will result that will have to be applied to the 71M6521 chip in order to make the chip apply the modified gains and phase shifts necessary for accurate operation. Table 1-11 shows the names of the calibration constants, their function, and their location in the CE RAM.

Again, the command line interface can be used to store the calibration constants in their respective CE RAM addresses. For example, the command

>**]8=+16302**

stores the decimal value 16302 in the CE RAM location controlling the gain of the voltage channel (*CAL_VA*).

| Constant | CE Address (hex) | Physical Address (hex) | Description |
|---|---|---|---|
| *CAL_VA*<br>*CAL_VB* | 0x09<br>0x0B | 0x1024<br>0x102C | Adjusts the gain of the voltage channel. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%. |
| *CAL_IA*<br>*CAL_IB* | 0x08<br>0x0A | 0x1020<br>0x1028 | Adjusts the gain of the current channels. +16384 is the typical value. The gain is directly proportional to the CAL parameter. Allowed range is 0 to 32767. If the gain is 1% slow, CAL should be increased by 1%. |
| *PHADJ_A*<br>*PHADJ_B*[1] | 0x0C<br>0x0D | 0x1030<br>0x1034 | This constant controls the CT phase compensation. No compensation occurs when PHADJ=0. As PHADJ is increased, more compensation is introduced.<br>**Note: *PHADJ_B*[1] applies to 3W/1-phase systems.** |

**Table 1-11: CE RAM Locations for Calibration Constants**

## 1.9.2 UPDATING THE 6521_DEMO.HEX FILE

The d_merge program updates the 6521_demo.hex file with the values contained in the macro file. This program is executed from a DOS command line window. Executing the d_merge program with no arguments will display the syntax description. To merge macro.txt and old_6521_demo.hex into new_6521_demo.hex, use the command:

```
d_merge old_6521_demo.hex macro.txt new_6521_demo.hex
```

The new hex file can be written to the 71M6521 through the ICE port using the ADM51 in-circuit emulator. This step makes the calibration to the meter permanent.

## 1.9.3 CALIBRATION MACRO FILE

The macro file in Figure 1-10 contains a sequence of commands to be used for Demo Boards that provide a serial command line interface (CLI). It is a simple text file and can be created with Notepad or an equivalent ASCII editor program. The file is executed with HyperTerminal's *Transfer->Send Text File* command.

```
]8=+16022/  CAL_IA (gain=CAL_IA/16384)
]9=+16381/  CAL_VA (gain=CAL_VA/16384)
]a=+16019/  CAL_IB (gain=CAL_IB/16384)
]b=+16370/  CAL_VB (gain=CAL_VB/16384)
]c=+115/    PHADJ_A (default 0)
]d=+113/    PHADJ_B (default 0)
ce1
```

**Figure 1-10: Typical Calibration Macro file**

It is possible to send the calibration macro file to the 71M6521 for "temporary" calibration. This will temporarily change the CE data values. Upon power up, these values are refreshed back to the default values stored in flash memory. Thus, until the flash memory is updated, the macro file must be loaded each time the part is powered up. The macro file is run by first issuing the ce0 command to turn off the compute engine and then sending the file with the *transfer → send text file* procedure. Turning off the CE before changing CE constants is not a hardware requirement of the chip, but is recommended because of the way the demo code is written.

**Note: Do not use the *Transfer → Send File* command!**

### 1.9.4 UPDATING CALIBRATION DATA IN EEPROM

It is possible to make data permanent that had been entered temporarily into the CE RAM. The transfer to EEPROM is done using the following serial interface command:

```
>]U
```

Thus, after transferring calibration data with manual serial interface commands or with a macro file, all that has to be done is invoking the `]U` command.

### 1.9.5 LOADING THE 6521_DEMO.HEX FILE INTO THE DEMO BOARD

**Hardware Interface for Programming:** The 71M6521 IC provides an interface for loading code into the internal flash memory. This interface consists of the following signals:

E_RXTX (data)

E_TCLK (clock)

E_RST (reset)

These signals, along with V3P3 and GND are available on the emulator header J14. Production meters may be equipped with much simpler programming connectors, e.g. a 5x1 header.

Programming of the flash memory requires a specific in-circuit emulator, the ADM51 by Signum Systems (http//www.signumsystems.com) or the Flash Programmer (TFP2) provided by TERIDIAN Semiconductor.

**In-Circuit Emulator:** If firmware exists in the 71M6521 flash memory, this memory has to be erased before loading a new file into memory. Figure 1-11 and Figure 1-12 show the emulator software active. In order to erase the flash memory, the RESET button of the emulator software has to be clicked followed by the ERASE button (Figure 1-11).

Once the flash memory is erased, the new file can be loaded using the commands File followed by Load. The dialog box shown in Figure 1-12 will then appear making it possible to select the file to be loaded by clicking the Browse button. Once the file is selected, pressing the OK button will load the file into the flash memory of the 71M6521 IC.

At this point, the emulator probe (cable) can be removed. Once the 71M6521 IC is reset using the reset button on the Demo Board, the new code starts executing.

**Teridian Flash Programmer (TFP2):** Follow the instructions given in the User Manual for the TFP2.

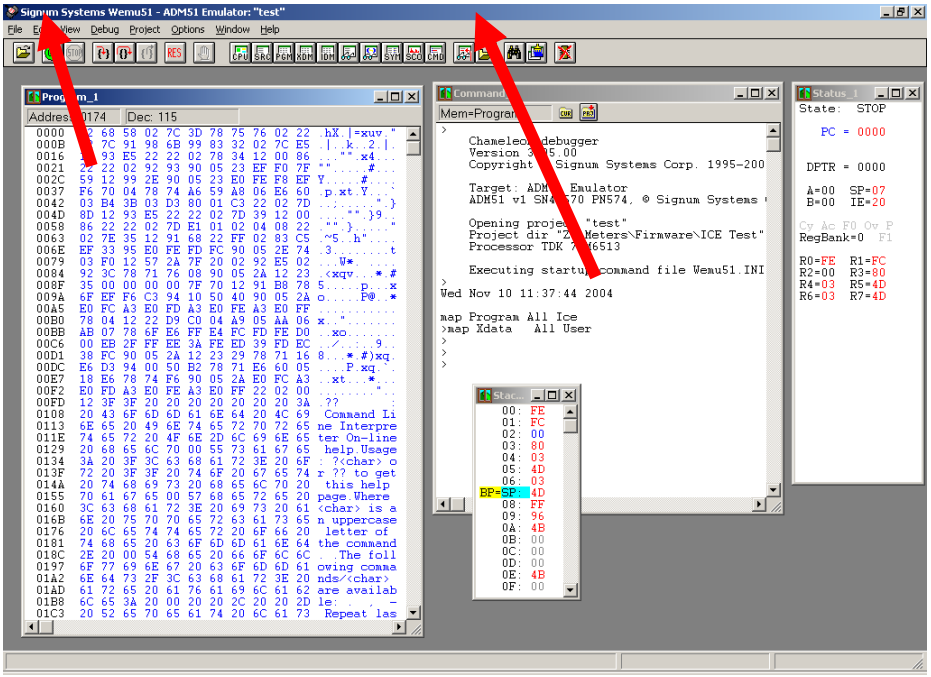


**Figure 1-11: Emulator Window Showing Reset and Erase Buttons**

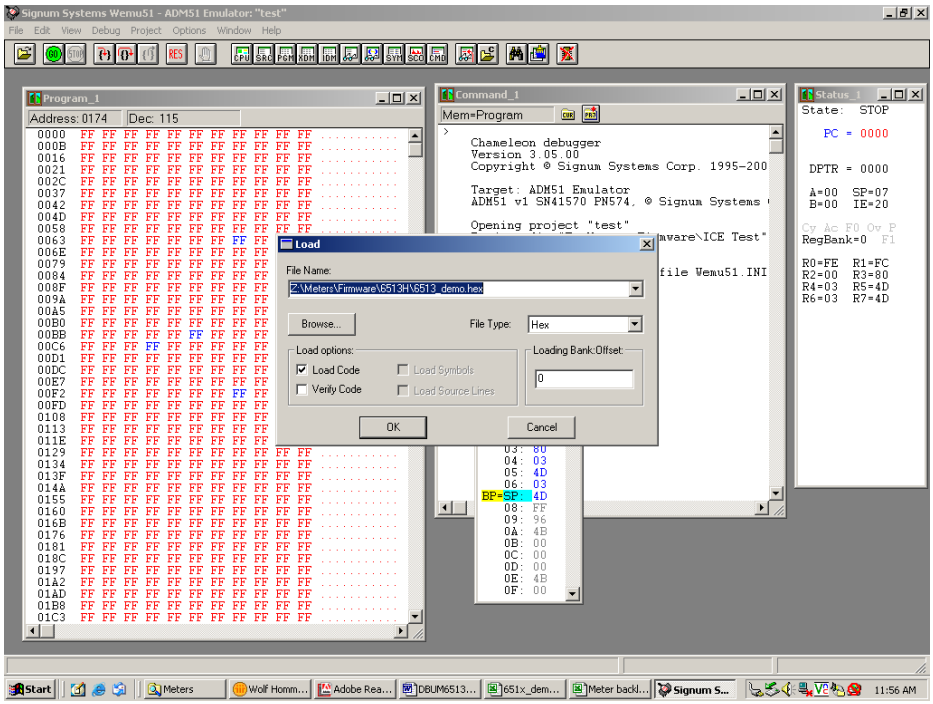


**Figure 1-12: Emulator Window Showing Erased Flash Memory and File Load Menu**

### 1.9.6 THE PROGRAMMING INTERFACE OF THE 71M6521

**Flash Programmer/ICE Interface Signals**

The signals listed in Table 1-12 are necessary for communication between the TFP2 or ICE and the 71M6521.

| Signal | Direction | Function |
|---|---|---|
| E_TCLK | Output from 71M6521 | Data clock |
| E_RXTX | Bi-directional | Data input/output |
| E_RST | Bi-directional | Flash Downloader Reset (active low) |

**Table 1-12: Flash Programming Interface Signals**

The same hardware and software precautions mentioned for emulator (ICE) operation in section 0 apply to TFP2 operation.

## 1.10 DEMO CODE

### 1.10.1 DEMO CODE DESCRIPTION

The Demo Board is shipped preloaded with Demo Code revision 4.7 or later in the 71M6521 chip. The code revision can easily be verified by entering the command >**i** via the serial interface (see section 1.7.2). Check with your local TERIDIAN representative or FAE for the latest revision.

Firmware for the Demo Boards can be updated to revision 4.7 or later using either an in-circuit emulator (ICE) or the Flash Programmer (TFP2), as described in section 1.9.5.

The Demo Code is useful due to the following features:

- It provides basic metering functions such as pulse generation, display of accumulated energy, frequency, date/time, and enables the user to evaluate the parameters of the metering IC such as accuracy, harmonic performance, etc.
- It maintains and provides access to basic household functions such as the real-time clock (RTC).
- It provides access to control and display functions via the serial interface, enabling the user to view and modify a variety of meter parameters such as Kh, calibration coefficients, temperature compensation etc.
- It provides libraries for access of low-level IC functions to serve as building blocks for code development.

The Demo Code source files provided with the TERIDIAN Demo Kits contain numerous routines that are not implemented, due to restrictions in available flash memory space. However, by recompiling the code using different compile-time options, many code variations with different features can be generated. See the Software User's Guide (SUG) for a complete description of the Demo Code.

## 1.10.2 DEMO CODE VARIATIONS

All recent Demo Kits are shipped with the 71M6521FE meter IC (32 KB of flash memory). The Demo Code version programmed into the chip installed in the Demo Board is for the 71M6521FE and for shunt/CT operation.

When planning to develop code for a 71M6521 meter IC with smaller flash size, it can be useful to load the Demo Codes that were written for the smaller flash sizes into the 71M6521FE IC.

- The Demo Code for the 71M6521FE chip (32KB of flash) supports a command line interface. This means that the user can directly communicate with the program by typing commands consisting of text and numbers using a terminal or PC.
- Demo Codes for the 71M6521BE and 71M6521DE have a much more basic user interface that utilizes Intel hex records for serial communication.

## 1.10.3 ACCESSING LCD AND SLEEP MODES FROM BROWNOUT MODE

Header JP12 controls the behavior of the Demo Code when system power is off. The setting of JP12 is read on power up (or after reset), and controls the Demo Code as follows:

- Jumper across pins 1-2 (GND): The Demo Code will communicate at 9600bd. No transitions to sleep or LCD mode will be made from brownout mode.
- Jumper across pins 2-3 (V3P3): The Demo Code will communicate at 300bd. Transitions to sleep or LCD mode can be made from brownout mode. **This operation mode requires connection of a battery or equivalent DC voltage at JP8.**

## 1.10.4 DEMO CODE MEMORY LOCATIONS FOR THE 71M6521DE/FE

Registers in MPU data RAM can be accessed via the command line interface (71M6521FE) or the using the method involving Intel Hex records (71M6521DE).

Table 1-13 lists MPU addresses of interest. Manipulating the values in the MPU addresses enables the user to change the behavior of the meter. For example, if the current transformer external to the Demo Board is changed, a different IMAX value n may have to be applied. This can be done by changing the value in the address 0x0A using the CLI command **)A=n**. Modifications to MPU data RAM will not be maintained when a reset or power-up occurs.

**Changes to the MPU data RAM can be made permanent by creating a macro file containing one or several CLI commands and merging the macro file into the code using the io_merge utility described in section 1.9.2.**

The following is an example showing how the battery bit can be set permanently by creating a new object file:

A text file (battery.txt) is generated, containing the CLI command **)1=20**. The io_merge utility is called, using the following syntax (**6521_demo.hex** is the existing object file):

```
io_merge 6521_demo.hex battery.txt new_6521_demo.hex
```

Now, the object file **new_6521_demo.hex** contains the battery bit.

| Name | Purpose | Function or LSB Value | CLI | Format | L in bits | XDATA |
|---|---|---|---|---|---|---|
| IThrshldA | Starting current, element A | $LSB = 2^{16}\sqrt{I0SQSUM}$ | )0 | unsigned | 32 | 0x0000 |
| | 0 in this location disables creep logic for both element A and B. The default value is 241610. The current threshold for this value is $LSB = \frac{241610}{2^{16}} 442\sqrt{6.6952 \cdot 10^{-13} \cdot 3600} = 80mA$ if IMAX = 442 A. | | | | | |
| Config | Configure meter operation on the fly. | bit 0:** reserved<br>0: VA = Vrms * Irms;<br>1: $VA = \sqrt{Wh^2 + VARh^2}$<br>bit1:* 1 = Clears accumulators<br>bit2:*1 = Calibration mode<br>bit3:** reserved: 1 = enable tamper detection<br>**bit 5: 1 = battery modes enabled** | )1 | N/A | 8 | 0x0004 |
| VPThrshld | error if exceeded.* | $LSB = 2^{16}\sqrt{V0SQSUM}$ | )2 | unsigned | 32 | 0x0005 |
| IPThrshld | error if exceeded.* | $LSB = 2^{16}\sqrt{I0SQSUM}$ | )3 | unsigned | 32 | 0x0009 |
| Y_Cal_Deg0 | RTC adjust | 100ppb | )4 | signed | 16 | 0x000D |
| Y_Cal_Deg1 | RTC adjust, linear by temp.* | 10ppb*ΔT, in 0.1˚C | )5 | signed | 16 | 0x000F |
| Y_Cal_Deg2 | RTC adjust, squared by temp.* | 1ppb*$\Delta T^2$, in 0.1˚C | )6 | signed | 16 | 0x0011 |
| PulseWSource<br>PulseVSource | Wh Pulse source, VARh pulse source selection* | See table for PulseWSource and PulseVSource | )7<br>)8 | unsigned | 8 | 0x0013<br>0x0014 |
| Vmax | Scaling Maximum Voltage for PCB, equivalent to 176mV at the VA/VB pins | 0.1V | )9 | unsigned | 16 | 0x0015 |
| ImaxA | Scaling maximum current for PCB, element A, equi-valent to 176mV at the IA pin | 0.1A | )A | unsigned | 16 | 0x0017 |
| ppmc1 | ADC linear adjust with temperature | PPM per degree centigrade. Default value is +150. | )B | signed | 16 | 0x0019 |
| ppmc2 | ADC quadratic adjust with temperature | PPM per degree centigrade squared. Default value is -392. | )C | signed | 16 | 0x001B |
| Pulse 3 source | Source for software pulse output 3** | See table for PulseWSource and PulseVSource | )D | unsigned | 8 | 0x001D |
| Pulse 4 source | Source for software pulse output 4** | See table for PulseWSource and PulseVSource | )E | unsigned | 8 | 0x001E |
| Scal | Duration for auto-calibration** in seconds | Count of accumulation intervals to be used for auto-calibration. | )F | unsigned | 16 | 0x001F |

| Name | Purpose | Function or LSB Value | CLI | Format | L in bits | XDATA |
|---|---|---|---|---|---|---|
| Vcal | Voltage value to be used for auto-calibration** | Nominal RMS voltage applied to all elements during auto-calibration (LSB = 0.1V). | )10 | unsigned | 16 | 0x0021 |
| Ical | Current value to be used for autocalibration** | Nominal RMS current applied to all elements during auto-calibration (LSB = 0.1V). Power factor must be 1. | )11 | unsigned | 16 | 0x0023 |
| VThrshld | Voltage at which to measure frequency, zero crossing, etc. | $LSB = 2^{16}\sqrt{V0SQSUM}$<br>This feature is approximated using the CE's sag detection.) | )12 | unsigned | 16 | 0x0025 |
| PulseWidth | Maximum time pulse is on. | t = (2*PulseWidth + 1)*397µs, 0xFF disables this feature. Takes effect only at start-up. | )13 | signed | 16 | 0x0029 |
| temp_nom | Nominal temperature, the temperature at which calibration occurs. | Units of TEMP_RAW, from CE. The value read from the CE must be entered at this address. | )14 | unsigned | 32 | 0x002B |
| ImaxB | Scaling maximum current for PCB element B, equivalent to 176mV at the IA pin | 0.1A | )15 | unsigned | 16 | 0x002F |
| IThrshldB | Starting current, element B | $2^{16}\sqrt{I1SQSUM}$ | )16 | unsigned | 32 | 0x0031 |
| VBatMin* | Minimum battery voltage. | Same as VBAT, below | )17 | unsigned | 32 | 0x0035 |
| CalCount | Count of calibrations | Counts the number of times calibration is saved, to a maximum of 255 | )18 | unsigned | 8 | 0x0039 |
| RTC copy | Nonvolatile copy of the most recent time the RTC was read. | Sec, Min, Hr, Day, Date, Month, Year | )19<br>1A<br>1B<br>1C<br>1D<br>1E<br>1F | unsigned | 8<br>8<br>8<br>8<br>8<br>8<br>8 | 0x163 |
| deltaT | Difference between raw temperature and temp_nom | Same units as TEMP_RAW | )20 | signed | 32 | 0x003B |
| Frequency* | Frequency | Units from CE. | )21 | unsigned | 32 | 0x003F |
| VBAT* | Last measured battery voltage* | $VBAT = \frac{n_{ADC}}{2^9}$<br>ADC counts, logically shifted right by 9 bits. Note: battery voltage is measured once per day, except when it is being displayed or requested with the BT command. | )22 | unsigned | 32 | 0x0043 |
| Vrms_A | Vrms, element A | $2^{16}\sqrt{V0SQSUM}$ | )23 | unsigned | 32 | 0x004B |
| Irms_A | Irms, element A | $2^{16}\sqrt{I0SQSUM}$ | )24 | unsigned | 32 | 0x004F |

| Name | Purpose | Function or LSB Value | CLI | Format | L in bits | XDATA |
|---|---|---|---|---|---|---|
| Vrms_B | Vrms, element B**,† | $2^{16}\sqrt{V1SQSUM}$ | )25 | unsigned | 32 | 0x0053 |
| Irms_B | Irms, element B | $2^{16}\sqrt{I1SQSUM}$ | )27 | unsigned | 32 | 0x0057 |
| STATUS | Status of meter | See table for STATUS register | )2A | unsigned | 32 | 0x0063 |
| CAI | Count of accumulation intervals since reset, or last clear. | count | )28 | signed | 32 | 0x0067 |
| Whi** | Imported Wh, all elements. | LSB of W0SUM | )2C | signed | 64 | 0x006B |
| Whi_A** | Imported Wh, element A | " | )2E | signed | 64 | 0x0073 |
| Whi_B** | Imported Wh, element B | " | )30 | signed | 64 | 0x007B |
| VARhi* | Imported VARh, all elements. | LSB of W0SUM | )34 | signed | 64 | 0x008B |
| VARhi_A* | Imported VARh, element A | " | )36 | signed | 64 | 0x0093 |
| VARhi_B* | Imported VARh, element B | " | )38 | signed | 64 | 0x009B |
| VAh** | VAh, all elements. | LSB of W0SUM | )3C | signed | 64 | 0x00AB |
| VAh_A** | VAh, element A | " | )3E | signed | 64 | 0x00B3 |
| VAh_B** | VAh, element B | " | )40 | signed | 64 | 0x00BB |
| Whe** | Exported Wh, all elements. | LSB of W0SUM | )44 | signed | 64 | 0x00CB |
| Whe_A** | Exported Wh, element A | " | )46 | signed | 64 | 0x00D3 |
| Whe_B** | Exported Wh, element B | " | )48 | signed | 64 | 0x00DB |
| VARhe** | Exported VARh, all elements. | LSB of W0SUM | )4C | signed | 64 | 0x00EB |
| VARhe_A** | Exported VARh, element A | " | )4E | signed | 64 | 0x00F3 |
| VARhe_B** | Exported VARh, element B | " | )50 | signed | 64 | 0x00FB |
| Whn | Net metered Wh, all elements A, | LSB of W0SUM | )54 | signed | 64 | 0x010B |
| Whn_A* | Net metered Wh, element A, for autocalibration | LSB of W0SUM | )56 | signed | 64 | 0x0113 |
| Whn_B* | Net metered Wh, element B, for autocalibration | " | )58 | signed | 64 | 0x011B |
| VARhn* | Net metered VARh, all elements | LSB of W0SUM | )5C | signed | 64 | 0x012B |
| VARhn_A* | Net metered VARh, element A, for autocalibration | LSB of W0SUM | )5E | signed | 64 | 0x0133 |
| VARhn_B* | Net metered VARh, element B, for autocalibration | " | )60 | signed | 64 | 0x013B |

| Name | Purpose | Function or LSB Value | CLI | Format | L in bits | XDATA |
|---|---|---|---|---|---|---|
| MainEdgeCnt | Count of voltage zero crossings | count | )64 | unsigned | 32 | 0x014B |
| Wh | Default sum of Wh, nonvolatile | LSB of W0SUM | )65 | signed | 64 | 0x014F |
| Wh_A | Wh, element A, nonvolatile | " | )67 | signed | 64 | 0x0157 |
| Wh_B | Wh, element B, nonvolatile | " | )69 | signed | 64 | 0x015F |
| StatusNV | Nonvolatile status | See Status | )6D | n/a | 32 | 0x016F |

*M6521FE (32K) only; compilation option in M6521DE (16K)
**Compilation option (available demo code), variable present but not in use.
† Requires features not in standard demo PCB

**Table 1-13: MPU memory locations (71M6521DE/FE)**

Table 1-14 lists the possible entries for the *PULSEWSOURCE* and *PULSEVSOURCE* registers.

| Decimal Value in *PULSEWSOURCE, PULSEVSOURCE* | Selected Pulse Source | Decimal Value in *PULSEWSOURCE, PULSEVSOURCE* | Selected Pulse Source |
|---|---|---|---|
| 0 | EQU= 0: *W0SUM*<br>if *W0SUM* > *W1SUM*, *W1SUM*<br>if *W1SUM* > *W0SUM**** | 18 | (reserved) |
| 1 | *W0SUM* | 19 | *WSUM_I*** |
| 2 | *W1SUM* | 20 | *W0SUM_I*** |
| 3 | (reserved) | 21 | *W1SUM_1*** |
| 4 | *VARSUM* | 22 | (reserved) |
| 5 | *VAR0SUM* | 23 | *VARSUM_I** |
| 6 | *VAR1SUM* | 24 | *VAR0SUM_I** |
| 7 | (reserved) | 25 | *VAR1SUM_I** |
| 8 | *I0SQSUM* | 26 | (reserved) |
| 9 | *I1SQSUM* | 27 | *WSUM_E*** |
| 10 | (reserved) | 28 | *W0SUM_E*** |
| 11 | *INSQSUM* | 29 | *W1SUM_E*** |
| 12 | *V0SQSUM* | 30 | (reserved) |
| 13 | *V1SQSUM†* | 31 | *VARSUM_E*** |
| 14 | (reserved) | 32 | *VAR0SUM_E*** |
| 15 | *VASUM*** | 33 | *VAR1SUM_E*** |
| 16 | *VA0SUM*** | 34 | (reserved) |
| 17 | *VA1SUM*** | | |

*M6521F (32K) only; compilation option in M6521D (16K)
**Compilation option (available demo code), variable present but not in use
*****Changing the equation (EQU) in the I/O RAM does not alter the computations implemented in the Demo Code.**
† Requires features not in standard demo PCB

**Table 1-14: Values for Pulse Source Registers**

Table 1-15 explains the bits of the STATUS register.

| Bit | Significance | Bit | Significance |
|---|---|---|---|
| 0 | CREEP | 16 | BATTERY_BAD, voltage below VBatMin |
| 1 | | 17 | -- |
| 2 | PB_PRESS, wake pushbutton was pressed | 18 | CAL_BAD (Checksum over calibration factors is invalid) |
| 3 | WAKE_ALARM | 19 | CLOCK_UNSET (Clock is not set) |
| 4 | -- | 20 | POWER_BAD (checksums for both energy registers are invalid) |
| 5 | MAXVA, voltage A exceeded maximum | 21 | GNDNEUTRAL (grounded neutral detected**) |
| 6 | MAXVB, voltage B exceeded maximum | 22 | TAMPER (tamper detected via I/O pin**) |
| 7 | -- | 23 | VXEDGE, as reported by CE |
| 8 | -- | 24 | -- |
| 9 | WD_DETECTED, reset from HW WDT was detected | 25 | SAGA (sag detected on A) |
| 10 | -- | 26 | SAGB (Sag detected on B†) |
| 11 | MAXIA, current A exceeded maximum | 27 | -- |
| 12 | MAXIB, current A exceeded maximum | 28 | F0_CE (reflects F0 bit from CE) |
| 13 | -- | 29 | -- |
| 14 | MINT (minimum temperature exceeded) | 30 | -- |
| 15 | MAXT (maximum temperature exceeded) | 31 | ONE_SEC |

**Table 1-15: STATUS Register**

## 1.10.5 CE CODE MEMORY LOCATIONS (71M6521DE/FE)

All CE memory locations are listed in the 71M6521DE/FE data sheet. These locations are listed again in Table 1-16, along with the addresses used by the CLI and the physical addresses used by the hex records interface. The corresponding CE address for the most significant byte is given by 0x1000 + 4 x CLI_address and 0x1003 + 4 x CLI_address for the least significant byte.

| CLI Address | Physical Address | Name | Default | Description |
|---|---|---|---|---|
| 0x08 | 0x1020 | *CAL_IA* | 16384 | These constants control the gain of their respective channels. The nominal value for each parameter is $2^{14}$ = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be scaled by 1/(1 – 0.01). |
| 0x09 | 0x1024 | *CAL_VA* | 16384 | |
| 0x0A | 0x1028 | *CAL_IB* | 16384 | |
| 0x0B | 0x102C | *CAL_VB* | 16384 | |
| 0x0C | 0x1030 | *PHADJ_A* | 0 | These two constants control the CT phase compensation. No compensation occurs when *PHADJ_X* = 0. As *PHADJ_X* is increased, more compensation (lag) is introduced. Range: $\pm 2^{15}$ – 1. |
| 0x0D | 0x1034 | *PHADJ_B* | 0 | |
| 0x0E | 0x1038 | *APULSEW* | 0 | Watt pulse generator input (see *DIO_PW* bit). The output pulse rate is: *APULSEW* * $F_S$ * $2^{-32}$ * *WRATE* * *X* * $2^{-14}$. This input is buffered and can be loaded during a computation interval. The change will take effect at the beginning of the next interval. |
| 0x0F | 0x103C | *APULSER* | 0 | VAR pulse generator input (see *DIO_PV* bit). The output pulse rate is: *APULSER* * $F_S$*$2^{-32}$ * *WRATE* * *X* * $2^{-14}$. This input is buffered and can be loaded during a computation interval. The change will take effect at the beginning of the next interval. |
| 0x10 | 0x1040 | *CESTATE* | 0x5020 | See description of *CESTATE* below |
| 0x11 | 0x1044 | *WRATE* | 122 | Kh = *VMAX***IMAX**47.1132 / (*In_8***WRATE**$N_{ACC}$*X) Wh/pulse. The default value results in a Kh of 3.2 Wh/pulse when 2520 samples are taken in each accumulation interval (and VMAX=600, IMAX = 208, In_8 = 1, X = 6). |
| 0x12 | 0x1048 | *GAIN_ADJ* | 16384 | Scales all voltage and current inputs. 16384 provides unity gain. |
| 0x13 | 0x104C | *QUANTA* | 0 | This parameter is added to the Watt calculation for element 0 to compensate for input noise and truncation. LSB = (*VMAX***IMAX / In_8*) *7.4162*$10^{-10}$ W |
| 0x14 | 0x1050 | *SAG_THR* | 443000 | The threshold for sag warnings. The default value is equivalent to 80V RMS if VMAX = 600V. The LSB value is VMAX * 4.255*$10^{-7}$V (peak). |
| 0x15 | 0x1054 | *QUANT_VARA* | 0 | This parameter is added to the VAR calculation for element A to compensate for input noise and truncation. |
| 0x16 | 0x1058 | *QUANT_I* | 0 | This parameter is added to compensate for input noise and truncation in the squaring calculations for $I^2$ and $V^2$. |
| 0x18 | 0x1060 | *QUANTB* | 0 | This parameter is added to the Watt calculation for element 1 to compensate for input noise and truncation. Same LSB as *QUANTA*. |
| 0x19 | 0x1064 | *CRV0* | 0 | Smoothing factors for low currents on element 0 and 1. $I_{RMS}$ is the operating RMS current. |
| 0x1A | 0x1068 | *CRV1* | 0 | |
| 0x1B | 0x106C | *QUANT_VARB* | 0 | This parameter is added to the VAR calculation for element B to compensate for input noise and truncation. |

| | | | | |
|---|---|---|---|---|
| 0x75 | 0x11D4 | *VAR0SUM_X* | -- | The sum of VAR samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*). |
| 0x71 | 0x11C4 | *VAR1SUM_X* | | |
| 0x76 | 0x11D8 | *W0SUM_X* | -- | The sum of Watt samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*). |
| 0x72 | 0x11C8 | *W1SUM_X* | | |
| 0x7A | 0x11E8 | *CESTATUS* | | See description of CE status above. |
| 0x7C | 0x11F0 | *MAINEDGE_X* | -- | The number of zero crossings of the selected voltage in the previous accumulation interval. Zero crossings are either direction and are debounced. |
| 0x7B | 0x11EC | *TEMP_RAW_X* | -- | Filtered, unscaled reading from the temperature sensor. |

**Table 1-16: CE Memory Locations (71M6521FE, 71M6521DE)**

## 1.10.6 CE CODE MEMORY LOCATIONS (71M6521BE)

All CE memory locations are listed in the 71M6521BE data sheet. These locations are listed again in Table 1-17, along with the physical addresses used by the hex records interface.

| Physical Address | Name | Default | Description |
|---|---|---|---|
| 0x1020 | *CAL_IA* | 16384 | These constants control the gain of their respective channels. The nominal value for each parameters is $2^{14}$ = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be scaled by 1/(1 – 0.01). |
| 0x1024 | *CAL_VA* | 16384 | |
| 0x1028 | *CAL_IB* | 16384 | |
| 0x102C | *CAL_VB* | 16384 | |
| 0x1030 | *PHADJ_A* | 0 | This constant controls the CT phase compensation. No compensation occurs when *PHADJ_A* = 0. As *PHADJ_A* is increased, more compensation (lag) is introduced. Range: $\pm 2^{15}$ – 1. |
| 0x1034 | *PHADJ_B* | 0 | This constant controls the CT phase compensation. No compensation occurs when *PHADJ_B* = 0. As *PHADJ_B* is increased, more compensation (lag) is introduced. Range: $\pm 2^{15}$ – 1. |
| 0x1038 | -- | -- | Unused |
| 0x103C | -- | -- | Unused |
| 0x1040 | *CESTATE* | 0x5020 | See description of *CESTATE* in the table below |
| 0x1044 | *WRATE* | 389 | Kh = *VMAX**IMAX**47.1132 / (*WRATE**360*$N_{ACC}$) Wh/pulse. The default value results in a Kh of 1.0Wh/pulse when 2520 samples are taken in each accumulation interval (and VMAX=600, IMAX = 208, In_8 = 1). |
| 0x1048 | *GAIN_ADJ* | 16384 | *GAIN_ADJ* is controlled by the temperature compensation mechanism, and scales all voltage and current inputs. 16384 provides unity gain. |
| 0x104C | *QUANTA* | 0 | This parameter is added to the Watt calculation for element 0 to compensate for input noise and truncation. LSB = (*VMAX***IMAX* ) *7.4162*$10^{-10}$ W |
| 0x1050 | *SAG_THR* | 443000 | The threshold for sag warnings. The default value is equivalent to 80V RMS if VMAX = 600V. The LSB value is 80V/443000. |

| | | | |
|---|---|---|---|
| 0x1054 | *DEGSCALE* | 0 | This constant is used for the calculation of *DELTA_T* . |
| 0x1058 | *QUANT_IA* | 0 | This parameter is added to compensate for input noise and truncation in the squaring calculations for $I^2$ |
| 0x105C | *TEMP_NOM* | $7.04*10^7$ | The reference temperature read from MPU location *TEMP_RAW* is stored in this location when the unit is calibrated. |
| 0x1060 | *QUANTB* | 0 | This parameter is added to the Watt calculation for element 1 to compensate for input noise and truncation. Same LSB as *QUANTA*. |
| 0x1064 | *CRV0* | 0 | Smoothing factors for low currents on element 0 and 1.<br>$I_{RMS}$ is the operating RMS current. |
| 0x1068 | *CRV1* | 0 | |
| 0x106C | *QUANT_IB* | 0 | This parameter is added to compensate for input noise and truncation in the squaring calculations for $I^2$ |
| 0x1070 | *CREEP_0* | 8311 | These parameters establish the creep threshold.<br>LSB = $6.6952*10^{-13}$*VMAX*IMAX*3600 W<br>The default values correspond to 2.5 W. |
| 0x1074 | *CREEP_1* | 8311 | |
| 0x1078 | *VNOMINAL* | $1.27*10^8$ | This parameter defines the nominal voltage to be used for the power calculation when tampering is detected.<br>$LSB = \frac{\sqrt{\frac{6.6952 \cdot 10^{-13}}{3600}} VMAX}{2^{14}}$<br>The default value corresponds to 230V, when *VMAX* = 600V |
| 0x107C | *WNOMINAL* | 7,646,277 | This parameter defines the nominal wattage to be used when magnetic tampering is detected.<br>LSB = $6.6952*10^{-13}$*VMAX*IMAX*3600 W |
| 0x1080 | *PPMC1* | +150 | Linear temperature compensation factor. |
| 0x1084 | *PPMC2* | -392 | Quadratic temperature compensation factor. |

**Table 1-17: CE memory locations (71M6521BE)**

The *CESTATE* register, shown in Table 1-18, is used to configure the CE.

| Bit | Significance | Bit | Significance |
|---|---|---|---|
| 0 | *PULSE_SLOW* | 8 | *SAG_CNT[0]* |
| 1 | *PULSE_FAST* | 9 | *SAG_CNT[1]* |
| 2 | *I0_SHUNT* | 10 | *SAG_CNT[2]* |
| 3 | *I1_SHUNT* | 11 | *SAG_CNT[3]* |
| 4 | *MAGNETIC_TAMPER* | 12 | *SAG_CNT[4]* |
| 5 | *NEUTRAL_TAMPER* | 13 | *SAG_CNT[5]* |
| 6 | *FREQSEL* | 14 | *SAG_CNT[6]* |
| 7 | Reserved | 15 | *SAG_CNT[7]* |

**Table 1-18: *CESTATE* Register**

## 1.10.7 SOME MPU CODE MEMORY LOCATIONS (71M6521BE)

There are no *VMAX* and *IMAX* parameters declared in the 6521BE Demo Code. The 6521BE Demo Code does not need these parameters, since it does not display voltage and current RMS values on the LCD. If necessary, the user can derive the values for register variables that depend on *VMAX* and *IMAX* by multiplying the count in the registers with the LSB values given in Table 1-17.

| Physical Address | Name | Default | Description |
|---|---|---|---|
| 0x0000 | *ENERGY* | 0 | Accumulated energy, in 10 BCD-coded bytes.<br>00 01 09 05 03 05 00 02 07 is equivalent to 19535.027Wh<br>When a sag event occurs, a check byte in LRC format is calculated as the 11$^{th}$ byte. |
| 0x019 | *W_PER_P* | 1 | Multiplier for the display of accumulated energy, in 4 BCD-coded bytes. Each pulse will register as the energy defined by *W_PER_P*.<br>00 01 00 00 is equivalent to 100Wh per pulse. |
| 0x001D | *VBAT_MIN* | 0 | Currently unused. This variable may be used to decide when to transfer to sleep mode. |
| 0x0024 | *CAL_CNT* | 0 | Counter for calibrations. |
| 0x0038 | *ACC_INT* | -- | 1-byte counter for completed accumulation intervals. |
| 0x00C0 | *DELTA_T* | -- | This memory location contains the current chip temperature relative to the reference temperature defined by *TEMP_NOM*.<br>LSB = 0.1°C. |
| 0x00C4 | *I1SQRT* | -- | Squared current for channel B. Used for neutral tamper. |
| 0x00C8 | *W1SUM* | -- | This memory location contains the energy value collected in the last accumulation interval for channel B.<br>LSB = $6.6952*10^{-13}*VMAX*IMAX$ Wh |
| 0x00CC | *I1SQSUM* | -- | This memory location contains the sum of the squared current values collected in the last accumulation interval for channel B.<br>LSB = $6.6952*10^{-13}*IMAX^2$ Wh |
| 0x00D4 | *I0SQRT* | -- | Squared current for channel A. Used for neutral tamper. |
| 0x00DC | *I0SQSUM* | | This memory location contains the sum of the squared current values collected in the last accumulation interval for channel A.<br>LSB = $6.6952*10^{-13}*IMAX^2$ Wh |
| 0x00D8 | *W0SUM* | -- | This memory location contains the energy value collected in the last accumulation interval for channel A.<br>LSB = $6.6952*10^{-13}*VMAX*IMAX$ Wh |
| 0x00E4 | *FREQ* | -- | The current frequency of the mains voltage signal. LSB = 1/170,396 |
| 0x00E8 | *CESTATUS* | -- | A copy of the current STATUS word of the CE. |
| 0x00EC | *TEMP_RAW* | -- | The unfiltered, unscaled output of the temperature sensor. |
| 0x00F0 | *MAIN_EDGE* | -- | The number of zero crossings of the mains voltage signal in the last accumulation interval. |
| 0x00F4 | *WSUM_ACC* | -- | Accumulated total energy for in the last accumulation interval for channel A. LSB = $6*6.6952*10^{-13}*VMAX*IMAX$ Wh |
| 0x00FC | *VBAT* | -- | Battery voltage. The *BME* bit in I/O RAM has to be enabled prior to measuring the battery voltage. |

**Table 1-19: Some MPU Memory Locations**

## 1.11 EMULATOR OPERATION

The Signum Systems ADM51 ICE (In-Circuit-Emulator) can be plugged into J14 (or J5) of the Demo Board. The following conditions are required for successful emulator operation (including code load/erase in flash memory):

1) Emulator operation is enabled by plugging a jumper into header JP4, pins V3P3D/ICE_E
2) For loading code into flash, the CE is disabled (using serial command **CE0** or writing 0x00 to XRAM cell 0x2000)

For details on code development and test see the Software User's Guide (SUG).

The emulator can also be operated when the 71M6521 is in brownout mode. In brownout mode, the 71M6521 provides power for the pull-up resistors necessary for emulator operation via its V3P3D pin.

2

# 2 APPLICATION INFORMATION

## 2.1 CALIBRATION THEORY

A typical meter has phase and gain errors as shown by $\phi_S$, $A_{XI}$, and $A_{XV}$ in Figure 2-1. Following the typical meter convention of current phase being in the lag direction, the small amount of phase lead in a typical current sensor is represented as $-\phi_S$. The errors shown in Figure 2-1 represent the sum of all gain and phase errors. They include errors in voltage attenuators, current sensors, and in ADC gains. In other words, no errors are made in the 'input' or 'meter' boxes.

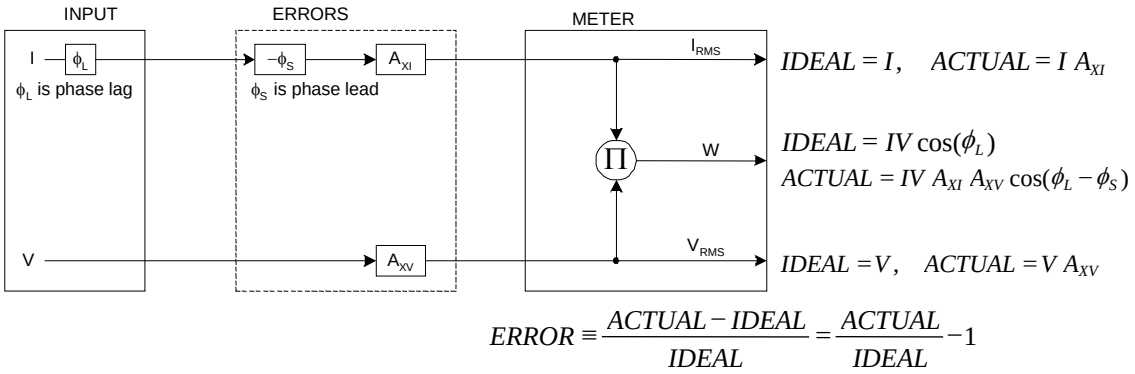



**Figure 2-1: Watt Meter with Gain and Phase Errors.**

During the calibration phase, we measure errors and then introduce correction factors to nullify their effect. With three unknowns to determine, we must make at least three measurements. If we make more measurements, we can average the results.

### 2.1.1 CALIBRATION WITH THREE MEASUREMENTS

A simple calibration method uses three measurements. Typically, a voltage measurement and two Watt-hour (Wh) measurements are made. A voltage display can be obtained for test purposes via the command >**MR2.1** in the serial interface.

Let's say the voltage measurement has the error $E_V$ and the two Wh measurements have errors $E_0$ and $E_{60}$, where $E_0$ is measured with $\phi_L = 0$ and $E_{60}$ is measured with $\phi_L = 60$. These values should be simple ratios—not percentage values. They should be zero when the meter is accurate and negative when the meter runs slow. The fundamental frequency is $f_0$. T is equal to $1/f_S$, where $f_S$ is the sample frequency (2560.62Hz). Set all calibration factors to nominal: *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

From the voltage measurement, we determine that

1.➔ $$A_{XV} = E_V + 1$$

We use the other two measurements to determine $\phi_S$ and $A_{XI}$.

2. $$E_0 = \frac{IV\, A_{XV}\, A_{XI} \cos(0 - \phi_S)}{IV \cos(0)} - 1 = A_{XV}\, A_{XI} \cos(\phi_S) - 1$$

2a. $$A_{XV} A_{XI} = \frac{E_0 + 1}{\cos(\phi_S)}$$

3. $$E_{60} = \frac{IV\, A_{XV}\, A_{XI} \cos(60 - \phi_S)}{IV \cos(60)} - 1 = A_{XV}\, A_{XI} \frac{\cos(60 - \phi_S)}{\cos(60)} - 1$$

3a. $$E_{60} = \frac{A_{XV} A_{XI} \left[\cos(60)\cos(\phi_S) + \sin(60)\sin(\phi_S)\right]}{\cos(60)} - 1$$

$$= A_{XV} A_{XI} \cos(\phi_S) + A_{XV} A_{XI} \tan(60)\sin(\phi_S) - 1$$

Combining 2a and 3a:

4. $$E_{60} = E_0 + (E_0 + 1)\tan(60)\tan(\phi_S)$$

5. $$\tan(\phi_S) = \frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}$$

6.➔ $$\phi_S = \tan^{-1}\left(\frac{E_{60} - E_0}{(E_0 + 1)\tan(60)}\right)$$

and from 2a:

7.➔ $$A_{XI} = \frac{E_0 + 1}{A_{XV} \cos(\phi_S)}$$

Now that we know the $A_{XV}$, $A_{XI}$, and $\phi_S$ errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from $\phi_S$, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1 - 2^{-9})^2 - 2(1 - 2^{-9})\cos(2\pi f_0 T)\right]}{(1 - 2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1 - 2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1+\frac{2^{-20}\,PHADJ\,(2+2^{-20}\,PHADJ-2(1-2^{-9})\cos(2\pi f_0 T))}{1-2(1-2^{-9})\cos(2\pi f_0 T)+(1-2^{-9})^2}}}$$

## 2.1.2 CALIBRATION WITH FIVE MEASUREMENTS

The five measurement method provides more orthogonality between the gain and phase error derivations. This method involves measuring $E_V$, $E_0$, $E_{180}$, $E_{60}$, and $E_{300}$. Again, set all calibration factors to nominal, i.e. *CAL_IA* = 16384, *CAL_VA* = 16384, *PHADJA* = 0.

First, calculate $A_{XV}$ from $E_V$:

1.➔ $$A_{XV} = E_V + 1$$

Calculate $A_{XI}$ from $E_0$ and $E_{180}$:

2. $$E_0 = \frac{IV\,A_{XV}\,A_{XI}\cos(0-\phi_S)}{IV\cos(0)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$$

3. $$E_{180} = \frac{IV\,A_{XV}\,A_{XI}\cos(180-\phi_S)}{IV\cos(180)} - 1 = A_{XV}\,A_{XI}\cos(\phi_S) - 1$$

4. $$E_0 + E_{180} = 2A_{XV}A_{XI}\cos(\phi_S) - 2$$

5. $$A_{XV}A_{XI} = \frac{E_0 + E_{180} + 2}{2\cos(\phi_S)}$$

6.➔ $$A_{XI} = \frac{(E_0 + E_{180})/2 + 1}{A_{XV}\cos(\phi_S)}$$

Use above results along with $E_{60}$ and $E_{300}$ to calculate $\phi_S$.

7. $$E_{60} = \frac{IV\,A_{XV}\,A_{XI}\cos(60-\phi_S)}{IV\cos(60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) + A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

8. $$E_{300} = \frac{IV\,A_{XV}\,A_{XI}\cos(-60-\phi_S)}{IV\cos(-60)} - 1$$

$$= A_{XV}A_{XI}\cos(\phi_S) - A_{XV}A_{XI}\tan(60)\sin(\phi_S) - 1$$

Subtract 8 from 7

9. $$E_{60} - E_{300} = 2A_{XV}A_{XI}\tan(60)\sin(\phi_S)$$

use equation 5:

10. $$E_{60} - E_{300} = \frac{E_0 + E_{180} + 2}{\cos(\phi_S)}\tan(60)\sin(\phi_S)$$

11. $$E_{60} - E_{300} = (E_0 + E_{180} + 2)\tan(60)\tan(\phi_S)$$

12.➔ $$\phi_S = \tan^{-1}\left(\frac{(E_{60} - E_{300})}{\tan(60)(E_0 + E_{180} + 2)}\right)$$

Now that we know the $A_{XV}$, $A_{XI}$, and $\phi_S$ errors, we calculate the new calibration voltage gain coefficient from the previous ones:

$$CAL\_V_{NEW} = \frac{CAL\_V}{A_{XV}}$$

We calculate PHADJ from $\phi_S$, the desired phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T) - \tan(\phi_S)\left[1 - (1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

And we calculate the new calibration current gain coefficient, including compensation for a slight gain increase in the phase calibration circuit.

$$CAL\_I_{NEW} = \frac{CAL\_I}{A_{XI}} \frac{1}{\sqrt{1 + \frac{2^{-20} PHADJ(2 + 2^{-20} PHADJ - 2(1-2^{-9})\cos(2\pi f_0 T))}{1 - 2(1-2^{-9})\cos(2\pi f_0 T) + (1-2^{-9})^2}}}$$

### 2.1.3 FAST CALIBRATION

A very fast calibration process can be implemented by offering a known voltage and current at exactly zero degree phase angle to the meter. If the meter is exposed to the current and voltage source for a known integer number of accumulation intervals, the accumulated real (Wh) and reactive (VARh) energy values along with the accumulated voltage ($V^2h$) can be used to determine the calibration factors quickly.

Another advantage of this method is that no pulse counts are necessary, since the energy accumulation values are directly accessible via their associated registers in the Demo Code.

The phase angle can be directly calculated from the inverse tangens of the ratio of reactive and real energy:

$$\phi_S = \tan^{-1}\left(\frac{Q}{P}\right)$$

The energy quantities are directly available as the values read from the accumulation registers ($n_Q$, $n_P$) multiplied with the LSB value, which is the product of the LSB of the CE and the VMAX and IMAX design constants:

$Q = n_Q * LSB = n_Q * IMAX * VMAX * LSB_{CE}$

$P = n_P * LSB = n_P * IMAX * VMAX * LSB_{CE}$

The accumulated voltage ($V^2h$) is available as the value read from its accumulation register multiplied with its LSB value:

$$V = n_V \cdot LSB = 3.761 \cdot 10^{-8} \frac{n_V}{\sqrt{PRE\_SUM \cdot SUM\_CYCLES}}$$

As in the methods described before, we can determine the voltage error from:

$$A_{XV} = E_V + 1$$

As in the methods described before, we calculate PHADJ from $\phi_S$, the determined phase lag:

$$PHADJ = 2^{20}\left[\frac{\tan(\phi_S)\left[1+(1-2^{-9})^2-2(1-2^{-9})\cos(2\pi f_0 T)\right]}{(1-2^{-9})\sin(2\pi f_0 T)-\tan(\phi_S)\left[1-(1-2^{-9})\cos(2\pi f_0 T)\right]}\right]$$

The correction factor for the current is determined by:

$$CAL\_IA = \frac{\cos\left(\frac{\phi_S P_{app}}{P_m}\right)}{CAL\_VA}$$

## 2.2 CALIBRATION PROCEDURES

### 2.2.1 GENERAL PRECAUTIONS

Calibration requires that a calibration system is used, i.e. equipment that applies accurate voltage, load current and load angle to the unit being calibrated, while measuring the response from the unit being calibrated in a repeatable way. By repeatable we mean that the calibration system is synchronized to the meter being calibrated. Best results are achieved when the first pulse from the meter opens the measurement window of the calibration system. This mode of operation is opposed to a calibrator that opens the measurement window at random time and that therefore may or may not catch certain pulses emitted by the meter.

**It is essential for a valid meter calibration to have the voltage stabilized a few seconds before the current is applied. This enables the Demo Code to initialize the 71M6521 and to stabilize the PLLs and filters in the CE. This method of operation is consistent with meter applications in the field as well as with metering standards.**

Each meter phase must be calibrated individually. The procedures below show how to calibrate a meter phase with either three or five measurements. The PHADJ equations apply only when a current transformer is used for the phase in question. Note that positive load angles correspond to lagging current (see Figure 2-2).

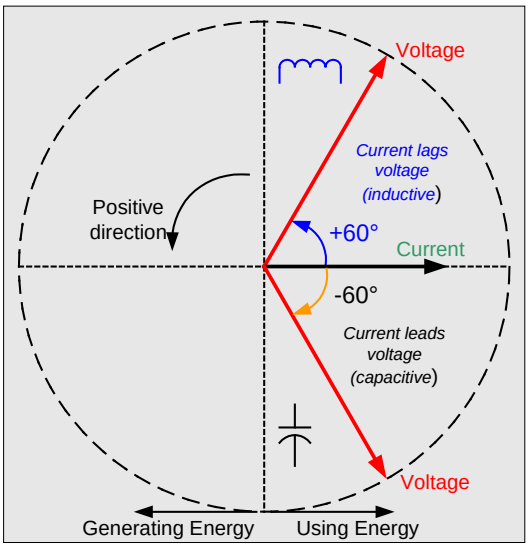



**Figure 2-2: Phase Angle Definitions**

The calibration procedures described below should be followed after interfacing the voltage and current sensors to the 71M6521 chip. When properly interfaced, the V3P3 power supply is connected to the meter neutral and is the DC reference for each input. Each voltage and current waveform, as seen by the 6521, is scaled to be less than 250mV (peak).

## 2.2.2 CALIBRATION PROCEDURE WITH THREE MEASUREMENTS

The calibration procedure is as follows:

1. All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.
2. An RMS voltage $V_{ideal}$ consistent with the meter's nominal voltage is applied, and the RMS reading $V_{actual}$ of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$
3. Apply the nominal load current at phase angles 0° and 60°, measure the Wh energy and record the errors $E_0$ AND $E_{60}$.
4. Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.1 or using the spreadsheet presented in section 2.2.4.
5. Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.
6. Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.
7. Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the EEPROM of the meter. If a Demo Board is calibrated, the methods shown in section 1.9.2 can be used.

## 2.2.3 CALIBRATION PROCEDURE WITH FIVE MEASUREMENTS

The calibration procedure is as follows:

1) All calibration factors are reset to their default values, i.e. CAL_IA = CAL_VA = 16384, and PHADJ_A = 0.
2) An RMS voltage $V_{ideal}$ consistent with the meter's nominal voltage is applied, and the RMS reading $V_{actual}$ of the meter is recorded. The voltage reading error Axv is determined as

   $Axv = (V_{actual} - V_{ideal}) / V_{ideal}$
3) Apply the nominal load current at phase angles 0°, 60°, 180° and –60° (-300°). Measure the Wh energy each time and record the errors $E_0$, $E_{60}$, $E_{180}$, and $E_{300}$.

4) Calculate the new calibration factors CAL_IA, CAL_VA, and PHADJ_A, using the formulae presented in section 2.1.2 or using the spreadsheet presented in section 2.2.4.

5) Apply the new calibration factors CAL_IA, CAL_VA, and PHADJ_A to the meter. The memory locations for these factors are given in section 1.9.1.

6) Test the meter at nominal current and, if desired, at lower and higher currents and various phase angles to confirm the desired accuracy.

7) Store the new calibration factors CAL_IA, CAL_VA, and PHADJ_A in the EEPROM of the meter. If the calibration is performed on a TERIDIAN Demo Board, the methods shown in sections 1.9.2 can be used.

### 2.2.4 PROCEDURE FOR FAST CALIBRATION

The calibration procedure is as follows:

1) Establish load voltage and current. The load angle must be exactly 0.00 degrees.

2) Wait 2 seconds.

3) Clear the accumulators (e.g. with CLI command **)1=2** )

4) Wait 30 seconds.

5) Disable the CE (e.g. with CLI command **CE0**)

6) Read accumulated values from MPU RAM registers and enter these in the spreadsheet supplied on the Demo Kit CD-ROM. Use the addresses as listed in Table 1-13. Enter applied voltage and current as well as the number of completed accumulation intervals in the spreadsheet.

7) Apply the measured IC temperature in register accessible at )14..

### 2.2.5 CALIBRATION SPREADSHEETS

Calibration spreadsheets are available from TERIDIAN Semiconductor. They are also included in the CD-ROM shipped with any Demo Kit. Figure 2-3 shows the spreadsheet for three measurements with three phases in use (only one phase needs to be used for the 71M6521 chip).

Figure 2-3 shows the spreadsheet for five measurements with three phases (only one phase needs to be used for the 71M6521 chip).

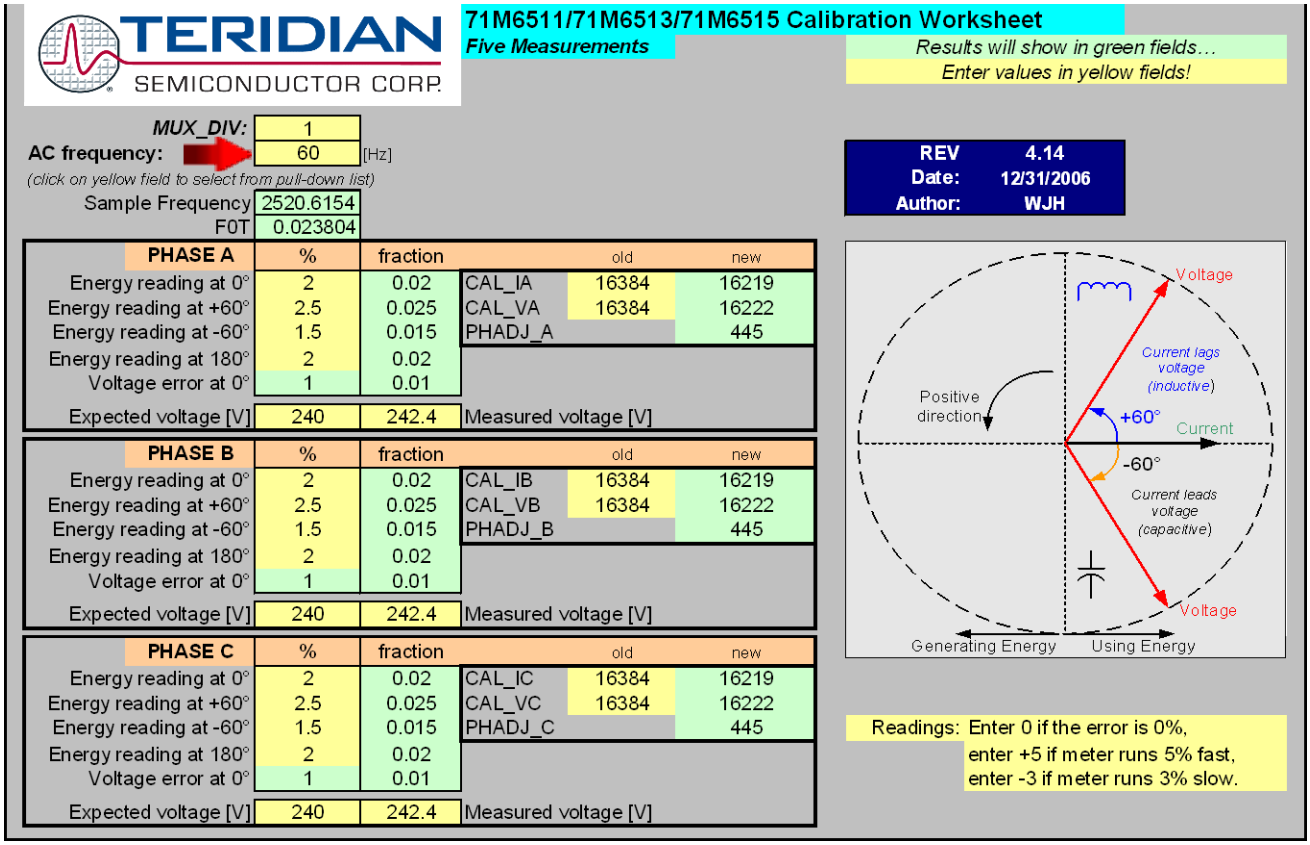



**Figure 2-3: Calibration Spreadsheet for Three Measurements**

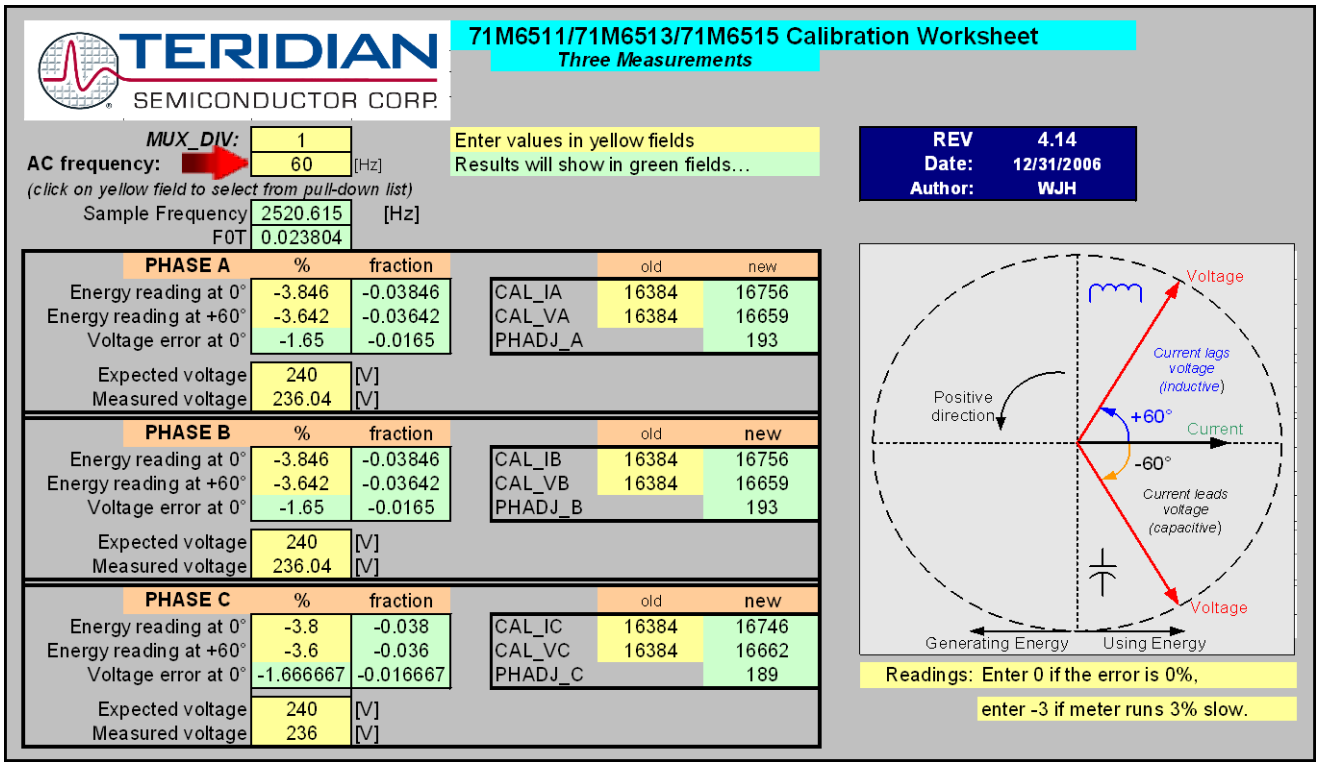



**Figure 2-4: Calibration Spreadsheet for Five Measurements**

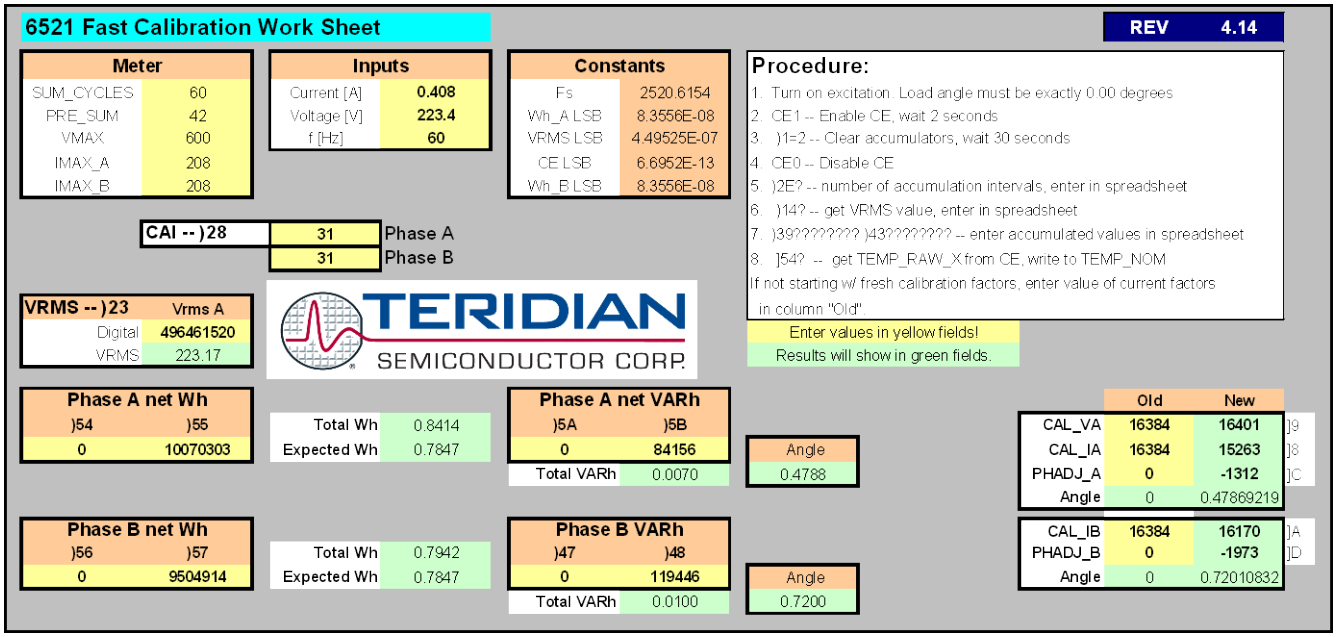



**Figure 2-5: Calibration Spreadsheet for Fast Calibration**

## 2.2.6 COMPENSATING FOR NON-LINEARITIES

Nonlinearity is most noticeable at low currents, as shown in Figure 2-6, and can result from input noise and truncation. Nonlinearities can be eliminated using the *QUANT* variable.

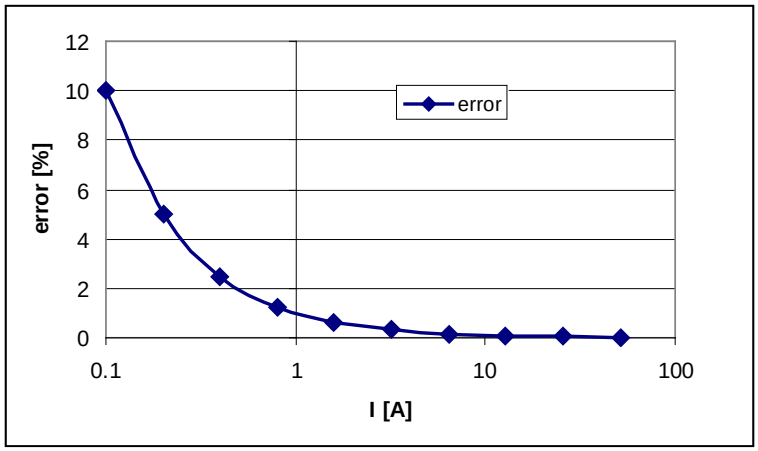



**Figure 2-6: Non-Linearity Caused by Quantification Noise**

The error can be seen as the presence of a virtual constant noise current. While 10mA hardly contribute any error at currents of 10A and above, the noise becomes dominant at small currents.

The value to be used for *QUANT* can be determined by the following formula:

$$QUANT = -\frac{\frac{error}{100} V \cdot I}{VMAX \cdot IMAX \cdot LSB}$$

Where error = observed error at a given voltage (V) and current (I),
VMAX = voltage scaling factor, as described in section 1.8.2,
IMAX = current scaling factor, as described in section 1.8.2,

LSB = *QUANT* LSB value = $7.4162*10^{-10}$W

**Example:** Assuming an observed error as in Figure 2-6, we determine the error at 1A to be +1%. If *VMAX* is 600V and *IMAX* = 208A, and if the measurement was taken at 240V, we determine *QUANT* as follows:

$$QUANT = -\frac{\frac{1}{100}240 \cdot 1}{600 \cdot 208 \cdot 7.4162 \cdot 10^{-10}} = -11339$$

*QUANT* is to be written to the CE location 0x2F. It does not matter which current value is chosen as long as the corresponding error value is significant (5% error at 0.2A used in the above equation will produce the same result for *QUANT*).

An alternative method for obtaining *QUANT* is as follows:

*WnSUM* holds an energy value with an LSB equal to $6.6952 * 10^{-13}$ VMAX IMAX Wh. The LSB for *QUANT* is not an energy value but a power value, and is $7.4162 * 10^{-10}$ W. If I divide the *QUANT* LSB by 3600, we get $2.06 * 10^{-13}$ Wh per accumulation interval (assuming an interval of 1000 ms), which is a factor 3.25 less than the LSB of *WnSUM*. This factor is due to the fact that *QUANT* is added in the CE signal flow before the summation to get *WnSUM*. In order to equate it to the *WnSUM* LSB, we need to correct the *QUANT* LSB by

$F_s*2^{-13}*3600$,

where $F_s$ is the sampling frequency (2520 Hz for standard demo code). This means that the value obtained from *WnSUM* needs to be scaled up by 1107.422 to get the corresponding value for *QUANT*.

**Example:** In *WASUM*, an average noise of 4 LSBs is observed while no current is flowing in phase A. The corresponding value to be placed in *QUANT* then calculates to:

*QUANT* = 1107.422 * 4 = 4429.7, which should be rounded up to 4430.

Input noise and truncation can cause similar errors in the VAR calculation that can be eliminated using the *QUANT_VAR* variable. *QUANT_VAR* is determined using the same formula as *QUANT*.

## 2.2.7 CALIBRATING METERS WITH COMBINED CT AND SHUNT RESISTOR

In many cases it is desirable to discourage tampering by using two current sensors. The simple tampering method that involves connecting the low side of the load to earth ground (neutral) can be detected by adding a second current sensor in the neutral path, as shown in Figure 2-7.

In this configuration, the shunt resistor is connected to the IA channel while the current transformer is connected to the IB channel of the 71M6521.

Calibrating this arrangement requires a few extra steps above the regular calibration. The calibration procedure applies to the sensor arrangement described above (SHUNT = IA, CT = IB).

**Preparation:**

1. Set the meter equation field of the configuration RAM for *EQU* to zero using the command:
2. **RI00 = 10** // *EQU* = 0; *CE_EN* =1; *TMUX* = 0;
3. For the sake of calculation, individual *WRATE* parameters for Pulse generation, i.e. *WRATE_SHUNT* and *WRATE_CT* will be used.
4. It is also necessary to compute and estimate *IMAX_SHUNT* and *IMAX_CT* parameters for meter billing purposes.
5. Using *IMAX_SHUNT* and *VMAX*, the energy calculations for channel A should be performed.
6. The energy calculations for channel B should be performed using *IMAX_CT* and *VMAX*.
7. The LSB values for measurements for *W0SUM / W1SUM/ VAR0SUM/ VAR1SUM/ I0SQSUM/ I1SQSUM/ V0SQSUM* should be modified to compute the correct energy values. That is, *IMAX_SHUNT* and *IMAX_CT* should be applied separately to individual channels based on the sensor connections.
8. Before starting a calibration, all calibration factors must be in their default state, i.e. *CAL_IA* (0x08), *CAL_VA* (0x09), *CAL_IB* (0x0A) must be 16384. *PHADJ_A* (0x0E) and *PHADJ_B* (0x0F) should be zero.

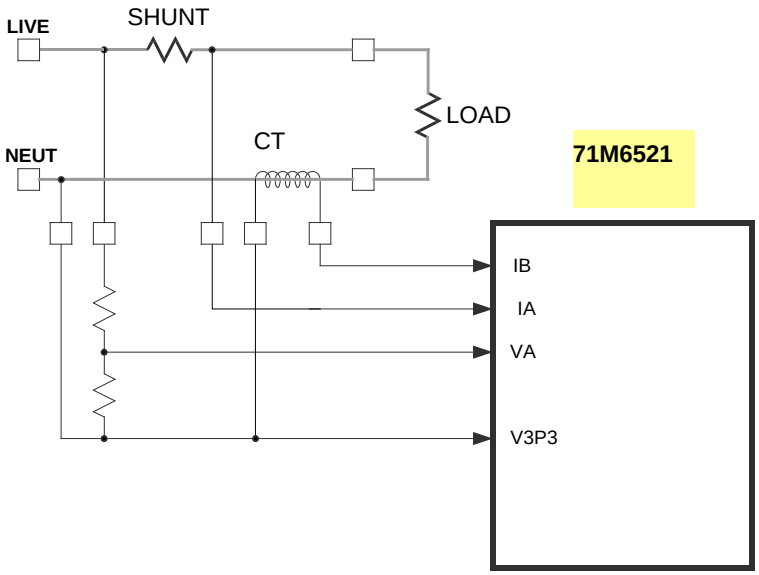



**Figure 2-7: 71M6521 with Shunt and CT**

**Calibrating for Shunt Resistor (Channel A):**

1. Calculate *IMAX* for the shunt resistor (*IMAX_SHUNT*). This can be done by using the following formula:

   *IMAX_SHUNT* = $Vi_{MAX}/R_{SH}$

   The $Vi_{MAX}$ value is the maximum analog input voltage for the channel, typically 177mV (RMS), and $R_{SH}$ is the resistance value of the shunt resistor.
   The value obtained for *IMAX_SHUNT* is stored at the MPU address 0x0A, using the command **)A=** *IMAX_SHUNT* of the Demo Code supplied by TERIDIAN.

2. Compute *WRATE_SHUNT* based on *IMAX_SHUNT* and *VMAX* and the formula given in 1.8.2:

   *WRATE_SHUNT* = (*IMAX_SHUNT* * *VMAX* * 47.1132) / (Kh * In_8 * $N_{ACC}$ * X)

   Use *VMAX* = 600V (RMS) for the 6521 Demo Board if the resistor divider for VA has not been changed.

3. Update the *WRATE* register (at CE address 0x11) with *WRATE_SHUNT*, using the command **]11=** *WRATE_SHUNT.*

4. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

5. Apply the error values to the calibration spreadsheet (revision 2.0 or later) and determine the calibration factors for channel A, i.e. *CAL_IA*, *CAL_VA*, and *PHADJ_A*.

6. Update the CE registers 0x08, 0x09 and 0x0E of the compute engine with the calibration factors obtained from the spreadsheet, using the commands **]8=***CAL_IA*, **]9=***CAL_VA*, and **]E=***PHADJ_A*.

7. Retest for accuracy at several currents and phase angles.

At this point, channel A is calibrated. *WSUM* will be based on the voltage applied to the meter and the current flowing through the shunt resistor. The pulses generated will be based on the parameters entered for channel A.

**Calibration for CT (Channel B):**

1. Compute *IMAX* for the CT channel (*IMAX_CT*), based on the CT turns ratio N and the termination resistor value $R_T$ using the formula:

   *IMAX_CT* = 177mV* N / $R_T$

   This value is used in the following step as *IMAX_CT*.

2. Compute *WRATE_CT* based on the values obtained for *IMAX_CT* and the formula given in 1.8.2:

   *WRATE_CT* = (*IMAX_CT* * *VMAX* * 47.1132) / (Kh * In_8 * $N_{ACC}$ * X)

3. Update the *WRATE* register (CE address 0x11) with *WRATE_CT*, using the command **]11=** *WRATE_CT.*

4. Enter the command **>)7=2.** Configure *W1SUM* as external pulse source since the CT is connected to Channel 1 for VA*IB.

5. Test for accuracy at 15A, 240V at phase angle 0, phase angle 60° and at phase angle –60°.

6. Apply these values to the calibration spread sheet (revision 2.0 or later) and derive the calibration factor *PHADJ_B*.

7. Update only the CE address 0x0F with the value for *PHADJ_B* using the command **]F=** *PHADJ_B.*

8. Adjust *CAL_IB* for the total error found in the accuracy test using the formula

   *CAL_IB* = 16384 * (1 - error/100)

   That is, if the chip reports an error of -2.5%, *CAL_IB* should be adjusted to a value of

   (16384 * (1 - (-2.5/100)).

9. Since *CAL_VA* and *CAL_IA* have already been adjusted for channel A, these registers should not be updated.

10. Retest for accuracy at several currents and phase angles.

After completing the calibration, the energy values W0SUM, based on VA*IA and W1SUM, based on VA*IB are accessible to the MPU firmware. The pulse rate is controlled by *W1SUM* and determined by the parameters selected for the CT channel (VA, IB). Differences between *W0SUM* and *W1SUM*, indicating tampering, can be detected by the MPU for each accumulation interval.

**The User has to customize the Demo Code to utilize the values obtained from the VA, IA, and IB channels for proper calculation of tariffs.**

Table 2-1 summarizes the important parameters used in the calibration procedure.

| Channel | Sensor | Formula | Parameters | W Pulse Generation | VAR Pulse Generation |
|---|---|---|---|---|---|
| A | Shunt Resistor | *WASUM* = VA*IA<br>*VARASUM* = VA*IA | *VMAX* = VMAX<br>*IMAX* = IMAX_SHUNT<br>*WRATE* = WRATE_SHUNT | *WASUM* | *VARASUM* |
| B | CT | *WBSUM* = VA*IB<br>*VARBSUM* = VA*IB | *VMAX* = VMAX<br>*IMAX* = IMAX_CT<br>*WRATE* = WRATE_CT | *WBSUM* | *VARBSUM* |

**Table 2-1: Calibration Summary**

## 2.3 SCHEMATIC INFORMATION

In this section, hints on proper schematic design are provided that will help designing circuits that are functional and sufficiently immune to EMI (electromagnetic interference).

### 2.3.1 COMPONENTS FOR THE V1 PIN

A voltage divider should be used to establish that V1 is in a safe range when the meter is in mission mode (V1 must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled). The header shown above R1 in Figure 2-8 can be used to disable the hardware watchdog timer by plugging in a shorting jumper.

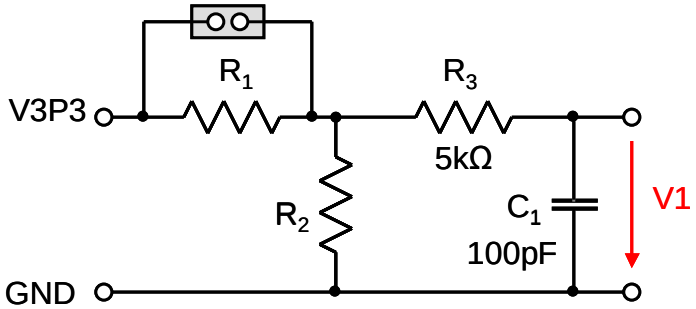



**Figure 2-8: Voltage Divider for V1**

On the 6521 Demo Boards this feature is implemented with resistors R83/R86 and TP10. See the board schematics in the Appendix for details.

### 2.3.2 OSCILLATOR

The oscillator of the 71M6521 drives a standard 32.768kHz watch crystal (see Figure 2-9). Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the 71M6521 has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

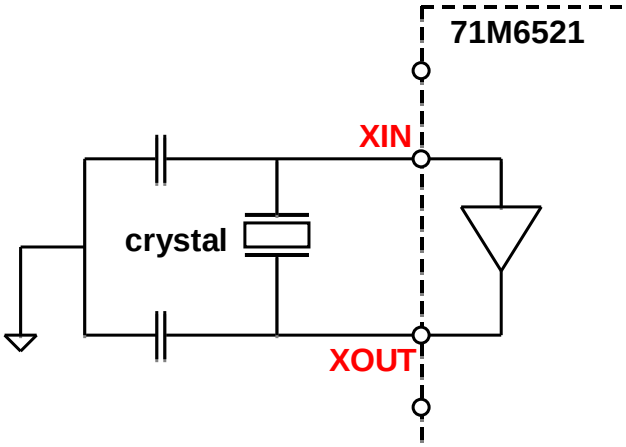



**Figure 2-9: Oscillator Circuit**

### 2.3.3 EEPROM

EEPROMs should be connected to the pins DIO4 and DIO5 (see Figure 2-10). These pins can be switched from regular DIO to implement an I2C interface by setting the I/O RAM register DIO_EEX (0x2008[4]) to 1. Pull-up resistors of 3kΩ must be provided for both the SCL and SDA signals.

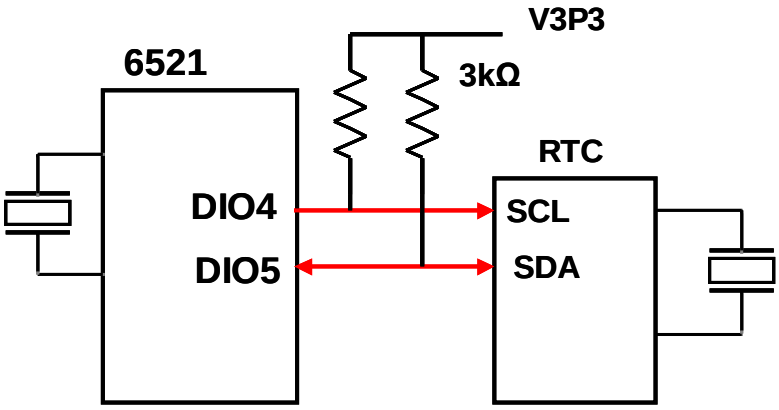



**Figure 2-10: EEPROM Circuit**

### 2.3.4 CONNECTING THREE-WIRE EEPROMS

µWire EEPROMs and other compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 2-11. DIO5 connects to both the DI and DO pins of the three-wire device. The CS pin must be connected to a vacant DIO pin of the 71M6521. A pull-up resistor of roughly 3kΩ to V3P3 should be used for the DI/DO signals, and the CS pin should be pulled down with a resistor to prevent that the three-wire device is selected on power-up, before the 71M6521 can establish a stable signal for CS. The *DIO_EEX* register in I/O RAM must be set to 10 in order to convert the DIO pins DIO4 and DIO5 to uWire pins. The pull-up resistor for DIO5 may not be necessary.

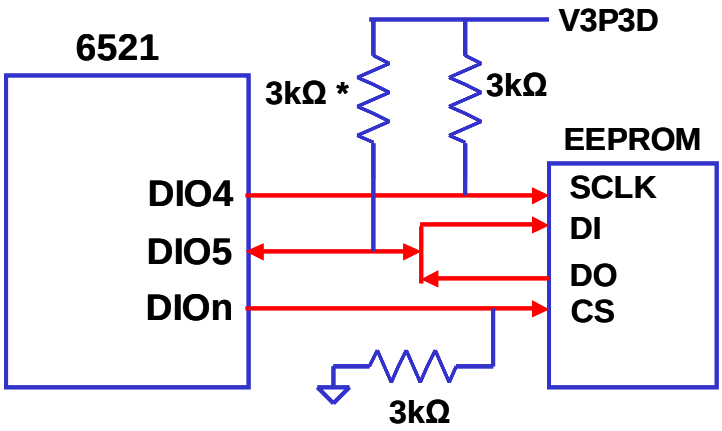



**Figure 2-11: Three-Wire EEPROM Circuit**

### 2.3.5 LCD

The 71M6521 has an on-chip LCD controller capable of controlling static or multiplexed LCDs. Figure 2-12 shows the basic connection for LCDs. Note that the LCD module itself has no power connection.

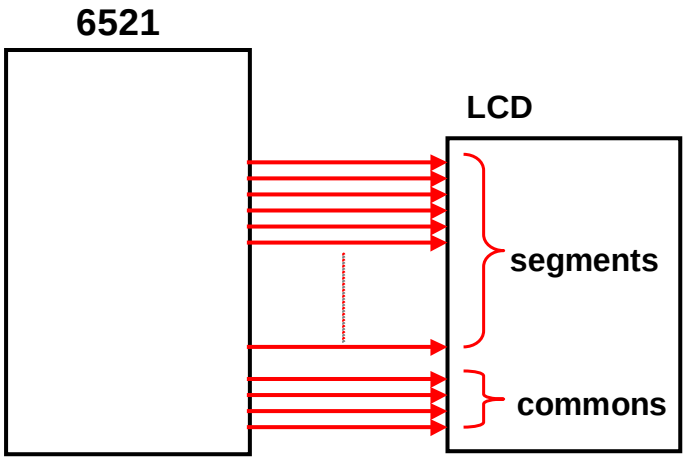



**Figure 2-12: LCD Connections**

### 2.3.6 OPTICAL INTERFACE

The 71M6521 IC is equipped with two pins supporting the optical interface: OPT_TX and OPT_RX. The OPT_TX pin can be used to drive a visual or IR light LED with up to 20mA, a series resistor ($R_2$ in Figure 2-13) helps limiting the current). The OPT_RX pin can be connected to the collector of a photo-transistor, as shown in Figure 2-13.

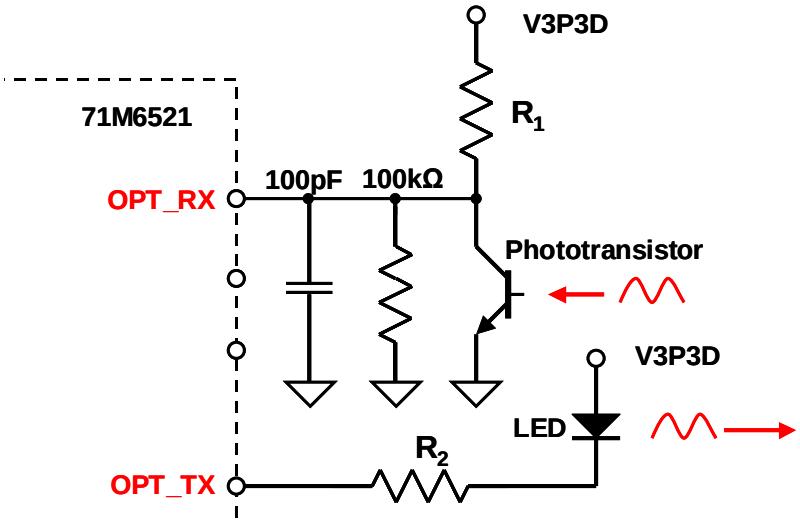



**Figure 2-13: Optical Interface Block Diagram**

J12 on the Demo Boards has all the provisions for connecting the IR LED and photo-transistor (see Figure 2-14). Depending on the required LED current, R79 may have to be scaled. Similarly, R84 may be scaled or removed, depending on the current generated by the photo-transistor.

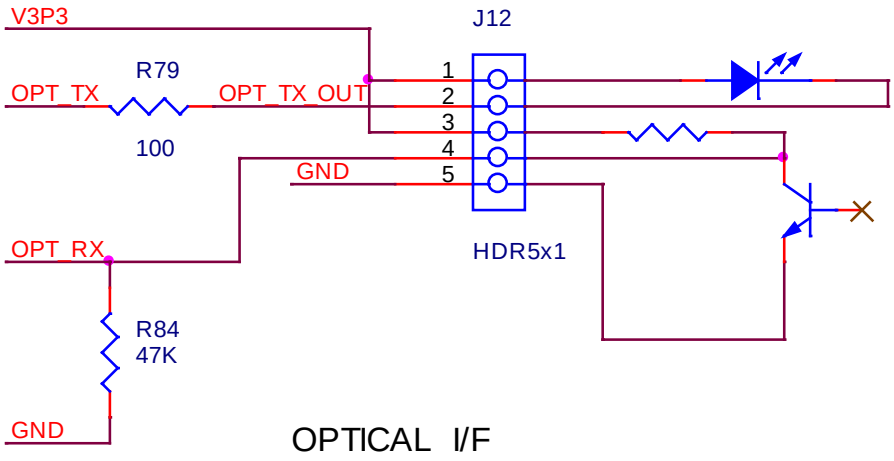



**Figure 2-14: Optical Port Circuitry on the Demo Board**

## 2.3.7 RESET AND PB SWITCHES

If not used, the RESET and PB pins should be connected to DGND either directly or via a resistor, as shown in Figure 2-15. This ensures good EMI performance. If RESET has to be enabled for testing, $R_1$ has to be removed.

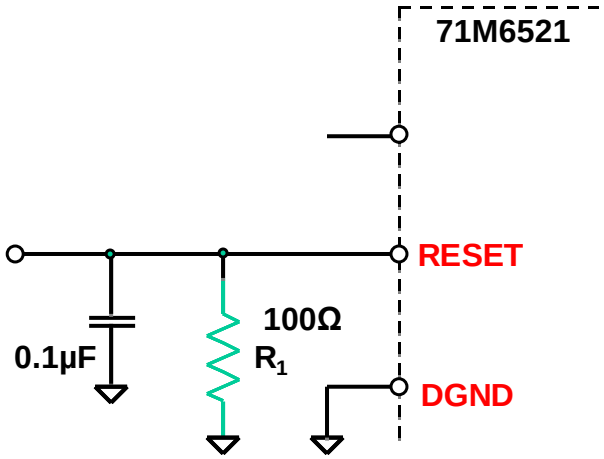



**Figure 2-15: RESET pin, disabled**

If the RESET and PB pins are to be used in the battery modes, care must be taken to ensure proper supply of the associated switches. In most cases, it is sufficient to supply RESET and PB with a voltage from the battery, as shown in Figure 2-16.

Some of the Demo Boards have dual supply options, since they may be operated with or without a battery. In these cases, the voltage to the switches may be supplied from two sources: VBAT and V3P3 (see Figure 2-17). In sleep and LCD mode, VBAT supplies voltage to the switch. When the battery is not installed, V3P3 enables the switch in mission and brownout mode.

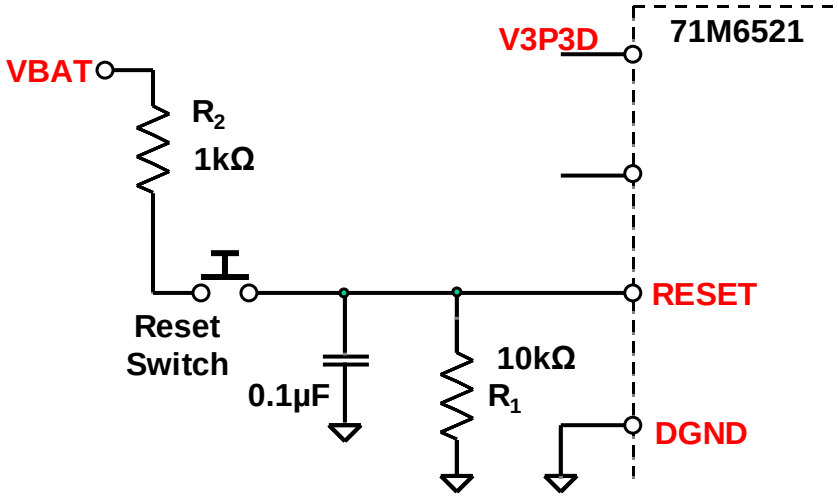



**Figure 2-16: RESET Switch Supplied by VBAT**

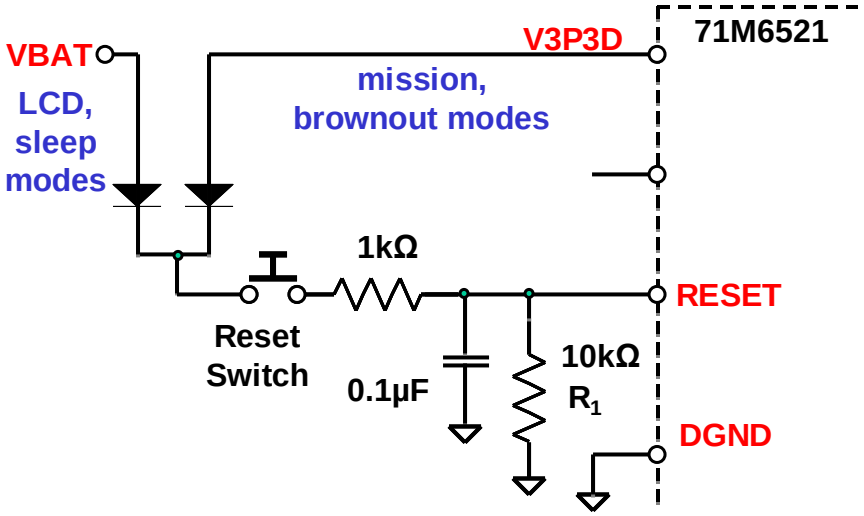



**Figure 2-17: RESET Switch with Multiple Supplies**

### 2.3.8 OPERATION WITH BATTERIES

Some types of meters are equipped with batteries, mostly to support TOU (time-of-use) functions. In these meters the battery maintains the oscillator circuit and the RTC, when board power is not present.

Many meter manufacturers assemble the meter PCB with the 71M6521 IC and the other electronic components first and then join the meter PCB with the meter enclosure, sensors and other main components separately at a later production step. Typically, final test (ATE), and calibration is performed after this second step.

Programming of the flash memory and insertion of a battery may happen at intermediate steps.

**To prevent battery drainage, it is essential that the code is written to permit transition to sleep mode immediately after the battery is inserted into the meter PCB.**

## 2.4 TESTING THE DEMO BOARD

This section will explain how the 71M6521 IC and the peripherals can be tested. Hints given in this section will help evaluating the features of the Demo Board and understanding the IC and its peripherals.

### 2.4.1 FUNCTIONAL METER TEST

This is the test that every Demo Board has to pass before being integrated into a Demo Kit. Before going into the functional meter test, the Demo Board has already passed a series of bench-top tests, but the functional meter test is the first test that applies realistic high voltages (and current signals from current transformers) to the Demo Board.

Figure 2-18 shows a meter connected to a typical calibration system. The calibrator supplies calibrated voltage and current signals to the meter. It should be noted that the current flows through the CT or CTs that are not part of the Demo Board. The Demo Board rather receives the voltage output signals from the CT. An optical pickup senses the pulses emitted by the meter and reports them to the calibrator. Some calibration systems have electrical pickups. The calibrator measures the time between the pulses and compares it to the expected time, based on the meter Kh and the applied power.

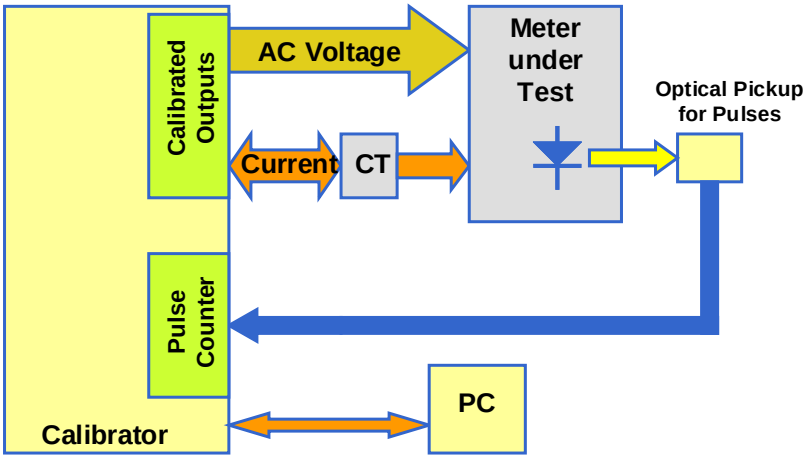



**Figure 2-18: Meter with Calibration System**

TERIDIAN Demo Boards are not calibrated prior to shipping. However, the Demo Board pulse outputs are tested and compared to the expected pulse output. Figure 2-19 shows the screen on the controlling PC for a typical Demo Board. The number in the red field under "As Found" represents the error measured for phase A, whereas the number in the red field under "As Left" represents the error measured for phase B. Both numbers are given in percent. This means that for the measured Demo Board, the sum of all errors resulting from tolerances of PCB components, CTs, and 71M6521 tolerances was –2.8% and –3.8%, a range that can easily be compensated by calibration.

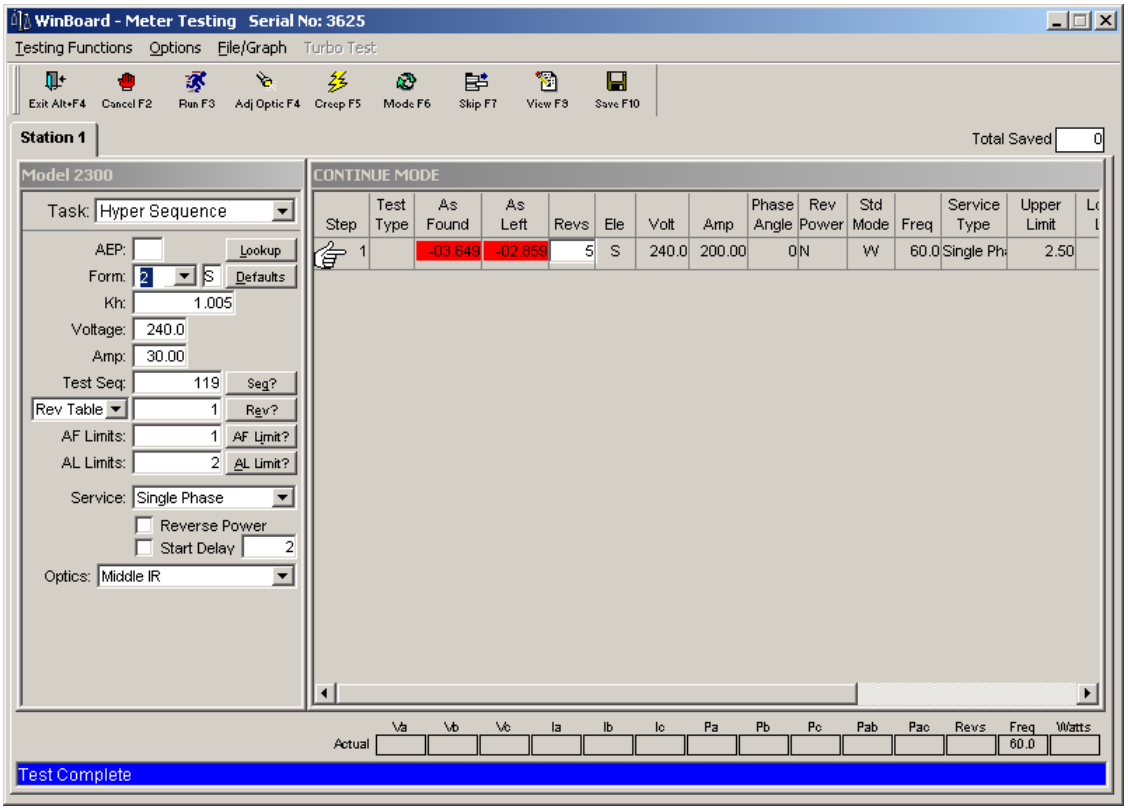



**Figure 2-19: Calibration System Screen**

## 2.4.2 EEPROM

Testing the EEPROM provided on the Demo Board is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To write a string of text characters to the EEPROM and read it back, we apply the following sequence of CLI commands:

**>EEC1** Enables the EEPROM

**>EESthis is a test** Writes text to the buffer

**>EET80** Writes buffer to address 80

**Written to EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….**

Response from Demo Code

**>EER80.E** Reads text from the buffer

**Read from EEPROM address 00000080 74 68 69 73 20 69 73 20 61 ….**

Response from Demo Code

**>EEC0** Disables the EEPROM

### 2.4.3 RTC

Testing the RTC inside the 71M6521 IC is straightforward and can be done using the serial command line interface (CLI) of the Demo Code.

To set the RTC and check the time and date, we apply the following sequence of CLI commands:

| | |
|---|---|
| >**M10** | LCD display to show calendar date |
| >**RTD05.09.27.3** | Sets the date to 9/27/2005 (Tuesday) |
| >**M9** | LCD display to show time of day |
| >**RTT10.45.00** | Sets the time to 10:45:00. AM/PM distinction: 1:22:33PM = 13:22:33 |

### 2.4.4 HARDWARE WATCHDOG TIMER

The hardware watchdog timer of the 71M6521 is disabled when the voltage at the V1 pin is at 3.3V (V3P3). On the Demo Boards, this is done by plugging in a jumper at TP10 between the V1 and V3P3 pins. Conversely, removing the jumper at TP10 will enable the hardware watchdog timer.

**Programming the flash memory or emulation using the ADM51 In-Circuit-Emulator can also be done when the ICE_E pin is pulled high.**

### 2.4.5 LCD

Various tests of the LCD interface can be performed with the Demo Board, using the serial command line interface (CLI):

The display outputs are enabled by setting the *LCD_EN* register to 1.

| Register Name | Address [bits] | R/W | Description |
|---|---|---|---|
| *LCD_EN* | 2021[5] | R/W | Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs. |

To access the *LCD_EN* register, we apply the following CLI commands:

| | |
|---|---|
| >**RI21$** | Reads the hex value of register 0x2021 |
| >**25** | Response from Demo Code indicating the bit 5 is set |
| >**RI21=5** | Writes the hex value 0x05 to register 0x2021 causing the display to be switched off |
| >**RI21=25** | Sets the *LCD_EN* register back to normal |

The *LCD_CLK* register determines the frequency at which the COM pins change states. A slower clock means lower power consumption, but if the clock is too slow, visible flicker can occur. The default clock frequency for the 71M6521 Demo Boards is 150Hz (*LCD_CLK* = 01).

| Register Name | Address [bits] | R/W | Description |
|---|---|---|---|
| *LCD_CLK[1:0]* | 2021[1:0] | R/W | Sets the LCD clock frequency, i.e. the frequency at which SEG and COM pins change states.<br>Note: $f_w$ = CKADC/128 = 38,400<br>00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$ |

To change the LCD clock frequency, we apply the following CLI commands:

| | |
|---|---|
| **>RI21$** | Reads the hex value of register 0x2021 |
| **>25** | Response from Demo Code indicating the bit 0 is set and bit 1 is cleared. |
| **>RI21=24** | Writes the hex value 0x24 to register 0x2021 clearing bit 0 – LCD flicker is visible now |
| **>RI21=25** | Writes the original value back to *LCD_CLK* |

### 2.4.6 SUPPLY CURRENT MEASUREMENTS

Some precautions have to be taken when exact supply current measurements are to be made. Supplying unnecessary pull-up resistors and/or external components with current will yield inaccurate measurement results. In brownout mode, the following precautions should be taken:

1) The Debug Board should be removed from the Demo Board.
2) The RX pin should be properly terminated, e.g. by tying it to GND. On the Demo Boards, this is accomplished with R90.
3) The jumper on JP4 should be moved to position 1-2 in order to save the current required to supply the ICE_E pin.

## 2.5 TERIDIAN APPLICATION NOTES

Below is a list of Teridian Applications Notes that are relevant to the 71M6521. They can be obtained on the Teridian web site:

- AN_651X_033 Development Tools
- AN_6521_035 RTC Compensation
- AN_652X_041 EMC Design Guidelines
- AN_6521_044 Meter Design for Power Failure
- AN_65XX_045 Power Monitoring Applications
- AN_6521_047 ESD Testing to IEC 61000-4-2
- AN_6521_049 Transition 6521-6521xE
- AN_65XX_054 The RTC of the 65XX Metering ICs
- AN_65XX_057 Programming of Teridian Metering ICs

3

# 3 HARDWARE DESCRIPTION

## 3.1 D6521T4A7 DEMO BOARD DESCRIPTION: JUMPERS, HEADERS, SWITCHES, TEST POINTS, CONNECTORS

This description covers the D6521T4A7 Demo Board. The D6521T4A8 and D6521T4A10, Demo Boards have similar jumpers, switches, test points and connectors.

The items described in the following tables refer to the flags in Figure 3-1.

| Item # (Figure 3.1) | Schematic & Silk Screen Reference | Name | Use |
|---|---|---|---|
| 1 | TP15 | GND | Test point for board ground |
| 2 | TP2 | VA, REFA | 2-pin header test point. Pin 1 is the VA line voltage input to the IC, pin 2 is REFA. |
| 3 | D5 | Wh | Wh LED (real energy) |
| 4 | D6 | VARh | VARh LED (reactive energy) |
| 5 | JP12 | BAT_MODE | This 3-pin header allows selection of the battery mode operation: A jumper across pins 1-2 indicates that **no external battery** is available. The 71M6521 will stay in brownout mode when system power is down and it will communicate at 9600bd.<br>A jumper across pins 2-3 indicates that an **external battery** is available. The 71M6521 will be able to transition from brownout mode to sleep and LCD modes when system power is down and it will communicate at 300bd. |
| 6 | J12 | V3P3, OPT_TX, V3P3, OPT_RX, GND | 5-pin header. Pins 1 and 3 carry the supply voltage to the 6521 IC. Pin 2 is the TX_OPT output of the 6521 IC. Pin 4 is the OPT_RX input to the 6521 IC. Pin 5 is ground. |
| 7 | TP21 | | Test points for pulses generated by the VARh LED. |
| 8 | SW1 | RESET | Chip reset switch: The RESET pin has an internal pull-down thatallows normal chip operation. When the switch is pressed, the RESET pin is pulled high which resets the IC into a known state.<br>**Note: The RESET button may be disabled in the Demo Board default configuration. The RESET button can be enabled by removing R91.** |
| 9 | TP22 | | Test points for pulses generated by the Wh LED. |
| 10 | JP8 | GND, VBAT | 3-pin header for connection of an external battery (+ at pin 2, - at pin 3). If no battery is connected, a jumper must be installed across pins 1-2. |
| 11 | JP4 | ICE enable | Selector for ICE/regular operation:<br>**Jumper 1-2 = regular operation (default)**<br>Jumper 2-3 = ICE operation<br>**Remove this jumper for brownout current measurements!** |

| Item # (Figure 3.1) | Schematic & Silk Screen Reference | Name | Use |
|---|---|---|---|
| 12 | U7 | | LCD |
| 13 | U5 | | 71M6521 in QFN-68 package |
| 14 | TP19 | IB, V3P3 | 2-pin test point. Pin 1 is the IB input to the IC and pin 2 is the V3P3 reference. |
| 15 | SW2 | PB | Pushbutton used to wake up the chip when in sleep or LCD mode. This button can also be used in Mission Mode to cycle the display. |
| 16 | J15 | | An emulator or flash programmer can be connected to this 5-pin header. For production units, this is a more economical alternative to J14. |
| 17 | J2 | DEBUG | Connector for plugging in the Debug Board, either directly or via a flat ribbon cable. |
| 18 | TP17 | | 2-pin header providing access to TMUXOUT and CKTEST. |
| 19 | J14 | EMULATOR I/F | 2x10 male header with 0.05" pitch. The connector of the Signum ADM51 emulator can be plugged into J14. Alternatively, J15 can be used. |
| 20 | TP10 | V1, V3P3 | 2-pin header representing the V1 comparator voltage input test point and ground. A jumper should be placed between V1 and V3P3 to disable the watchdog timer. |
| 21 | TP1 | IA, V3P3 | 2-pin header test point. Pin 1 is the IA input to the IC and pin 2 is V3P3. |
| 22 | J3 | IA_IN | 3-pin header on the bottom of the board for connection of the CT for phase A. Pin 3 may be used to ground an optional cable shield. In shunt configuration, two wires from the shunt resistor representing the voltage across the shunt are connected to pins 1 and 2. |
| 23 | J16 | IB_IN | 3-pin header on the bottom of the board for connection of the CT for phase B. Pin 3 may be used to ground an optional cable shield. |
| 24 | J1 | 5VDC | Plug for connection of the external 5 VDC power supply. |
| 25 | J9 | NEUTRAL | This is the NEUTRAL line voltage input. It is connected to the 3.3V net of the 71M6521. The neutral wire is connected to the spade terminal on the bottom of the board. |
| 26 | J4 | VA_IN   | This is the line voltage input that feeds both the resistor divider leading to the VA pin on the chip and the internal power supply. The line voltage wire is connected to the spade terminal on the bottom of the board. **Caution: High Voltage. Do not touch this pin!** |

**Table 3-1: D6521N12A7 Demo Board Description**

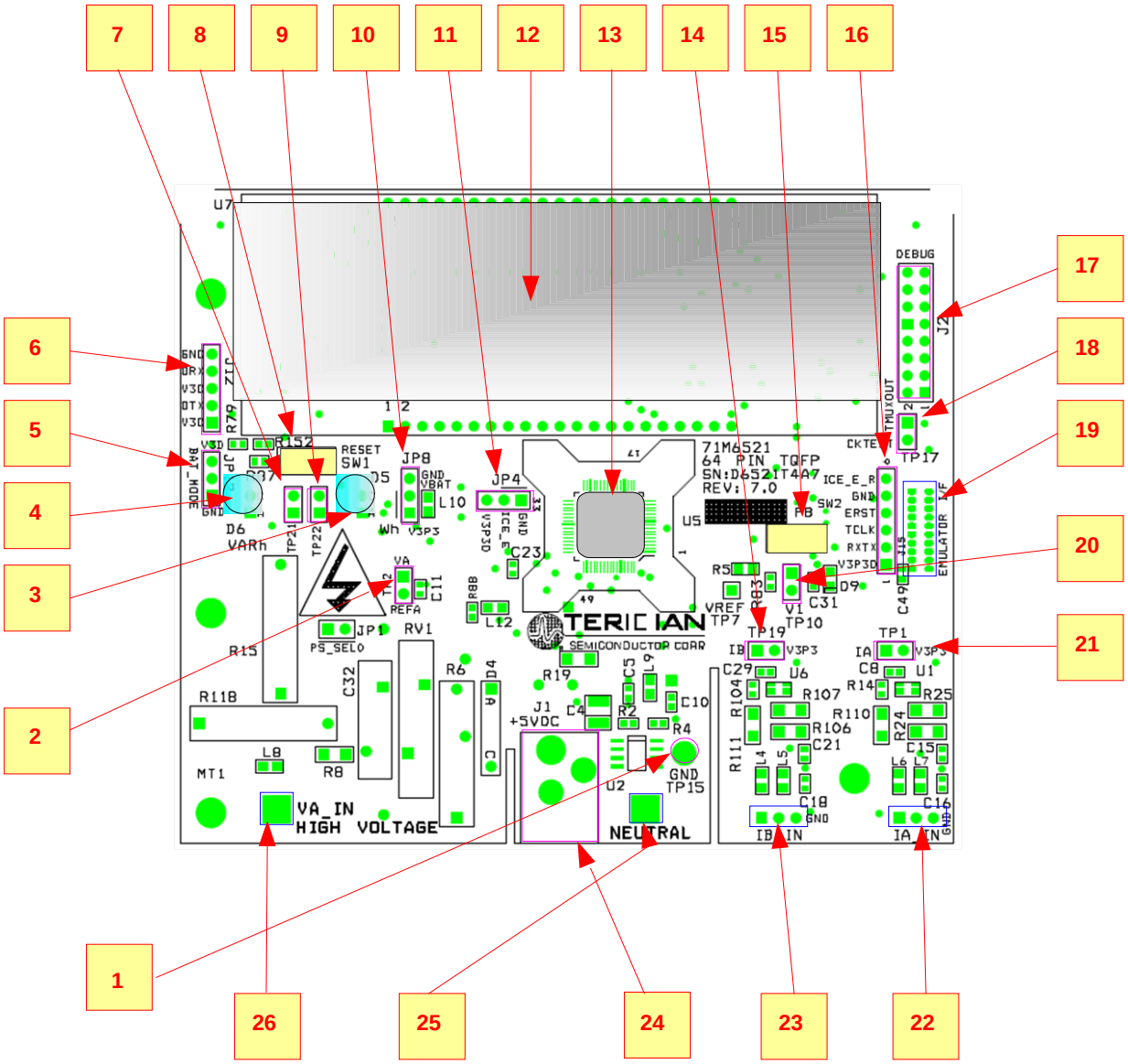



**Figure 3-1: 71M6521T4A7 Demo Board Connectors, Jumpers, Switches, and Test Points**

## 3.2 DEMO BOARD HARDWARE SPECIFICATIONS

**PCB Dimensions**

| | |
|---|---|
| ▪ Dimensions | 4.5" x 3.8" (114.3mm x 96.5mm) |
| ▪ Thickness | 0.062" (1.6mm) |
| ▪ Height w/ components | 2.0" (51mm) |

**Environmental**

| | |
|---|---|
| ▪ Operating Temperature (function of crystal oscillator affected outside –10°C to +60°C) | -40°…+85°C |
| ▪ Storage Temperature | -40°C…+100°C |

**Power Supply**

| | |
|---|---|
| ▪ Using AC Input Signal | 180V…700V rms |
| ▪ DC Input Voltage (powered from DC supply) | 5VDC ±0.5V |
| ▪ Supply Current | 25mA typical |

**Input Signal Range**

| | |
|---|---|
| ▪ AC Voltage Signal (VA) | 0…240V rms |
| ▪ AC Current Signals (IA, IB) from Transducer | 0…0.25V p/p |

**Interface Connectors**

| | |
|---|---|
| ▪ DC Supply Jack (J1) to Wall Transformer | Concentric connector, 2.5mm |
| ▪ Emulator (J14) | 10x2 Header, 0.05" pitch |
| ▪ Emulator (J15) | 5x1 Header, 0.1" pitch |
| ▪ Input Signals | Spade terminals and 0.1" headers on PCB bottom |
| ▪ Debug Board (J2) | 8x2 Header, 0.1" pitch |
| ▪ Target Chip (U5) | LQFP64/QFN68 |

**Functional Specification**

| | |
|---|---|
| ▪ Time Base Frequency | 32.768kHz, ±20PPM at 25°C |
| ▪ Time Base Temperature Coefficient | -0.04PPM/°C$^2$ (max) |

**Controls and Displays**

| | |
|---|---|
| ▪ Reset | Button (SW2) |
| ▪ Numeric Display | 8-digit LCD, 8-segments per digit, 12.7mm character height, 89.0 x 17.7mm view area |
| ▪ "Watts", "VARS" | red LEDs (D5, D6) |

**Measurement Range**

| | |
|---|---|
| ▪ Voltage | 120…700 V rms (resistor division ratio 1:3,398) |
| ▪ Current | 1.7Ω termination for 2,000:1 CT input (200A) |

**Regulatory Compliance**

| | |
|---|---|
| ▪ RoHS | For boards manufactured after 7-17-2006, the PCB, components, and processing are in compliance with the RoHS guidelines. |

## 3.3 CHANGES TO THE D6521T4A7

The Demo Board revision 7.0 (D6521T4A7) improves performance over previous revisions in the following areas:

1. Optimized schematics for increased resistance against ESD.
2. Optimized layout for improved accuracy at low currents.
3. Added ICE_E signal to headers J14 and J15.
4. Default configuration is for resistive shunt.

The changes made to the D6521T4A7 design will be described in the following four chapters.

### 3.3.1 INCREASED ESD PROTECTION

The following components were added or removed to improve the stability of the V3P3D net for increased rejection of ESD, as specified by IEC 6100-4-2 (ESD spikes applied to table-top equipment via a metallic plate mounted underneath the meter):

- C38 (1,000pF) added at J2
- C44 (1,000pF) added at J14
- C45 (1,000pF) added at J12
- C46 (1,000pF) added at JP12
- C47 (1,000pF) added at JP5
- Pull-up resistors R88, R89, R119 removed at J14
- C7, C13, C48 (22pF) added at J14

### 3.3.2 IMPROVED ACCURACY AT LOW CURRENTS

Improvement of meter accuracy at low currents was achieved by assigning both copper structures at the current inputs (top and bottom) to the V3P3 net, as shown in Figure 3-2.

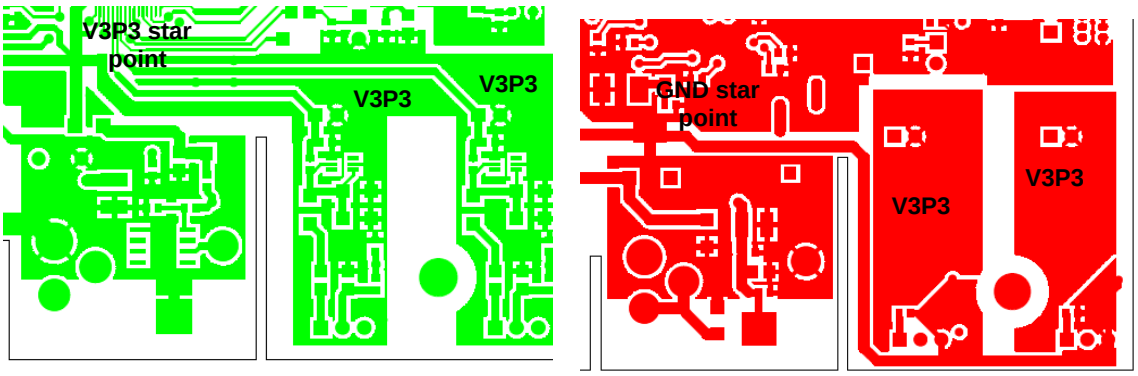



**Figure 3-2: Top (Left) and Bottom Copper (Right) Structures at Current Inputs**

### 3.3.3 ACCESS TO THE ICE_E SIGNAL

Another improvement is the added access to the ICE_E signal via the filter formed by R100 (1kΩ) and C12 (1,000pF) for the TFP-2 Flash Programming Device at the programming headers J 15 (pin #6) and J14 (pin #2). These pins allow the TFP-2 to reset the 71M6521 chip after a flash erase operation using the watchdog-timeout mechanism, allowing flash memory parts with the *SECURE* bit set (see the data sheet for more information) to be erased and reprogrammed.

### 3.3.4 DEFAULT CONFIGURATION FOR RESISTIVE CURRENT SHUNT

Due to the majority of the 71M6521 meter designs using resistive shunts, the D6521T4A7 Demo Board are shipped configured for shunts. To convert the D6521T4A7 Demo Board to CT configuration, the following changes have to be made:

1. Remove R88
2. Install L12, L9, R19, and C10
3. Remove R24 and install the proper burden resistor combination at R24 and R25.

## 3.4 D6521T4A10: FEATURES

### 3.4.1 D6521T4A10 FEATURE SUMMARY

The features added to the D6521T4A10 Demo Board are:

1) Circuitry was added that supports features required for the India market.
2) J14 was removed. The 6-pin header J15 is the only programming connector available on the board. An adapter that enables the transition from the AMP/Tyco connector used for the ADM51 ICE or for the TFP2 programmer to the 6-pin header J15 is supplied with the Demo Kit.
3) J1 was replaced by a simple two-pin header with key feature that prevents reversing the polarity.

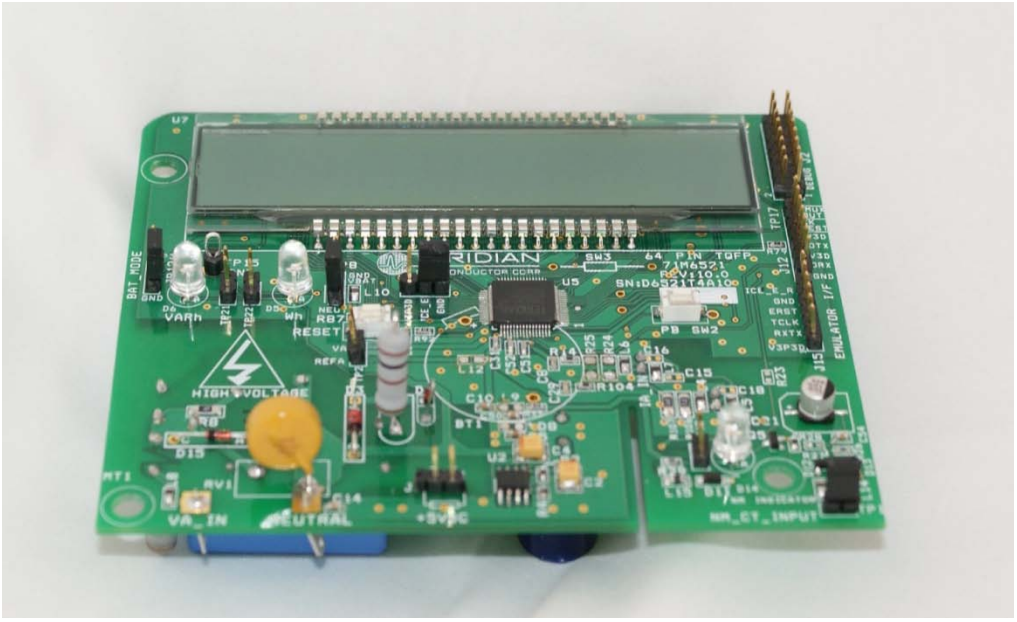



**Figure 3-3: D6521T4A10 Demo Board**

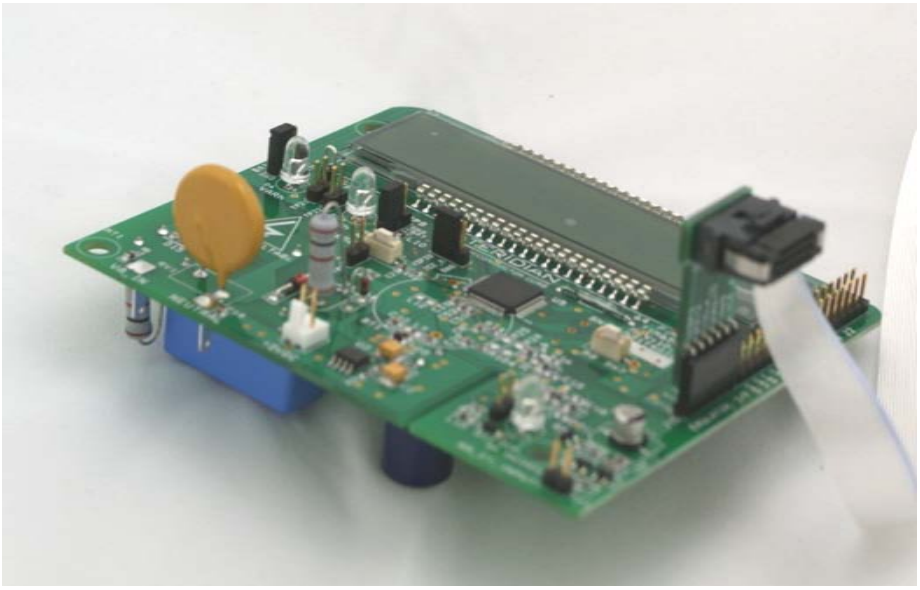


**Figure 3-4: D6521T4A10 Demo Board with ICE Adapter**

### 3.4.2 D6521T4A10 FEATURES FOR THE INDIA MARKET

Several India-specific features were added to the D6521T4A10 Demo Board to support the detection of tamper attempts. These features are:

1) A 2-pin header (TP1) is provided that allows the connection of a "neutral-missing" transformer. This transformer normally provides enough output voltage and current to supply the Demo Board in case the main AC supply is disconnected.

2) The output of the NM circuit is routed to the 6521FE and annunciated by LED D14.

3) Magnetic tamper switch (SW3).

4) The net connected to the pushbutton is separated from the 6521FE by a capacitor. This prevents drainage of the battery by constant activation of the pushbutton.

For details see the schematics in the Appendix.

The India-specific features are currently not supported by Demo Code. Demo Code will be supplied to interested customers as soon as it becomes available.

### 3.4.3 D6521T4A10 BOARD DESCRIPTION

The D6521T4A10 Demo Board is very similar to the D6521T4A8, and D6521T4A7 Demo Boards. The main functional elements and connectors are shown in Figure 3-5.

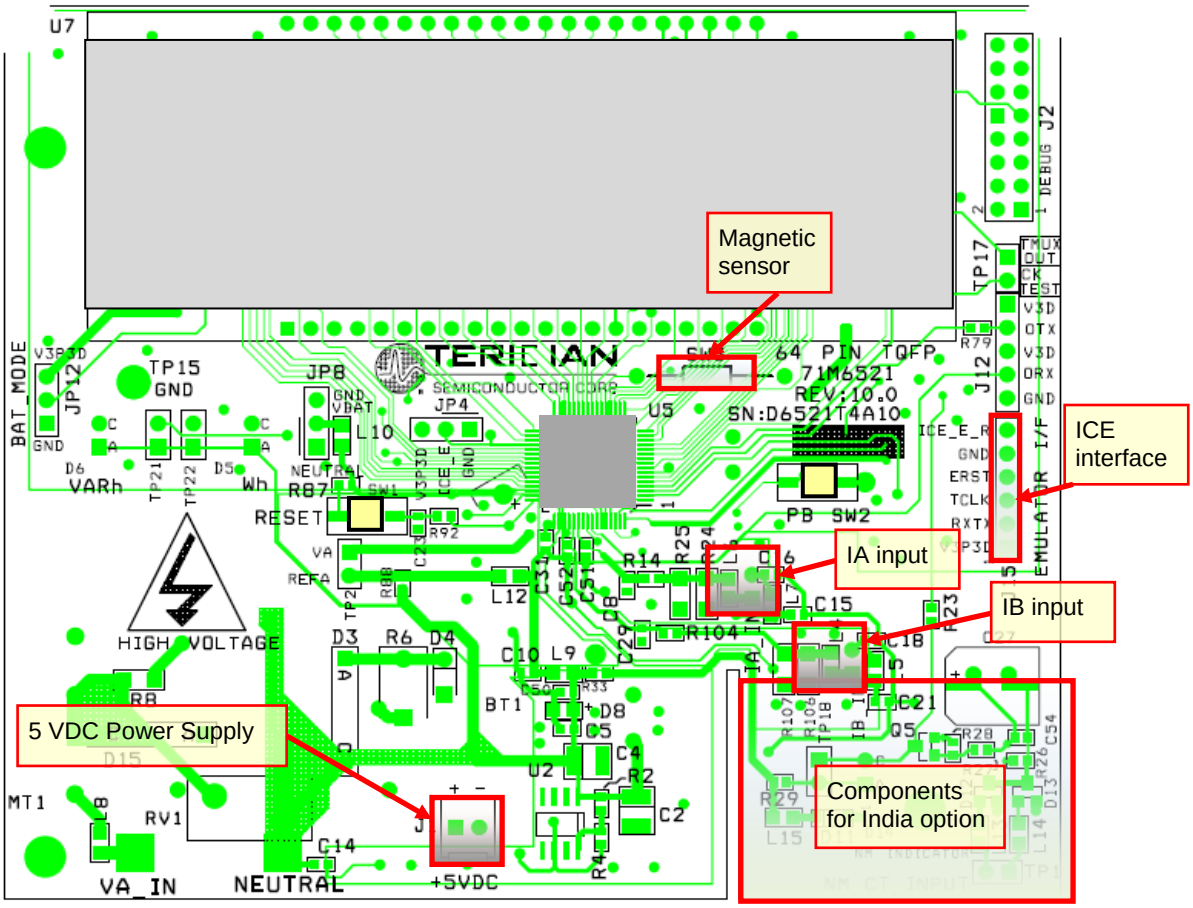



**Figure 3-5: D6521T4A10 Demo Board**

4

# 4 APPENDIX

**Demo Board Description**

This appendix includes the following documentation, tables and drawings for the, D65214A7, D65214A8, and D6521T4A10 Demo Boards:

- Schematics
- Bills of Materials (Parts Lists)
- PCB Layout Views

**Debug Board Description**

- Debug Board Electrical Schematic
- Debug Board Bill of Materials
- Debug Board PCB Silk screen layer – Top and Bottom side
- Debug Board PCB Metal Layer – Top and Bottom side signal layer
- Debug Board PCB Metal Layer – Middle 1, ground plane
- Debug Board PCB Metal Layer – Middle 2, supply plane

**71M6521 Pin-Out and Mechanical Description**

- 71M6521 Pin Description
- 71M6521 Pin-out

## 4.1 64-PIN DEMO BOARD ELECTRICAL SCHEMATIC (D6521T4A7)

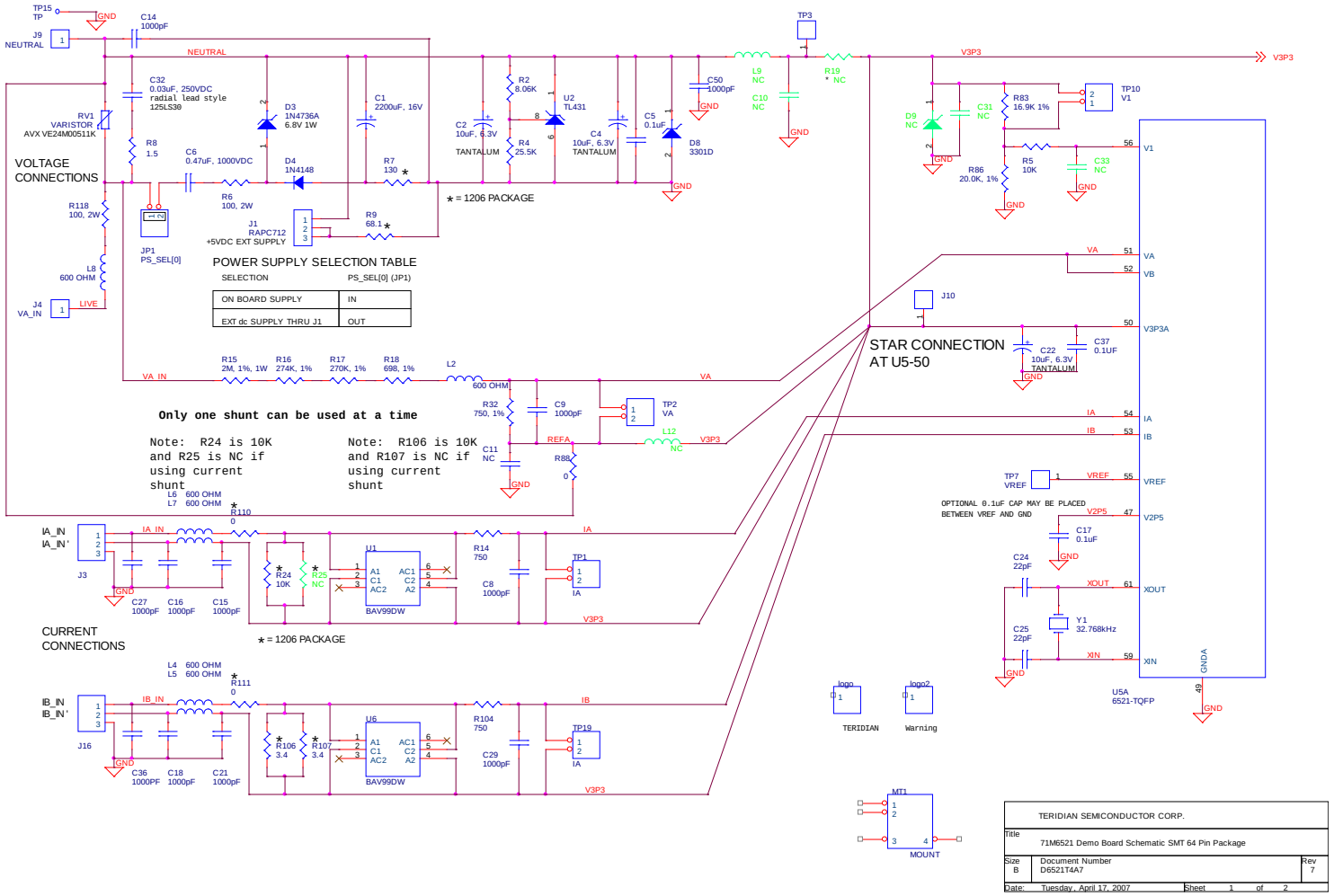



**Figure 4-1: D6521T4A7 Demo Board: Electrical Schematic 1/2**

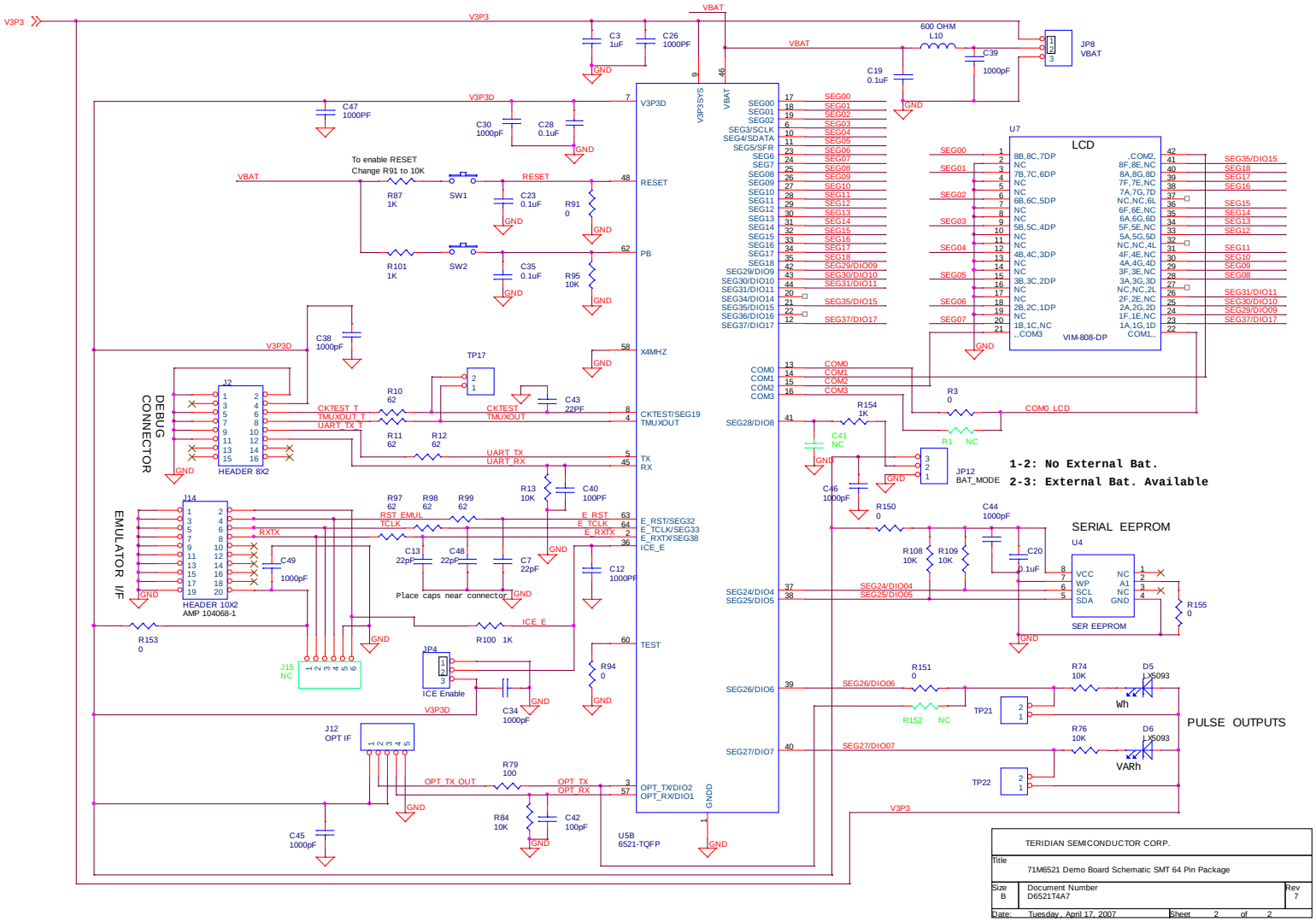



**Figure 4-2: D6521T4A7 Demo Board: Electrical Schematic 2/2**

## 4.2 64-PIN DEMO BOARD ELECTRICAL SCHEMATIC (D6521T4A8)

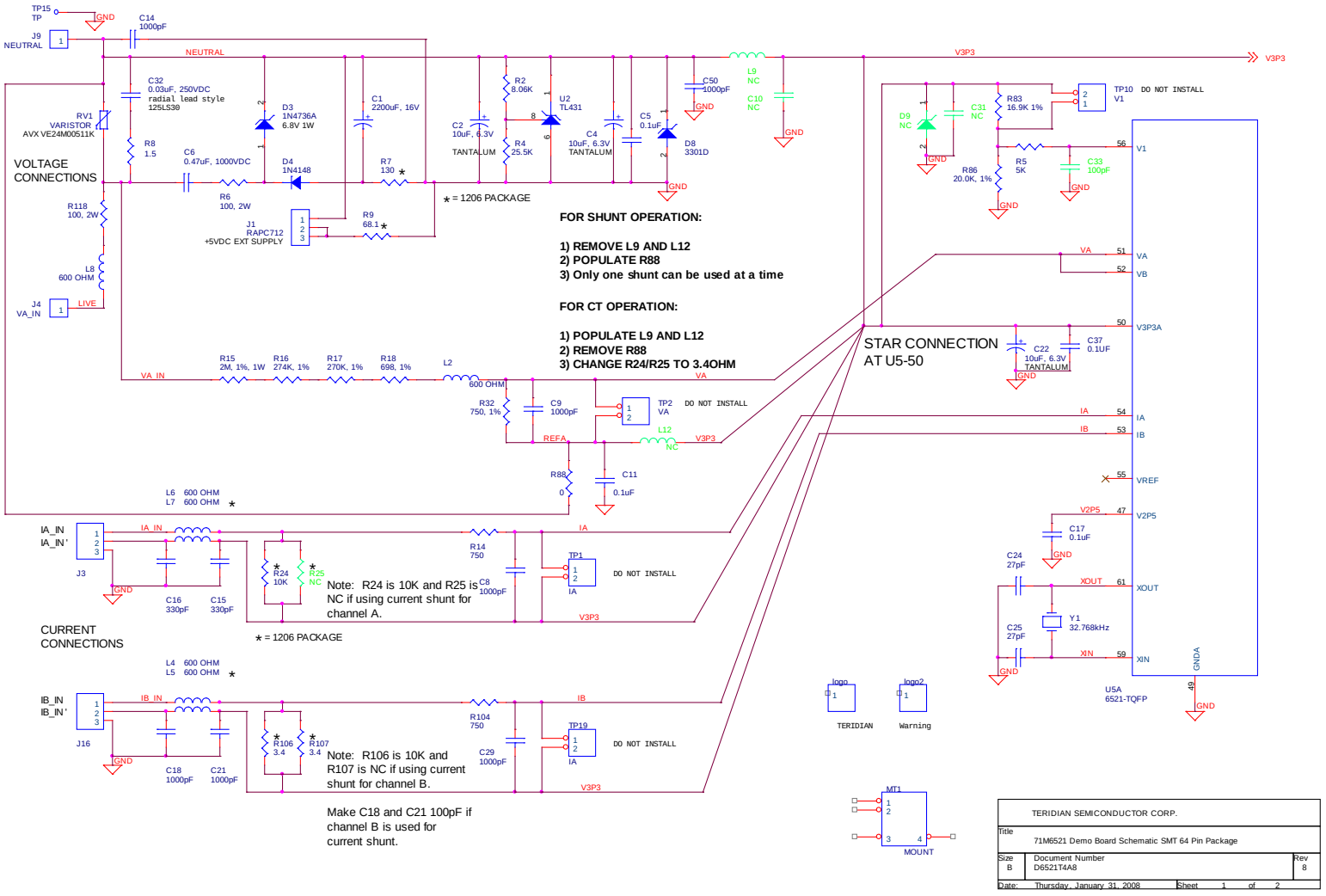



**Figure 4-3: D6521T4A8 Demo Board: Electrical Schematic 1/2**

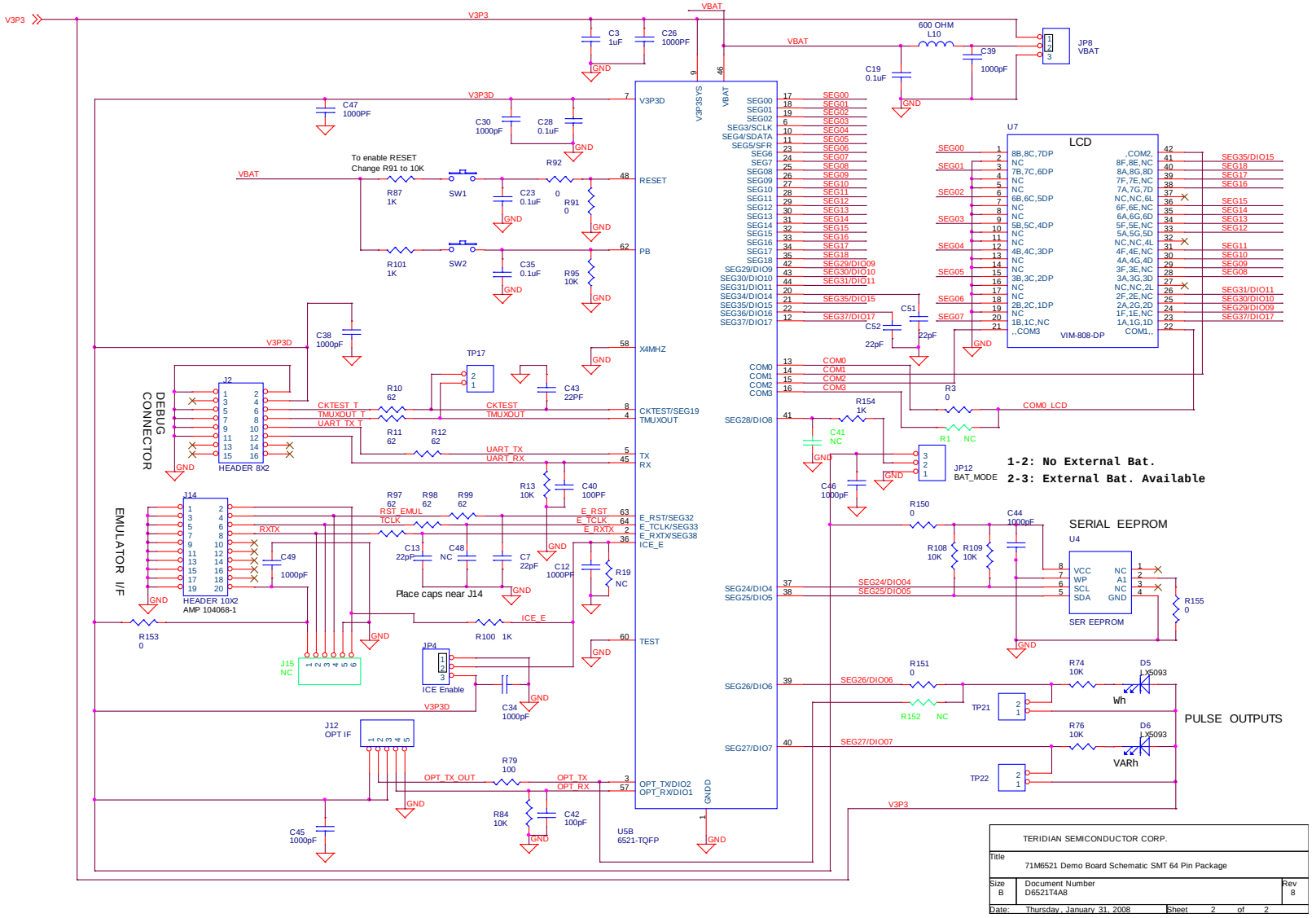



**Figure 4-4: D6521T4A8 Demo Board: Electrical Schematic 2/2**

## 4.3 64-PIN DEMO BOARD ELECTRICAL SCHEMATIC (D6521T4A10)

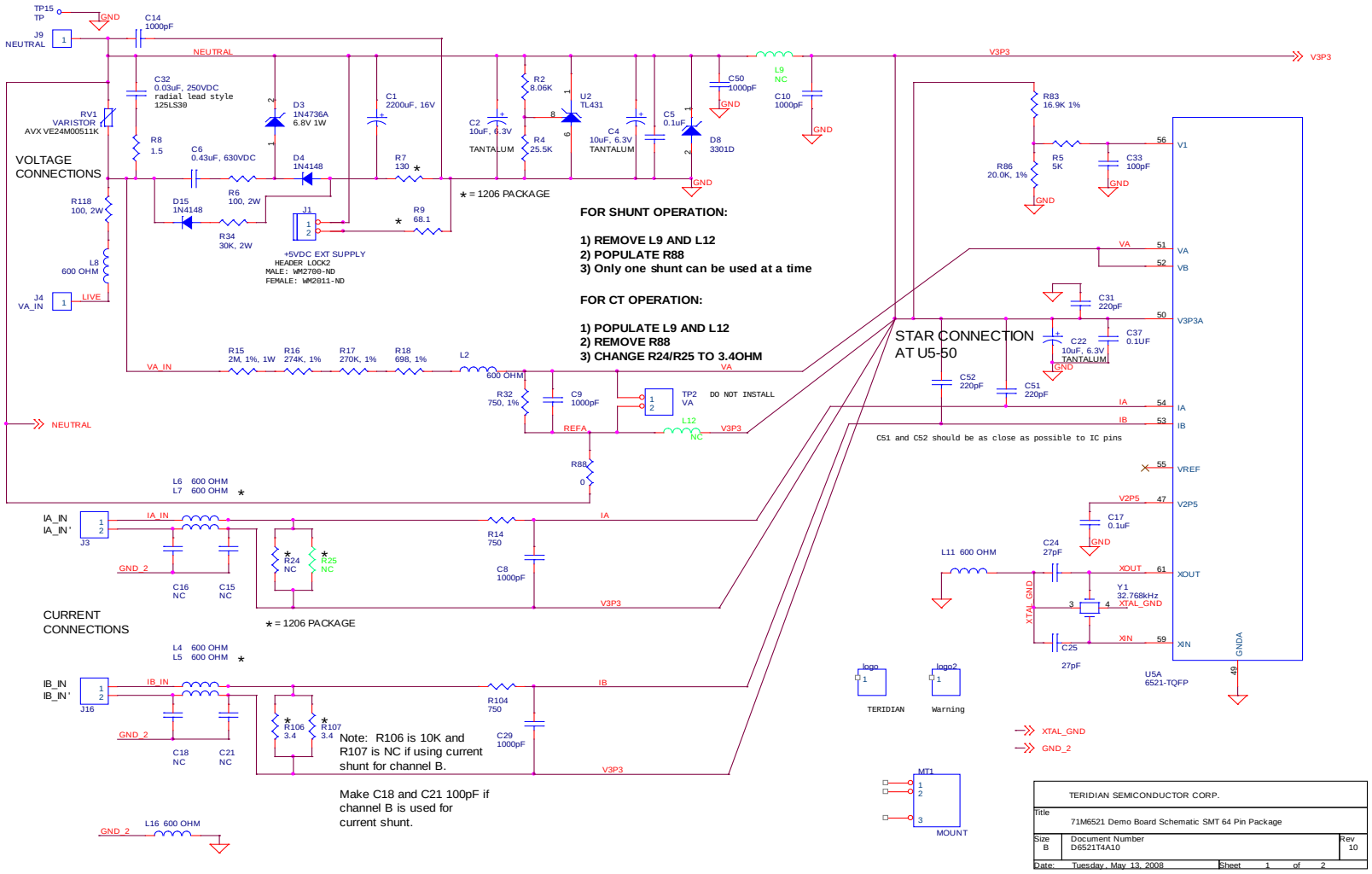



**Figure 4-5: D6521T4A10 Demo Board: Electrical Schematic 1/3**

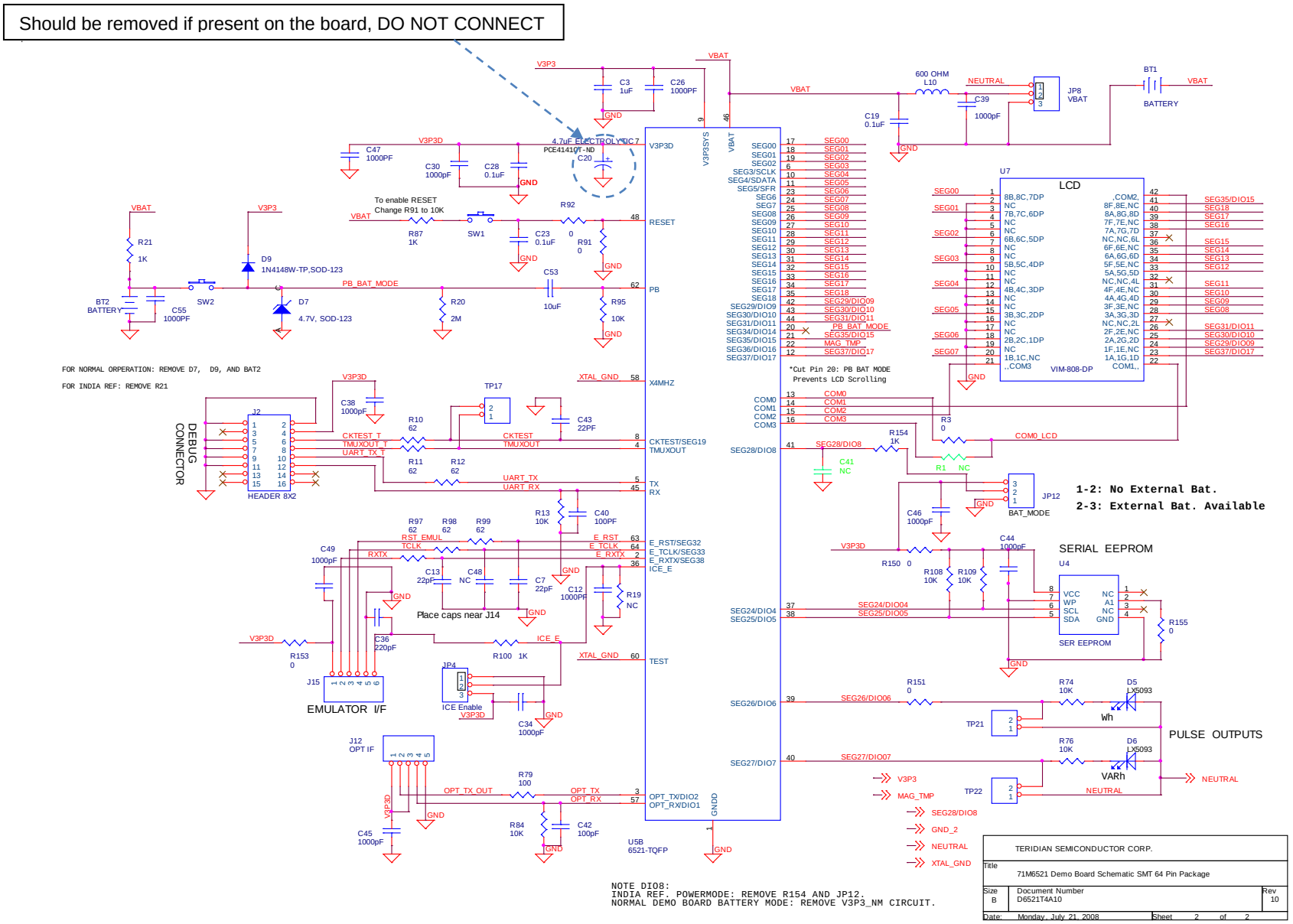



**Figure 4-6: D6521T4A10 Demo Board: Electrical Schematic 2/3**

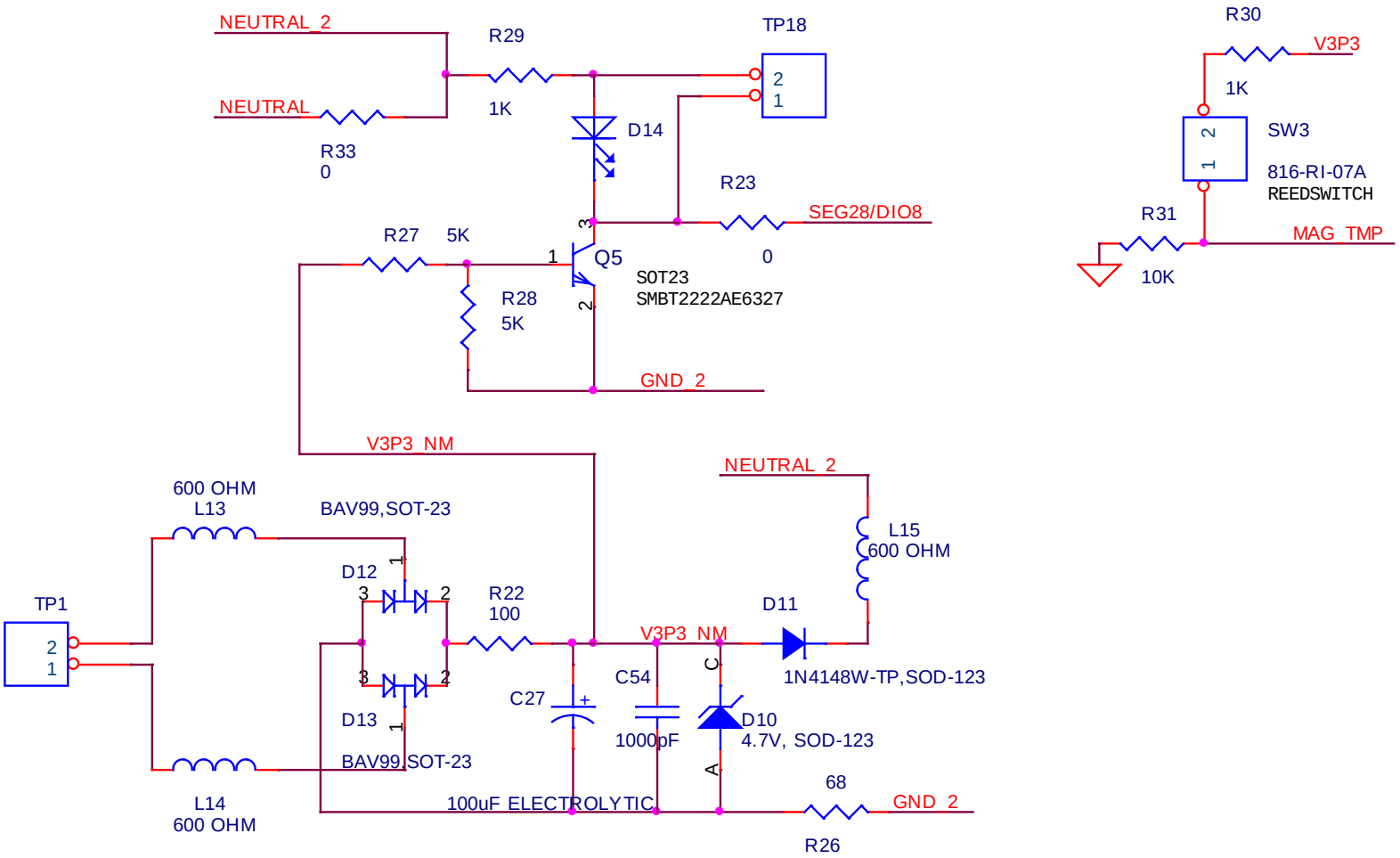



**Figure 4-7: D6521T4A10 Demo Board: Electrical Schematic 3/3**

## 4.4 D6521T4A7 DEMO BOARD BILL OF MATERIAL

| Item | Q | Reference | Part | PCB Footprint | Digi-Key/Mouser Part Number | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 2200uF | radial | P5143-ND | ECA-1CM222 | Panasonic |
| 2 | 3 | C2,C4,C22 | 10uF | RC1812 | 478-1672-1-ND | TAJB106K010R | AVX |
| 3 | 1 | C3 | 1uF | RC0603 | PCC2224CT-ND | ECJ-1VB1C105K | Panasonic |
| 4 | 8 | C5,C17,C19,C20,C23,C28, | 0.1uF | RC0603 | 445-1314-1-ND | C1608X7R1H104K | TDK |
| | | C35,C37 | | | | | |
| 5 | 1 | C6 | 0.47uF | | BC1918-ND | 2222 383 30474 | BC Components |
| 6 | 6 | C7,C13,C24,C25,C43,C48 | 22pF | RC0603 | 445-1273-1-ND | C1608C0G1H220J | TDK |
| 7 | 22 | C8,C9,C12,C14-C16,C18,C21, | 1000pF | RC0603 | 445-1298-1-ND | C1608X7R2A102K | TDK |
| | | C26,C27,C29,C30,C34,C36,C38, | | | | | |
| | | C39,C44,C45,C46,C47,C49,C50 | | | | | |
| 8 | | C10,C11,C31,C33,C41 | NC | RC0603 | | | |
| 9 | 1 | C32 | 0.03uF | axial | 75-125LS30-R | 125LS30-R | Vishay |
| 10 | 2 | C40,C42 | 100pF | RC0603 | 445-1281-1-ND | C1608C0G1H101J | TDK |
| 11 | 1 | D3 | 6.8V ZENER | D041 | 1N4736ADICT-ND | 1N4736A-T | DIODES |
| 12 | 1 | D4 | Switching Diode | D035 | 1N4148DICT-ND | 1N4148-T | DIODES |
| 13 | 2 | D5,D6 | LED | radial | 404-1104-ND | H-3000L | Stanley |
| 14 | 1 | D8 | UCLAMP3301D | SOD-323 | -- | UCLAMP3301D.TCT | SEMTECH |
| 15 | | D9 | NC | SOD-323 | | | |
| 16 | 1 | J1 | DC CONNECTOR | | SC237-ND | RAPC712X | Switchcraft |
| 17 | 1 | J2 | HEADER 8X2 | 8X2PIN | S2011E-36-ND | PZC36DAAN | Sullins |
| 18 | 2 | J3,J16 | HEADER 3 | 3X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 19 | 2 | J4,J9 | Spade Terminal | | A24747CT-ND | 62395-1 | AMP |
| 20 | 1 | J10 | HEADER 1 | 1X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 21 | 1 | J12 | HEADER 5 | 5X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 22 | 1 | J14 | 10X2 CONNECTOR, 0.05" | | 571-5-104068-1 | 5-104068-1 | AMP |
| 23 | | J15 | NC | 6X1PIN | | | |
| 24 | 1 | JP1 | HEADER 2 | 2X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 25 | 3 | JP4,JP8,JP12 | HEADER 3 | 3X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 26 | 8 | L2,L4-L8, L10, L12* | Ferrite bead, 600 Ohm | RC0805 | 445-1556-1-ND | MMZ2012S601A | TDK |
| 27 | | L9 | NC | RC0805 | | | |
| 28 | 1 | RV1 | VARISTOR | radial | 581-VZD510XX | VE24M00511K | AVX |
| 29 | | R1,R152 | NC | RC0603 | | | |
| 30 | 1 | R2 | 8.06K, 1% | RC0603 | P8.06KHCT-ND | ERJ-3EKF8061V | Panasonic |
| 31 | 8 | R3,R88,R91,R94,R150,R151, | 0 | RC0603 | P0.0GCT-ND | ERJ-3GEY0R00V | Panasonic |
| | | R153,R155 | | | | | |
| 32 | 1 | R4 | 25.5K, 1% | RC0603 | P25.5KHCT-ND | ERJ-3EKF2552V | Panasonic |
| 33 | | R5 | 10K | RC0805 | P10KACT-ND | ERJ-6GEYJ103V | Panasonic |
| 34 | 2 | R6,R118 | 100, 2W | axial | 100W-2-ND | RSF200JB-100R | Yageo |
| 35 | 1 | R7 | 130, 1% | RC1206 | P130FCT-ND | ERJ-8ENF1300V | Panasonic |
| 36 | 1 | R8 | 1.5 | RC1206 | P1.5ECT-ND | ERJ-8GEYJ1R5V | Panasonic |
| 37 | 1 | R9 | 68.1 | | P68.1FCT-ND | ERJ-8ENF68R1V | Panasonic |
| 38 | 6 | R10,R11,R12,R97,R98,R99 | 62 | RC0603 | P62GCT-ND | ERJ-3GEYJ620V | Panasonic |
| 39 | 7 | R13,R74,R76,R84,R95, | 10K | RC0603 | P10KGCT-ND | ERJ-3GEYJ103V | Panasonic |
| | | R108,R109 | | | | | |
| 40 | 3 | R14,R32,R104 | 750, 1% | RC0603 | P750HCT-ND | ERJ-3EKF7500V | Panasonic |
| 41 | 1 | R15 | 2M, 1% | axial | 71-RN65DF-2.0M | RN65D2004FB14 | Dale |
| 42 | 1 | R16 | 274K, 1% | RC0805 | P274KCCT-ND | ERJ-6ENF2743V | Panasonic |
| 43 | 1 | R17 | 270K, 1% | RC0805 | RHM270KCCT-ND | MCR10EZHF2703 | Rohm |
| 44 | 1 | R18 | 698, 1% | RC0805 | P698CCT-ND | ERJ-6ENF6980V | Panasonic |
| 45 | 2 | R19,R25 | NC | RC1206 | | | |
| 46 | 1 | R24 | 10K | RC1206 | P10.0KFCT-ND | ERJ-8ENF1002V | Panasonic |
| 47 | 1 | R79 | 100 | RC0603 | P100GCT-ND | ERJ-3GEYJ101V | Panasonic |
| 48 | 1 | R83 | 16.9K, 1% | RC0603 | P16.9KHCT-ND | ERJ-3EKF1692V | Panasonic |
| 49 | 1 | R86 | 20K, 1% | RC0603 | P20.0KHCT-ND | ERJ-3EKF2002V | Panasonic |
| 50 | 4 | R87, R100,R101,R154 | 1K | RC0603 | P1.0KGCT-ND | ERJ-3GEYJ102V | Panasonic |
| 51 | 2 | R106,R107 | 3.4, 1% | RC1206 | 311-3.40FRCT-ND | RC1206FR-073R40L | Yageo |
| 52 | 2 | R110,R111 | 0 | RC1206 | P0.0ECT-ND | ERJ-8GEY0R00V | Panasonic |
| 53 | 2 | SW1,SW2 | | | P8051SCT-ND | EVQ-PJX05M | Panasonic |
| 54 | 7 | TP1,TP2,TP10,TP17,TP19, | TP | 2X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| | | TP21,TP22 | | | | | |
| 55 | 2 | TP3,TP7 | TP | 1X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 56 | 1 | TP15 | Test Point | | 5011K-ND | 5011 | Keystone 1) |
| 57 | 2 | U1,U6 | BAV99DW | SOT363 | BAV99DW-FDICT-ND | BAV99DW-7-F | DIODES |
| 58 | 1 | U2 | REGULATOR, 1% | SO8 | 296-1288-1-ND | TL431AIDR | Texas Instruments |
| 59 | 1 | U4 | SER EEPROM | | AT24C1024W10SU2.7-ND | AT24C1024W-10SU-2.7 | ATMEL |
| 60 | 1 | U5 | 71M6521 | 64TQFP | -- | 71M6521F-IGT | TERIDIAN |
| 61 | 1 | U7 | | | 153-1056-ND | VIM-808-DP-RC-S-HV | VARITRONIX 2) |
| 62 | 1 | Y1 | 32.768kHz | | XC1195CT-ND | ECS-.327-12.5-17X-TR | ECS |

**Table 4-1: D652T4A7 Demo Board: Bill of Material**

## 4.5 D6521T4A8 DEMO BOARD BILL OF MATERIAL

| Item | Q | Reference | Part | PCB Footprint | Digi-Key/Mouser Part Number | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 2200uF | radial | P5143-ND | ECA-1CM222 | Panasonic |
| 2 | 3 | C2,C4,C22 | 10uF | RC1812 | 478-1672-1-ND | TAJB106K010R | AVX |
| 3 | 1 | C3 | 1uF | RC0603 | PCC2224CT-ND | ECJ-1VB1C105K | Panasonic |
| 4 | 8 | C5,C11,C17,C19,C23,C28 | 0.1uF | RC0603 | 445-1314-1-ND | C1608X7R1H104K | TDK |
| | | C35,C37 | | | | | |
| 5 | 1 | C6 | 0.47uF | | BC1918-ND | 2222 383 30474 | BC Components |
| 6 | 6 | C7,C13,C43,C51,C52 | 22pF | RC0603 | 445-1273-1-ND | C1608C0G1H220J | TDK |
| 7 | 2 | C24,C25 | 27pF | RC0603 | 445-1274-1-ND | C1608C0G1H270J | TDK |
| 8 | 18 | C8,C9,C12,C14,C18,C21 | 1000pF | RC0603 | 445-1298-1-ND | C1608X7R2A102K | TDK |
| | | C26,C29,C30,C34,C38,C39 | | | | | |
| | | C44-C47,C49,C50 | | | | | |
| 9 | 0 | C10,C31,C41,C48 | NC | RC0603 | -- | -- | -- |
| 10 | 1 | C32 | 0.03uF | axial | 75-125LS30-R | 125LS30-R | Vishay |
| 11 | 3 | C33,C40,C42 | 100pF | RC0603 | 445-1281-1-ND | C1608C0G1H101J | TDK |
| 12 | 2 | C15,C15 | 330pF | RC0603 | 445-1287-1-ND | C1608COG1H331J | TDK |
| 13 | 1 | D3 | 6.8V ZENER | D041 | 1N4736ADICT-ND | 1N4736A-T | DIODES |
| 14 | 1 | D4 | Switching Diode | D035 | 1N4148DICT-ND | 1N4148-T | DIODES |
| 15 | 2 | D5,D6 | LED | radial | 404-1104-ND | H-3000L | Stanley |
| 16 | 1 | D8 | UCLAMP3301D | SOD-323 | -- | UCLAMP3301D.TCT | SEMTECH |
| 17 | 1 | J1 | DC CONNECTOR | | SC237-ND | RAPC712X | Switchcraft |
| 18 | 1 | J2 | HEADER 8X2 | 8X2PIN | S2011E-36-ND | PZC36DAAN | Sullins |
| 19 | 2 | J3,J16 | HEADER 3 | 3X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 20 | 2 | J4,J9 | Spade Terminal | | A24747CT-ND | 62395-1 | AMP |
| 21 | 1 | J12 | HEADER 5 | 5X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 22 | 1 | J14 | 10X2 CONNECTOR, 0.05" | | 571-5-104068-1 | 5-104068-1 | AMP |
| 23 | | J15 | NC | 6X1PIN | | | |
| 24 | 3 | JP4,JP8,JP12 | HEADER 3 | 3X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 25 | 7 | L2,L4,L5,L6,L7,L8,L10 | Ferrite bead, 600 Ohm | RC0805 | 445-1556-1-ND | MMZ2012S601A | TDK |
| 26 | 0 | L9,D9,L12 | N/C | RC0805 | | | |
| 27 | 1 | RV1 | VARISTOR | radial | 581-VZD510XX | VE24M00511K | AVX |
| 28 | 1 | R2 | 8.06K, 1% | RC0603 | P8.06KHCT-ND | ERJ-3EKF8061V | Panasonic |
| 29 | | R1.R19,R52 | N/C | RC0603 | | | |
| 30 | 8 | R3,R88,R91,R92,R150,R151 | 0 | RC0603 | P0.0GCT-ND | ERJ-3GEY0R00V | Panasonic |
| | | R153,R155 | | | | | |
| 31 | 1 | R4 | 25.5K, 1% | RC0603 | P25.5KHCT-ND | ERJ-3EKF2552V | Panasonic |
| 32 | 1 | R5 | 4.99K | RC0805 | | | Panasonic |
| 33 | 2 | R6,R118 | 100, 2W | axial | 100W-2-ND | RSF200JB-100R | Yageo |
| 34 | 1 | R7 | 130, 1% | RC1206 | P130FCT-ND | ERJ-8ENF1300V | Panasonic |
| 35 | 1 | R8 | 1.5 | RC1206 | P1.5ECT-ND | ERJ-8GEYJ1R5V | Panasonic |
| 36 | 1 | R9 | 68.1 | | P68.1FCT-ND | ERJ-8ENF68R1V | Panasonic |
| 37 | 6 | R10,R11,R12,R97,R98,R99 | 62 | RC0603 | P62GCT-ND | ERJ-3GEYJ620V | Panasonic |
| 38 | 7 | R13,R74,R76,R84,R95 | 10K | RC0603 | P10KGCT-ND | ERJ-3GEYJ103V | Panasonic |
| | | R108,R109 | | | | | |
| 39 | 3 | R14,R32,R104 | 750, 1% | RC0603 | P750HCT-ND | ERJ-3EKF7500V | Panasonic |
| 40 | 1 | R15 | 2M, 1% | axial | 71-RN65DF-2.0M | RN65D2004FB14 | Dale |
| 41 | 1 | R16 | 274K, 1% | RC0805 | P274KCCT-ND | ERJ-6ENF2743V | Panasonic |
| 42 | 1 | R17 | 270K, 1% | RC0805 | RHM270KCCT-ND | MCR10EZHF2703 | Rohm |
| 43 | 1 | R18 | 698, 1% | RC0805 | P698CCT-ND | ERJ-6ENF6980V | Panasonic |
| 44 | | R25 | NC | RC1206 | | | |
| 45 | 1 | R24 | 10K | RC1206 | P10.0KFCT-ND | ERJ-8ENF1002V | Panasonic |
| 46 | 1 | R79 | 100 | RC0603 | P100GCT-ND | ERJ-3GEYJ101V | Panasonic |
| 47 | 1 | R83 | 16.9K, 1% | RC0603 | P16.9KHCT-ND | ERJ-3EKF1692V | Panasonic |
| 49 | 1 | R86 | 20K, 1% | RC0603 | P20.0KHCT-ND | ERJ-3EKF2002V | Panasonic |
| 50 | 4 | R87, R100,R101,R154 | 1K | RC0603 | P1.0KGCT-ND | ERJ-3GEYJ102V | Panasonic |
| 51 | 2 | R106,R107 | 3.4, 1% | RC1206 | 311-3.40FRCT-ND | RC1206FR-073R40L | Yageo |
| 52 | 2 | SW1,SW2 | push button switch | | P8051SCT-ND | EVQ-PJX05M | Panasonic |
| 53 | 6 | TP1,TP2,TP17,TP19, | TP | 2X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| | | TP21,TP22 | | | | | |
| 54 | 1 | TP15 | Test Point | | 5011K-ND | 5011 | Keystone |
| 55 | 1 | U2 | REGULATOR, 1% | SO8 | 296-1288-1-ND | TL431AIDR | Texas Instruments |
| 56 | 1 | U4 | serial EEPROM | | AT24C1024W10SU2.7-ND | AT24C1024W-10SU-2.7 | ATMEL |
| 57 | 1 | U5 | 71M6521 | 64TQFP | -- | 71M6521F-IGT | TERIDIAN |
| 58 | 1 | U7 | LCD | | 153-1056-ND | VIM-808-DP-RC-S-HV | VARITRONIX |
| 59 | 1 | Y1 | 32.768kHz | | XC1195CT-ND | ECS-.327-12.5-17X-TR | ECS |

**Table 4-2: D652T4A8 Demo Board: Bill of Material**

# 4.6 D6521T4A10 DEMO BOARD BILL OF MATERIAL

| Item | Q | Reference | Part | PCB Footprint | Digi-Key/Mouser Part Number | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 1 | 2 | BT1,BT2 | Battery | | | | |
| 2 | 1 | C1 | 2200uF | radial | P5143-ND | ECA-1CM222 | Panasonic |
| 3 | 3 | C2,C4,C22 | 10uF | RC1812 | 478-1672-1-ND | TAJB106K010R | AVX |
| 4 | 1 | C3 | 1uF | RC0603 | PCC2224CT-ND | ECJ-1VB1C105K | Panasonic |
| 5 | 6 | C5,C17,C19,C23,C28,C37 | 0.1uF | RC0603 | 445-1314-1-ND | C1608X7R1H104K | TDK |
| 6 | 1 | C6 | 0.43uF, 630VDC | Radial | BC1870-ND | 2222 383 20434 | BC Components |
| 7 | 3 | C7,C13,C43 | 22pF | RC0603 | 445-1273-1-ND | C1608C0G1H220J | TDK |
| 8 | 19 | C8,C9,C10,C12,C14,C26,C29 | 1000pF | RC0603 | 445-1298-1-ND | C1608X7R2A102K | TDK |
| | | C30,C34,C38,C39,C44,C45 | | | | | |
| | | C46,C47,C49,C50,C54,C55 | | | | | |
| 9 | 13 | R1,L9,L12,J15,C15,C16 | NC | RC0603 | | | |
| | | C18,R19,C21,R24,R25,C41,C48 | | | | | |
| 10 | 1 | C20 | 4.7uF ELECTROLYTIC | 0.169" L x 0.169" W x 0.228" H | PCE4141CT-ND | EEE-HB1E4R7R | Panasonic |
| 11 | 2 | C24,C25 | 27pF | RC0603 | 445-1274-1-ND | C1608C0G1H270J | TDK |
| 12 | 1 | C27 | 100uF ELECTROLYTIC | | PCE3867CT-ND | EEE-1AA101WR | Panasonic |
| 13 | 4 | C31,C36,C51,C52 | 220pF | RC0603 | 445-1285-1-ND | C1608C0G1H221J | TDK |
| 14 | 1 | C32 | 0.03uF, 250VDC | axial | 75-125LS30-R | 125LS30-R | Vishay |
| 15 | 3 | C33,C40,C42 | 100pF | RC0603 | 445-1281-1-ND | C1608C0G1H101J | TDK |
| 16 | 1 | C53 | 10uF | RC0805 | 445-1371-1-ND | C2012Y5V1A106Z | TDK |
| 17 | 1 | D3 | 6.8V ZENER | D041 | 1N4736ADICT-ND | 1N4736A-T | DIODES |
| 18 | 2 | D4,D15 | Switching Diode | D035 | 1N4148DICT-ND | 1N4148-T | DIODES |
| 19 | 3 | D5,D6,D14 | LED | radial | 404-1104-ND | H-3000L | Stanley |
| 20 | 2 | D7,D10 | 4.7V ZENER | SOD-123 | BZT52C4V7-FDICT-ND | BZT52C4V7-7-F | DIODES |
| 21 | 1 | D8 | UCLAMP3301D | SOD-323 | UCLAMP3301DCT-ND | UCLAMP3301D.TCT | SEMTECH |
| 22 | 2 | D9,D11 | Diode Switch | SOD-123 | 1N4148WTPMSCT-ND | 1N4148W-TP | Micro Commercial |
| 23 | 2 | D12,D13 | ---- | SOT-23 | MMBD7000FSCT-ND | MMBD7000 | Fairchild |
| 24 | 3 | JP4,JP8,JP12 | HEADER 3 | 3X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 25 | 1 | J1 | DC CONNECTOR | 2X1PIN | WM2700-ND | 22-11-2022 | Molex |
| 26 | 1 | J2 | HEADER 8X2 | 8X2PIN | S2011E-36-ND | PZC36DAAN | Sullins |
| 27 | 5 | J3,J16,TP1,TP17,TP18 | HEADER 3 | 2X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 28 | 2 | J4,J9 | Spade Terminal | | A24747CT-ND | 62395-1 | AMP |
| 29 | 1 | J12 | HEADER 5 | 5X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 30 | 12 | L2,L4,L5,L6,L7,L8,L10,L11,L13,L14,L15,L16 | Ferrite bead, 600 Ohm | RC0805 | 445-1556-1-ND | MMZ2012S601A | TDK |
| 31 | 1 | Q5 | NPN Transistor | SOT-23 | SMBT2222AINCT-ND | SMBT2222AE6327 | Infineon |
| 32 | 1 | RV1 | VARISTOR | radial | 581-VZD510XX | VE24M00511K | AVX |
| 33 | 1 | R2 | 8.06K, 1% | RC0603 | P8.06KHCT-ND | ERJ-3EKF8061V | Panasonic |
| 34 | 10 | R3,R23,R33,R88,R91,R92 | 0 | RC0603 | P0.0GCT-ND | ERJ-3GEY0R00V | Panasonic |
| | | R150,R151,R153,R155 | | | | | |
| 35 | 1 | R4 | 25.5K, 1% | RC0603 | P25.5KHCT-ND | ERJ-3EKF2552V | Panasonic |
| 36 | 1 | R5,R27,R28 | 4.99K 1% | RC0603 | P4.99KHCT-ND | ERJ-3EKF4991V | Panasonic |
| 37 | 2 | R6,R118 | 100, 2W | axial | 100W-2-ND | RSF200JB-100R | Yageo |
| 38 | 1 | R7 | 130, 1% | RC1206 | P130FCT-ND | ERJ-8ENF1300V | Panasonic |
| 39 | 1 | R8 | 1.5 | RC1206 | P1.5ECT-ND | ERJ-8GEYJ1R5V | Panasonic |
| 40 | 2 | R9,R26 | 68.1 | RC1206 | P68.1FCT-ND | ERJ-8ENF68R1V | Panasonic |
| 41 | 6 | R10,R11,R12,R97,R98,R99 | 62 | RC0603 | P62GCT-ND | ERJ-3GEYJ620V | Panasonic |
| 42 | 8 | R13,R31,R74,R76,R84,R95,R108,R109 | 10K | RC0603 | P10KGCT-ND | ERJ-3GEYJ103V | Panasonic |
| 43 | 3 | R14,R32,R104 | 750, 1% | RC0603 | P750HCT-ND | ERJ-3EKF7500V | Panasonic |
| 44 | 1 | R15 | 2M, 1% | axial | 71-RN65DF-2.0M | RN65D2004FB14 | Dale |
| 45 | 1 | R16 | 274K, 1% | RC0805 | P274KCCT-ND | ERJ-6ENF2743V | Panasonic |
| 46 | 1 | R17 | 270K, 1% | RC0805 | RHM270KCCT-ND | MCR10EZHF2703 | Rohm |
| 47 | 1 | R18 | 698, 1% | RC0805 | P698CCT-ND | ERJ-6ENF6980V | Panasonic |
| 48 | 1 | R20 | 2M | RC0603 | P2.0MGCT-ND | ERJ-3GEYJ205V | Panasonic |
| 49 | 6 | R21,R29,R30,R87,R100,R154 | 1K | RC0603 | P1.0KGCT-ND | ERJ-3GEYJ102V | Panasonic |
| 50 | 1 | R22,R79 | 100 | RC0603 | P100GCT-ND | ERJ-3GEYJ101V | Panasonic |
| 51 | 1 | R34 | 30K, 2W | axial | P30KW-2BK-ND | ERG-2SJ303 | Panasonic |
| 52 | 1 | R83 | 16.9K, 1% | RC0603 | P16.9KHCT-ND | ERJ-3EKF1692V | Panasonic |
| 53 | 1 | R86 | 20K, 1% | RC0603 | P20.0KHCT-ND | ERJ-3EKF2002V | Panasonic |
| 54 | 2 | R106,R107 | 3.4, 1% | RC1206 | 311-3.40FRCT-ND | RC1206FR-073R40L | Yageo |
| 55 | 2 | SW1,SW2 | push button switch | | P8051SCT-ND | EVQ-PJX05M | Panasonic |
| 56 | 1 | SW3 | Dry Reed Switch | axial | 816-RI-07A | RI-07A | Coto Technology |
| 57 | 3 | TP2,TP21,TP22 | TP | 2X1PIN | S1011E-36-ND | PZC36SAAN | Sullins |
| 58 | 1 | TP15 | Test Point | | 5011K-ND | 5011 | Keystone |
| 59 | 1 | U2 | REGULATOR, 1% | SO8 | 296-1288-1-ND | TL431AIDR | Texas Instruments |
| 60 | 1 | U4 | serial EEPROM | | AT24C1024W10SU2.7-ND | AT24C1024W-10SU-2.7 | ATMEL |
| 61 | 1 | U5 | 71M6521 | 64TQFP | -- | 71M6521F-IGT | TERIDIAN |
| 62 | 1 | U7 | LCD | | 153-1056-ND | VIM-808-DP-RC-S-HV | VARITRONIX |
| 63 | 1 | Y1 | 32.768kHz | | XC1195CT-ND | ECS-.327-12.5-17X-TR | ECS |

**Should be removed if present, DO NOT CONNECT**

**Table 4-3: D652T4A10 Demo Board: Bill of Material**

## 4.7 D6521T4A7 DEMO BOARD PCB LAYOUT

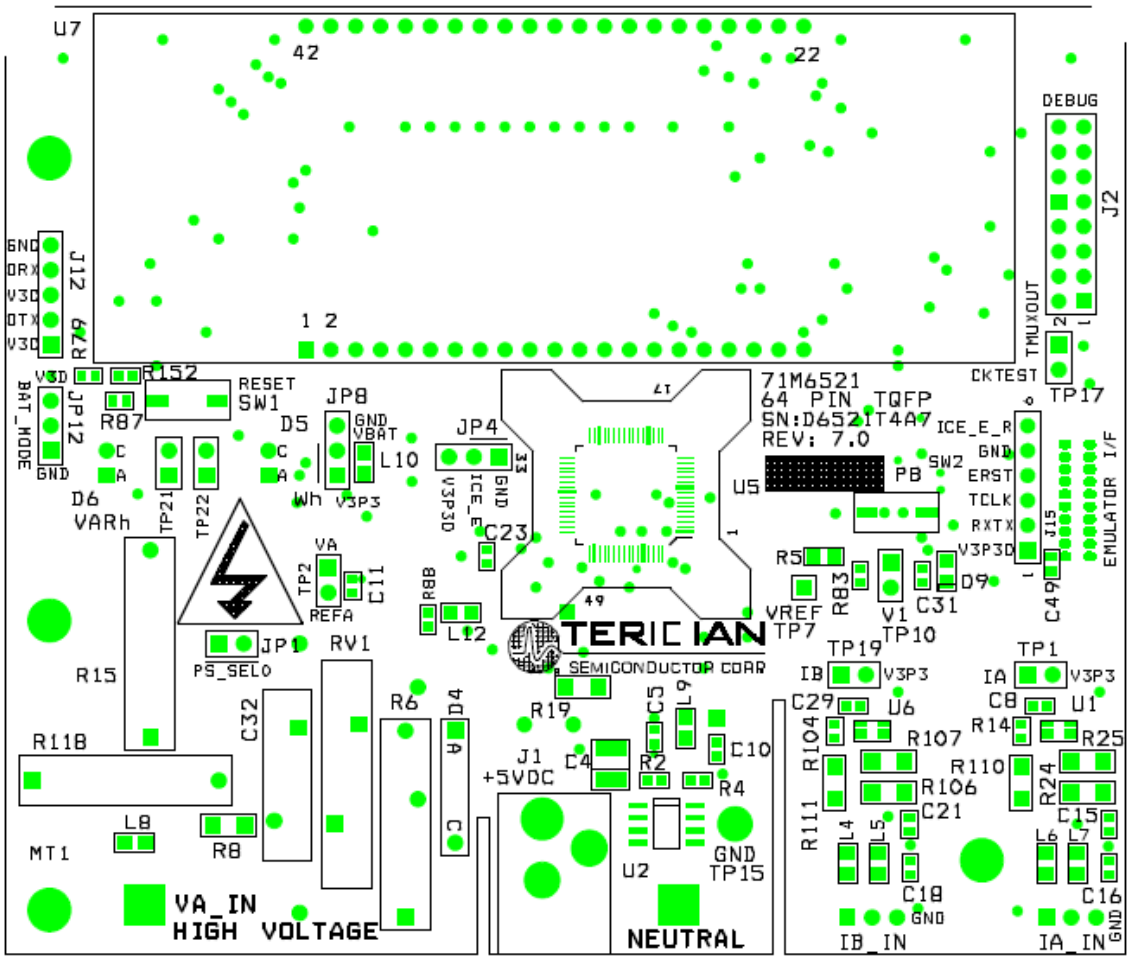



**Figure 4-8: D6521T4A7 Demo Board: Top View**

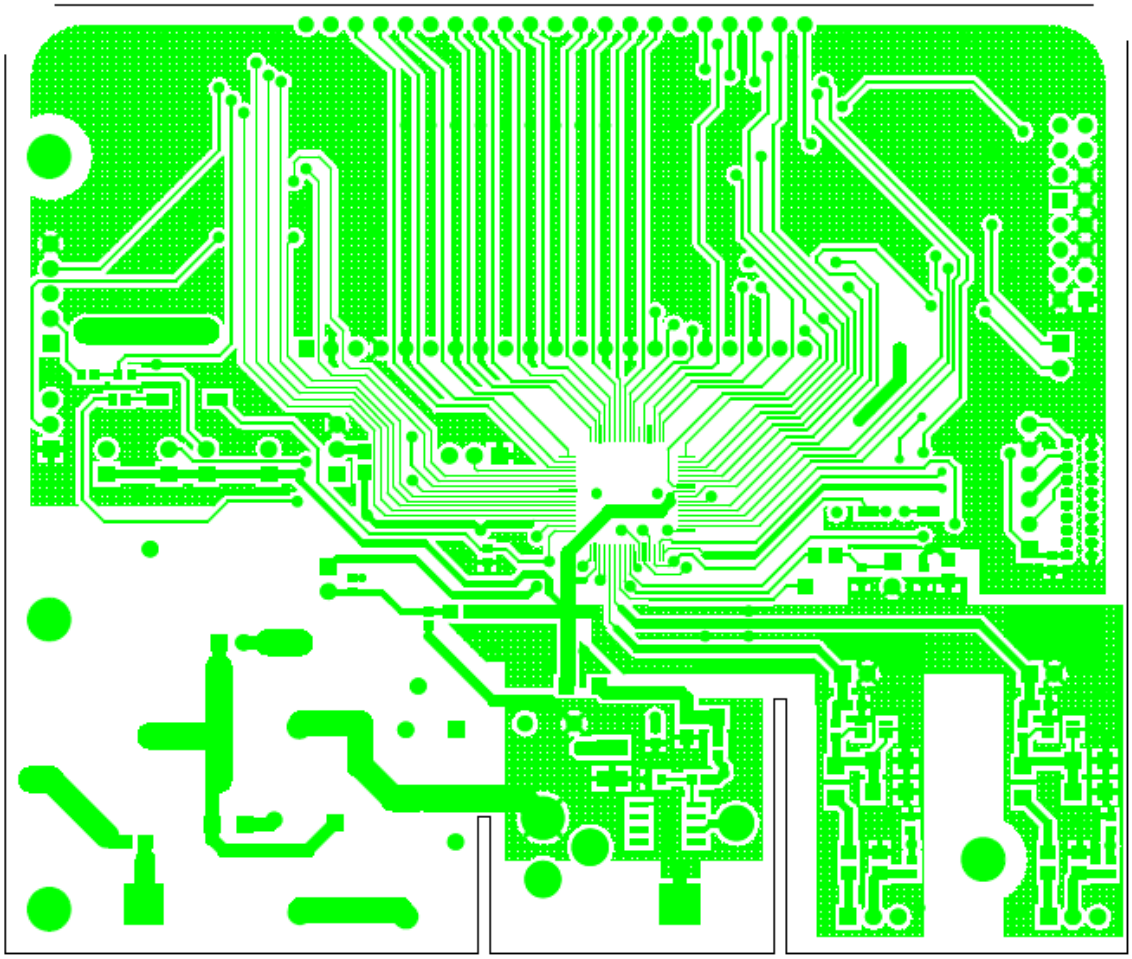


**Figure 4-9: D6521T4A7 Demo Board: Top Copper**

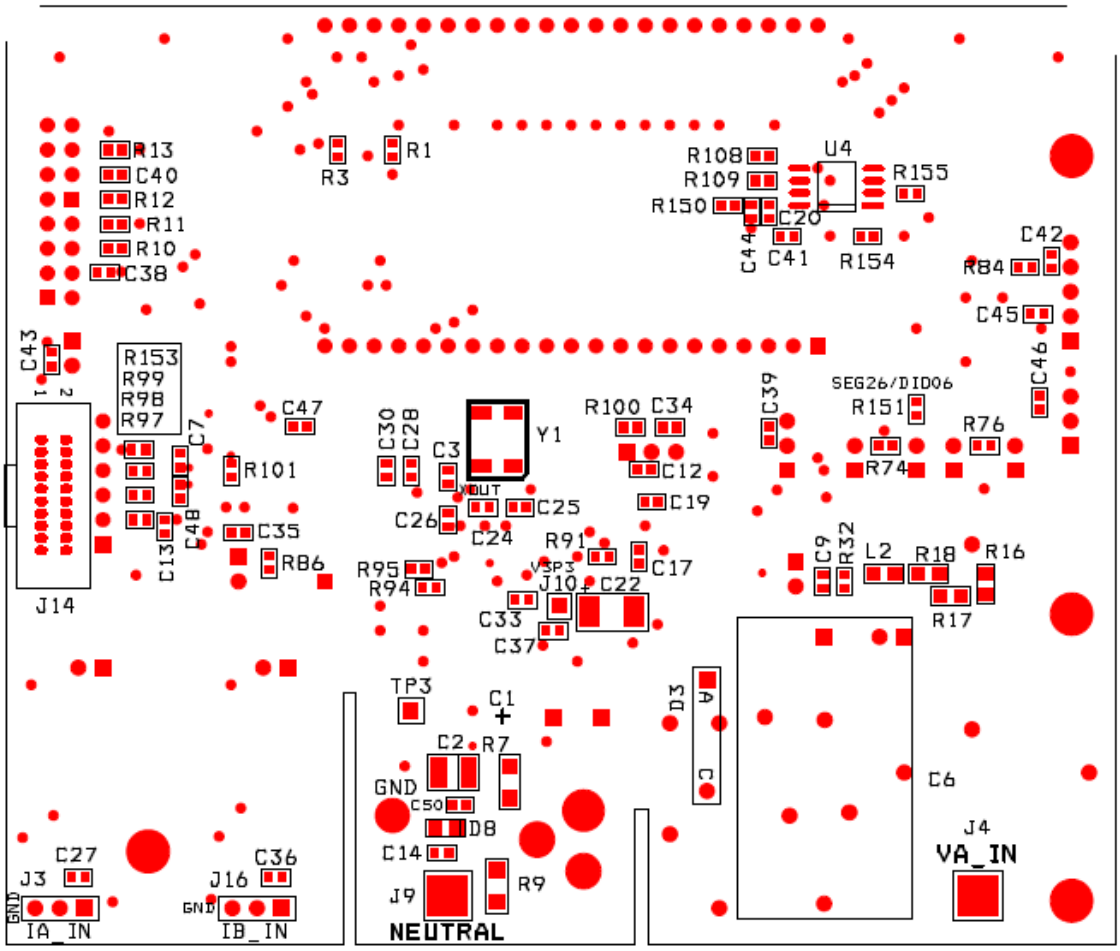



**Figure 4-10: D6521T4A7 Demo Board: Bottom View**

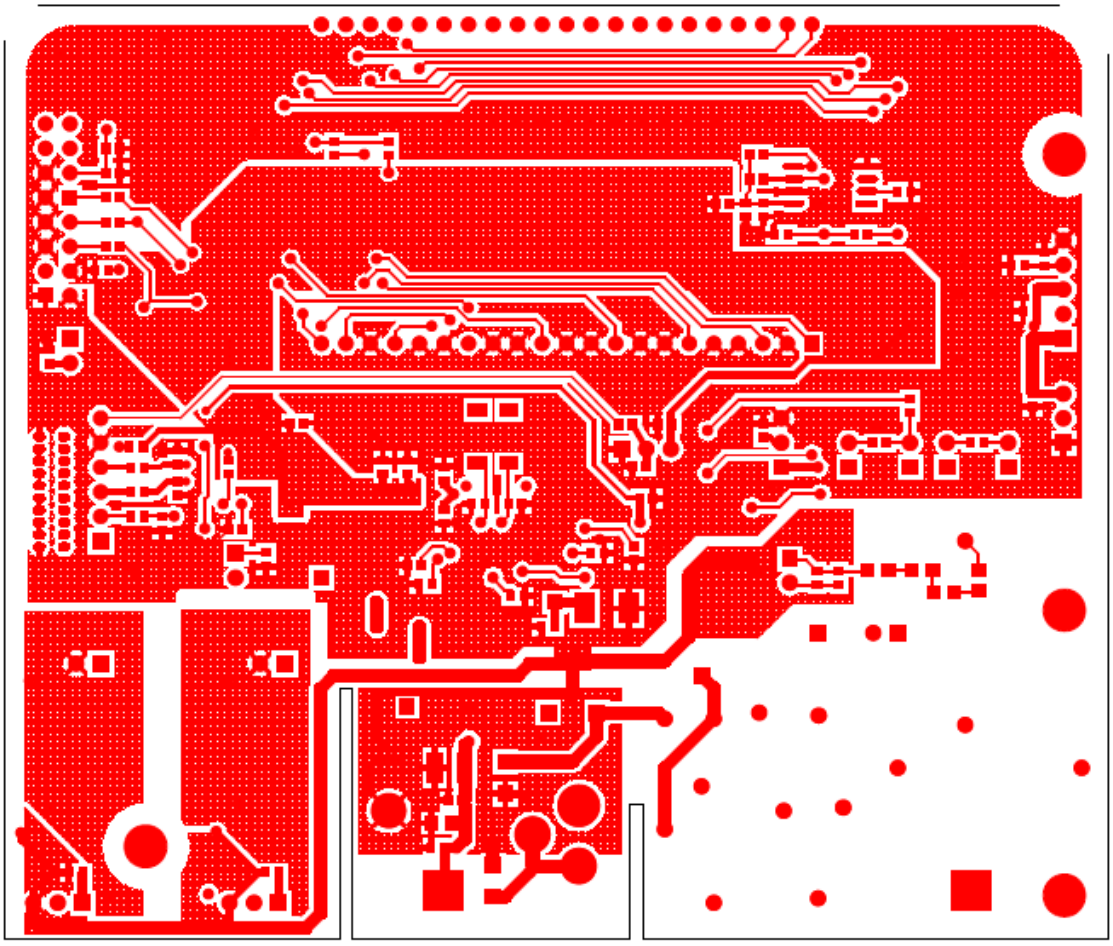


**Figure 4-11: D6521T4A7 Demo Board: Bottom Copper**

## 4.8 D6521T4A8 DEMO BOARD PCB LAYOUT

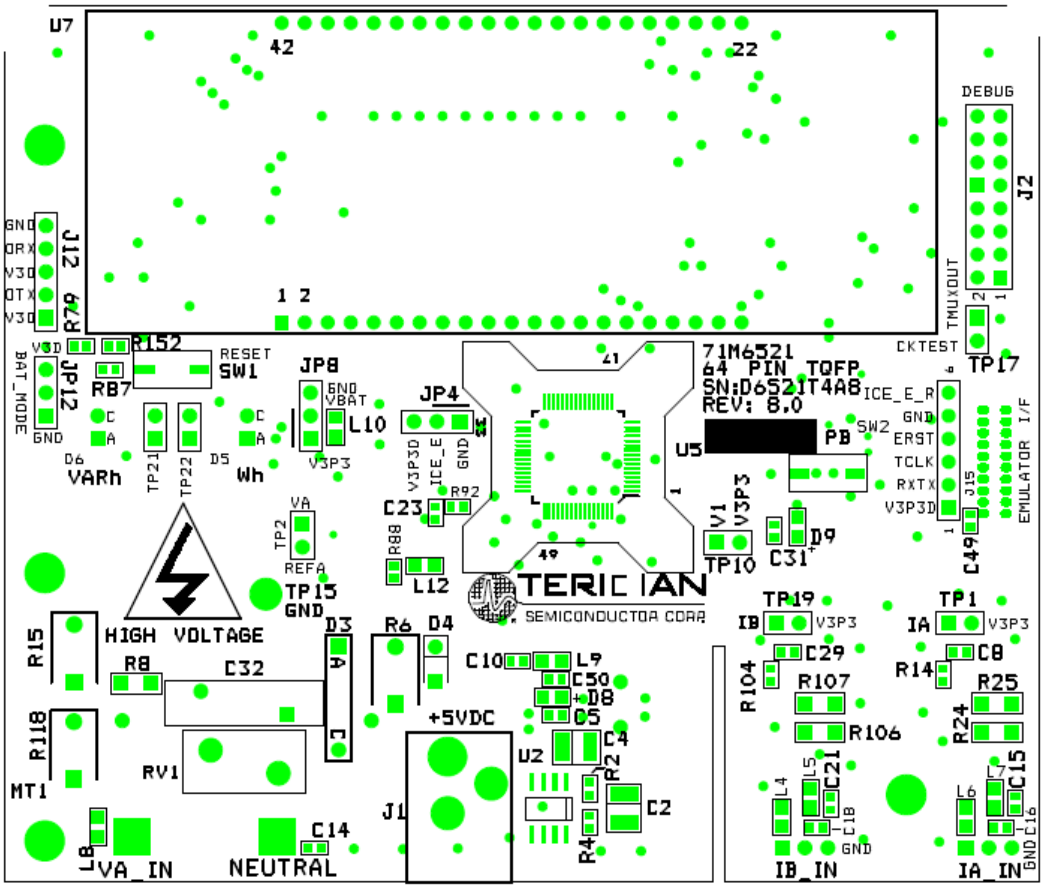



**Figure 4-12: D6521T4A8 Demo Board: Top View**

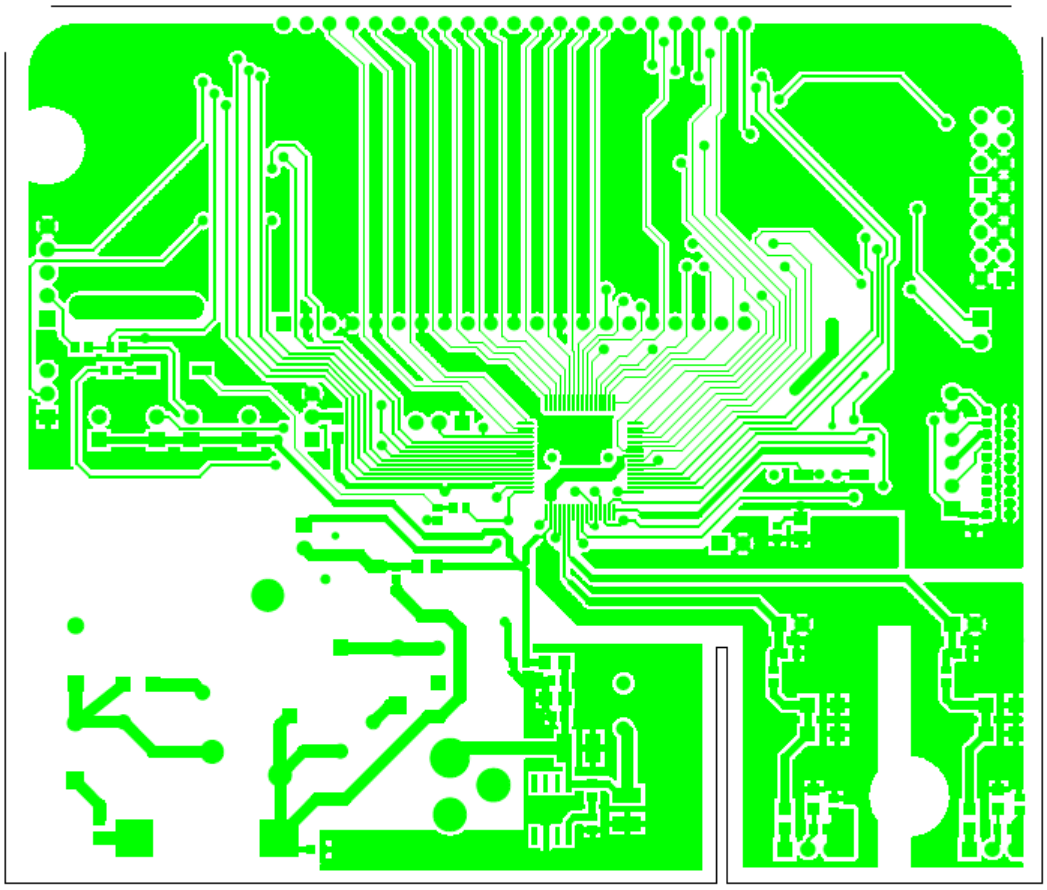


**Figure 4-13: D6521T4A8 Demo Board: Top Copper**

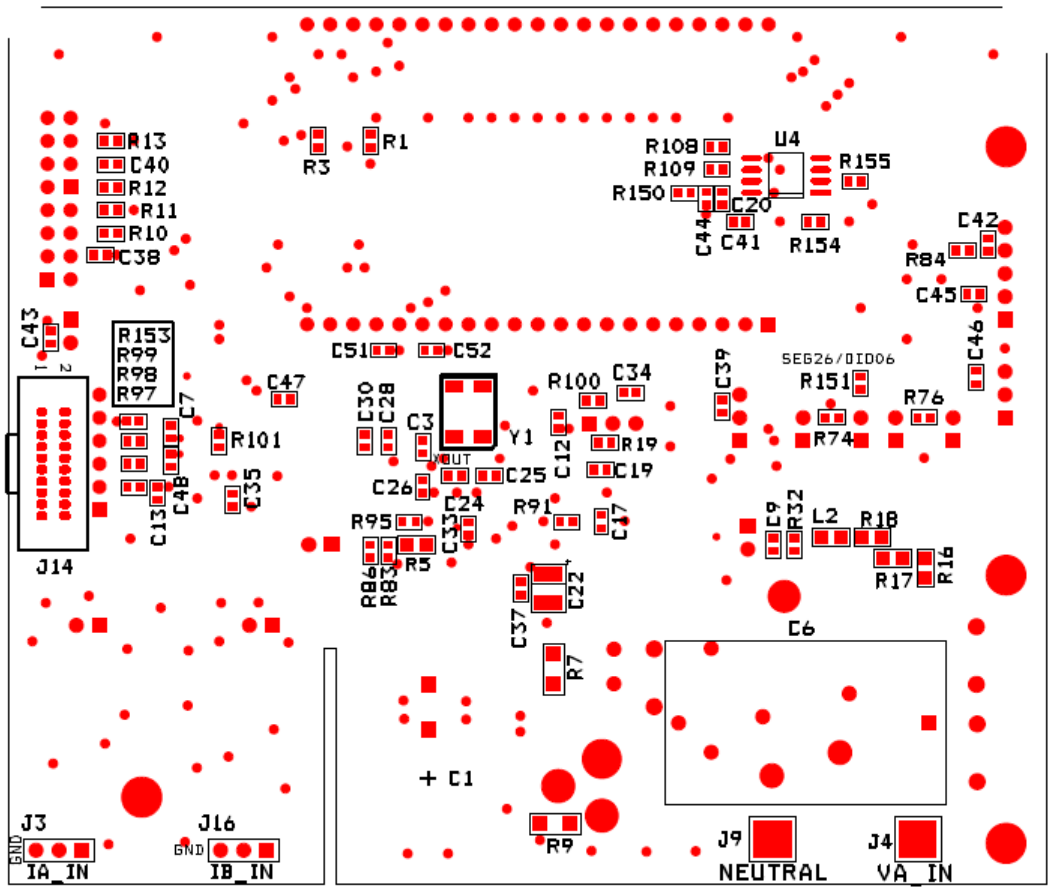



**Figure 4-14: D6521T4A8 Demo Board: Bottom View**

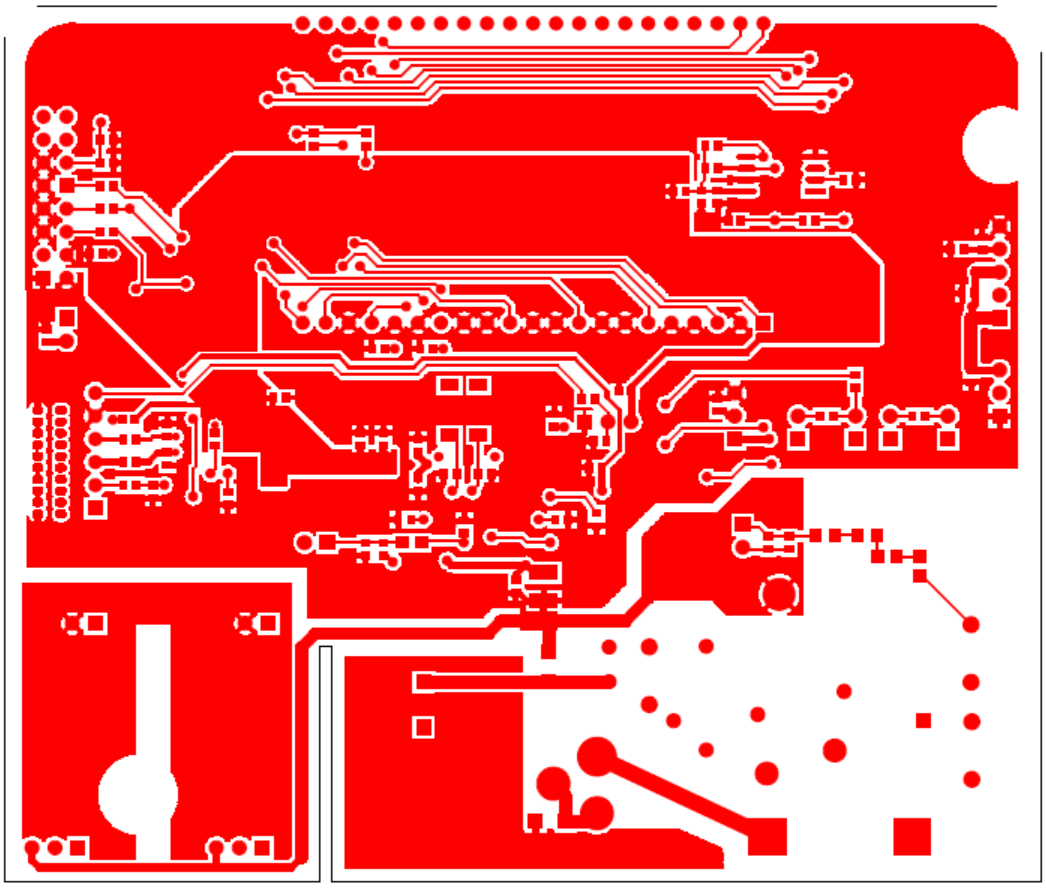


**Figure 4-15: D6521T4A8 Demo Board: Bottom Copper**

## 4.9 D6521T4A10 DEMO BOARD PCB LAYOUT

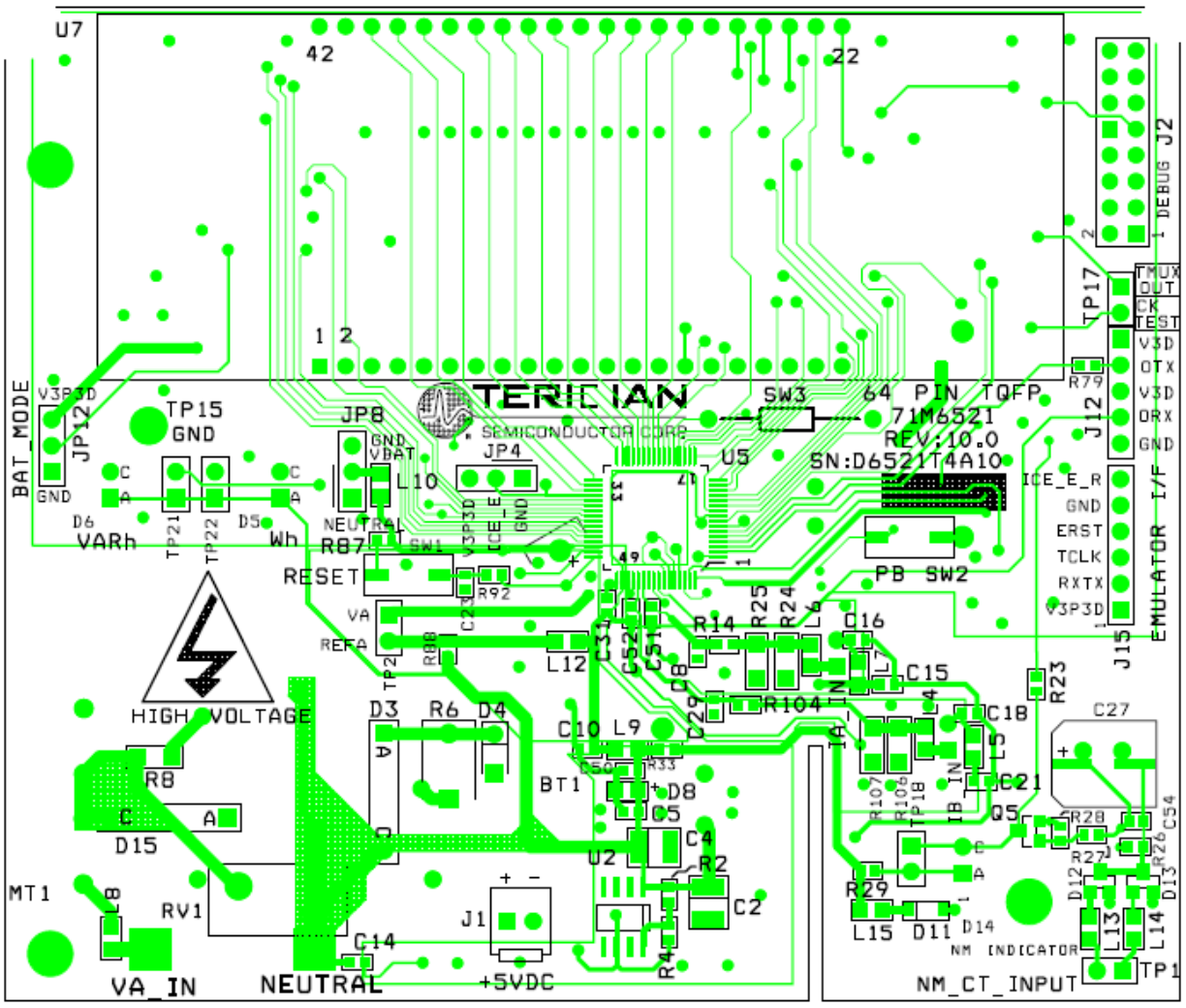



**Figure 4-16: D6521T4A10 Demo Board: Top View**

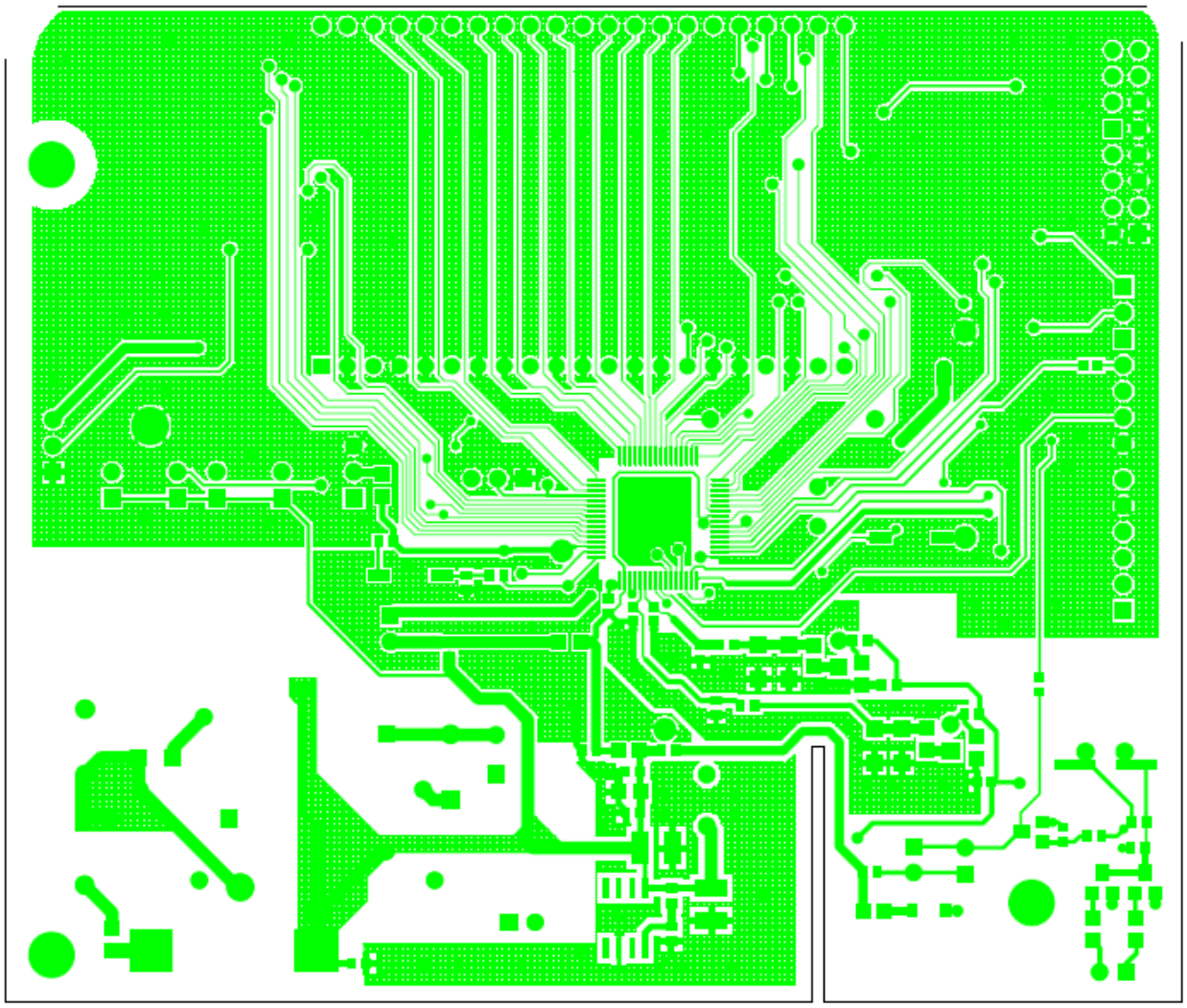


**Figure 4-17: D6521T4A10 Demo Board: Top Copper**

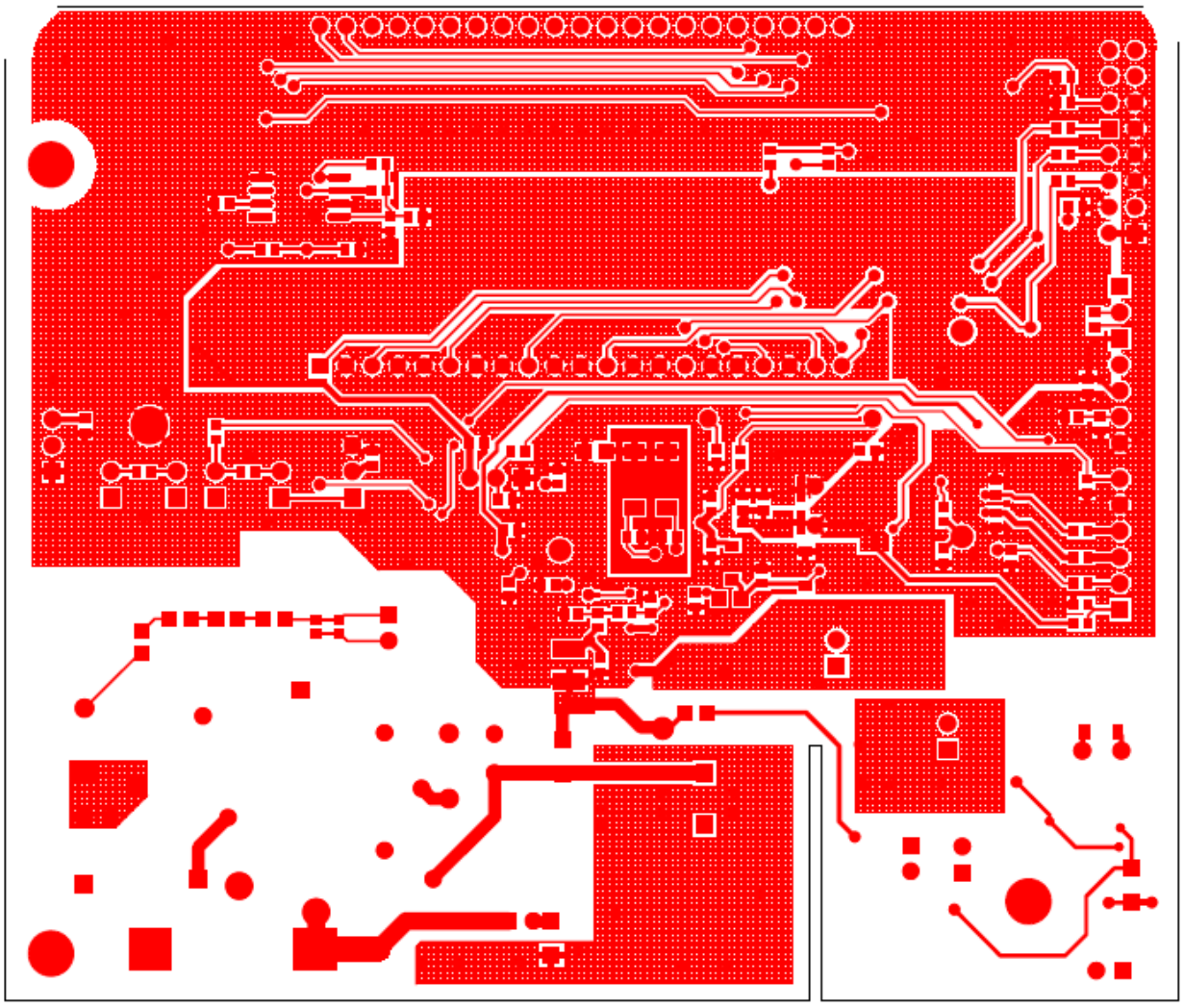


**Figure 4-18: D6521T4A10 Demo Board: Bottom Copper**

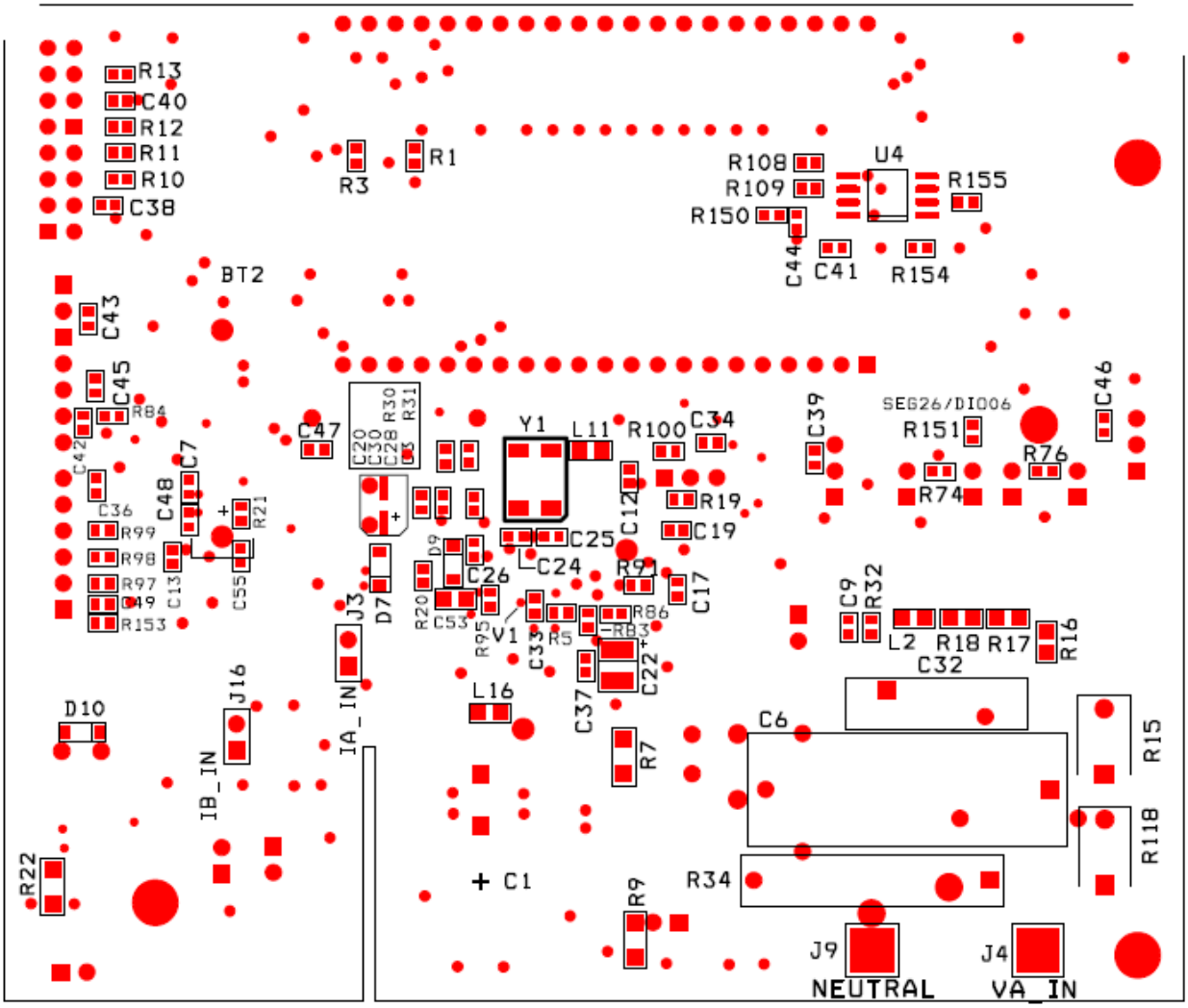



**Figure 4-19: D6521T4A10 Demo Board: Bottom View**

## 4.10 DEBUG BOARD BILL OF MATERIAL

| Item | Q | Reference | Value | PCB Footprint | P/N | Manufacturer | Vendor | Vendor P/N |
|---|---|---|---|---|---|---|---|---|
| 1 | 21 | C1-C3,C5-C10,C12-C23 | 0.1uF | 0805 | C2012X7R1H104K | TDK | Digi-Key | 445-1349-1-ND |
| 2 | 1 | C4 | 33uF/10V | 1812 | TAJB336K010R | AVX | Digi-Key | 478-1687-1-ND |
| 3 | 1 | C11 | 10uF/16V, B Case | 1812 | TAJB106K016R | AVX | Digi-Key | 478-1673-1-ND |
| 4 | 2 | D2,D3 | LED | 0805 | LTST-C170KGKT | LITEON | Digi-Key | 160-1414-1-ND |
| 5 | 4 | JP1,JP2,JP3,JP4 | HDR2X1 | 2x1pin | PZC36SAAN | Sullins | Digi-Key | S1011-36-ND |
| 6 | 1 | J1 | RAPC712 | | RAPC712 | Switchcraft | Digi-Key | SC1152-ND |
| 7 | 1 | J2 | DB9 | DB9 | A2100-ND | AMP | Digi-Key | A2100-ND |
| 8 | 1 | J3 | HEADER 8X2 | 8x2pin | PPTC082LFBN | Sullins | Digi-Key | S4208-ND |
| 9 | 4 | R1,R5,R7,R8 | 10K | 0805 | ERJ-6GEYJ103V | Panasonic | Digi-Key | P10KACT-ND |
| 10 | 2 | R2,R3 | 1K | 0805 | ERJ-6GEYJ102V | Panasonic | Digi-Key | P1.0KACT-ND |
| 11 | 1 | R4 | NC | 0805 | N/A | N/A | N/A | N/A |
| 12 | 1 | R6 | 0 | 0805 | ERJ-6GEY0R00V | Panasonic | Digi-Key | P0.0ACT-ND |
| 13 | 1 | SW2 | PB Switch | PB | EVQ-PJX05M | Panasonic | Digi-Key | P8051SCT-ND |
| 14 | 2 | TP5,TP6 | test point | TP | 5011 | Keystone | Digi-Key | 5011K-ND |
| 15 | 5 | U1,U2,U3,U5,U6 | ADUM1100 | SOIC8 | ADUM1100AR | ADI | Digi-Key | ADUM1100AR-ND |
| 16 | 1 | U4 | MAX3237CAI | SOG28 | MAX3237CAI | MAXIM | Digi-Key | MAX3237CAI-ND |
| 17 | 4 | | spacer | | 2202K-ND | Keystone | Digi-Key | 2202K-ND |
| 18 | 4 | | 4-40, 1/4" screw | | PMS4400-0025PH | Building Fasteners | Digi-Key | H342-ND |
| 19 | 2 | | 4-40, 5/16" screw | | PMS4400-0031PH | Building Fasteners | Digi-Key | H343-ND |
| 20 | 2 | | 4-40 nut | | HNZ440 | Building Fasteners | Digi-Key | H216-ND |

**Table 4-4: Debug Board: Bill of material**

# 4.11 DEBUG BOARD SCHEMATICS

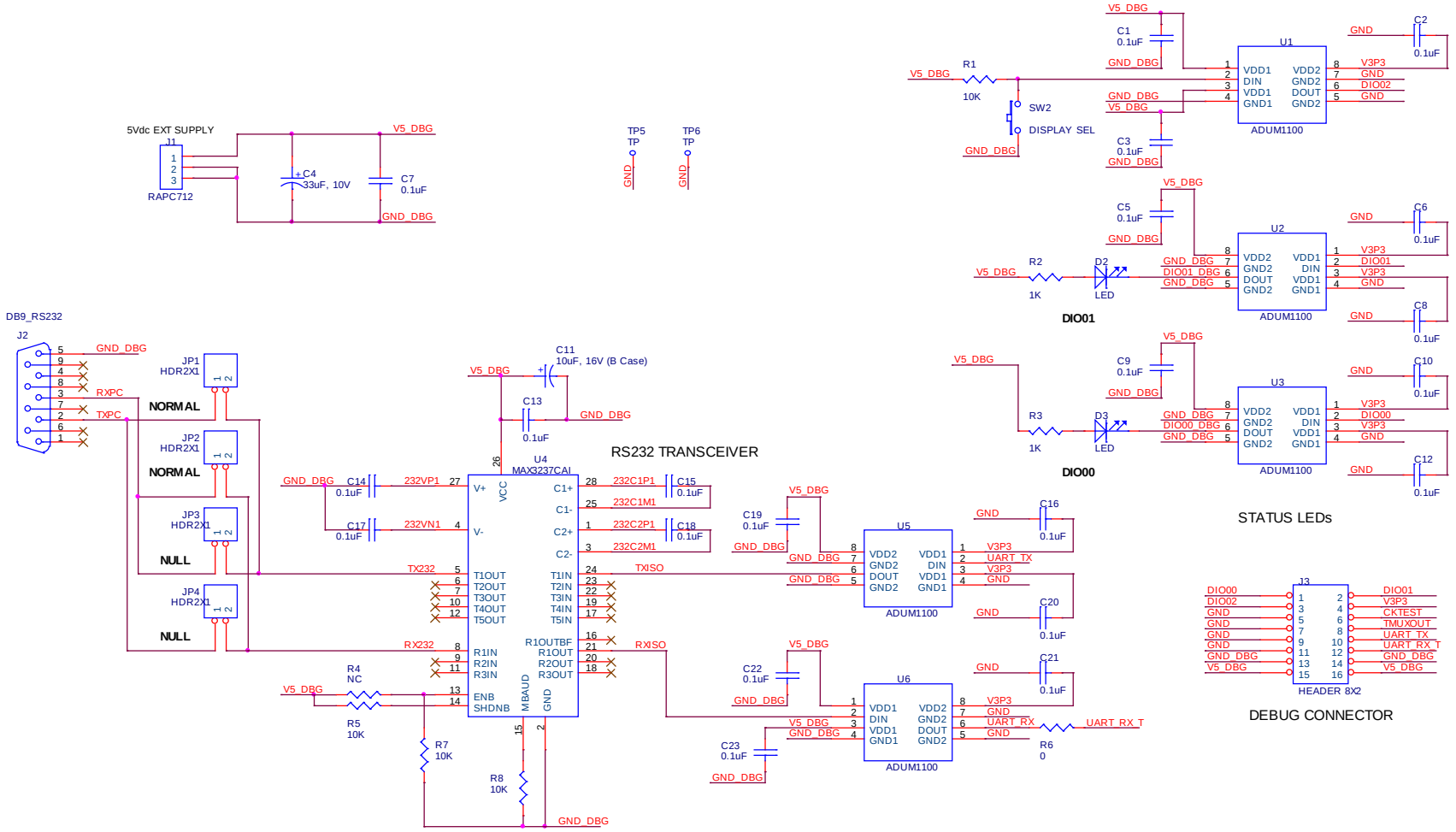



**Figure 4-20: Debug Board: Electrical Schematic**

## 4.12 DEBUG BOARD PCB LAYOUT

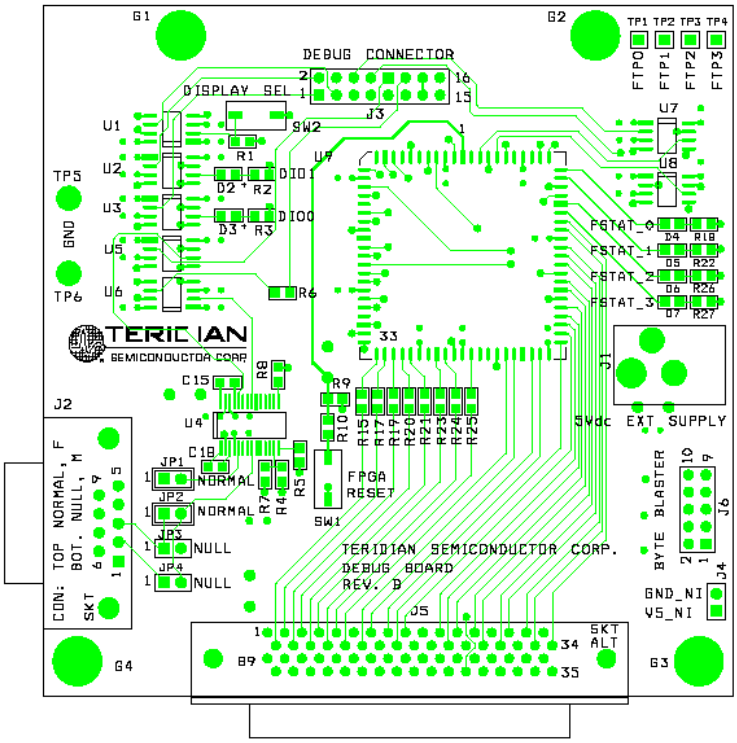



**Figure 4-21: Debug Board: Top View**

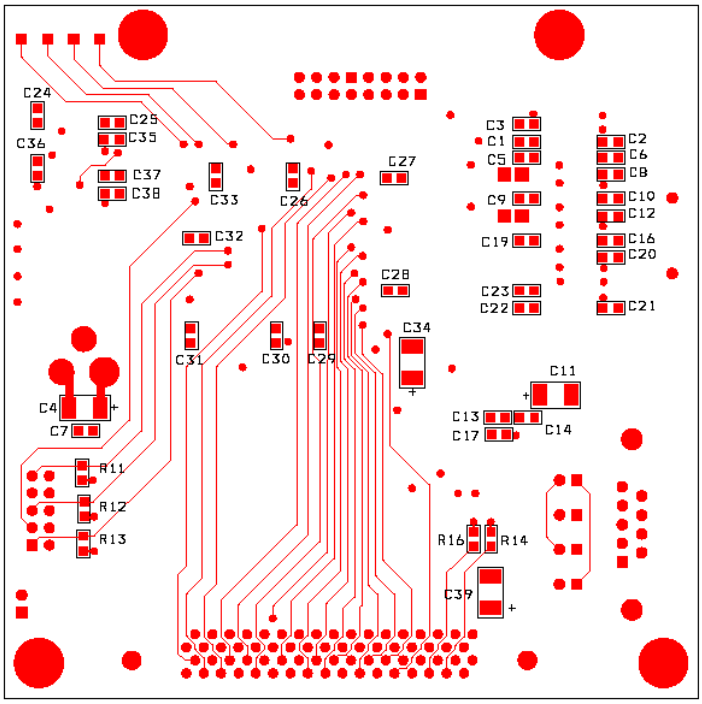


**Figure 4-22: Debug Board: Bottom View**

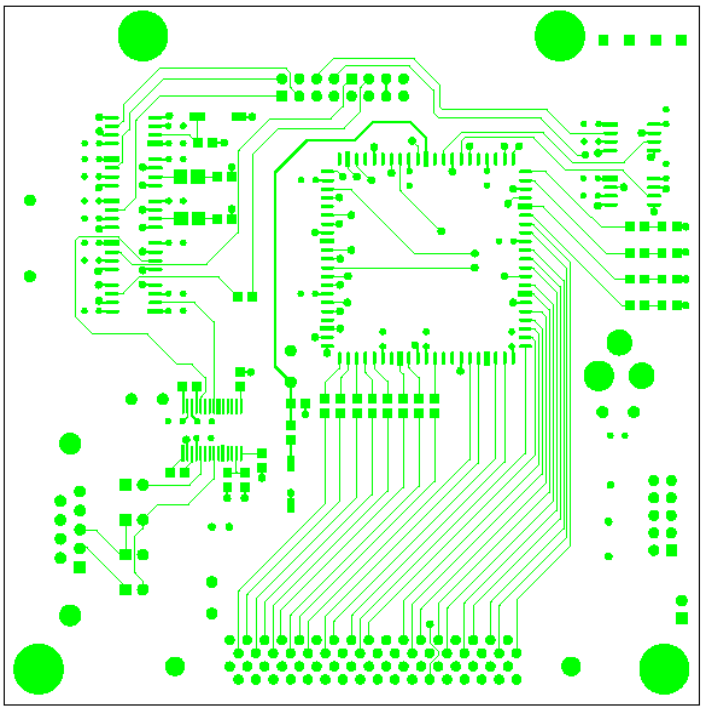


**Figure 4-23: Debug Board: Top Signal Layer**

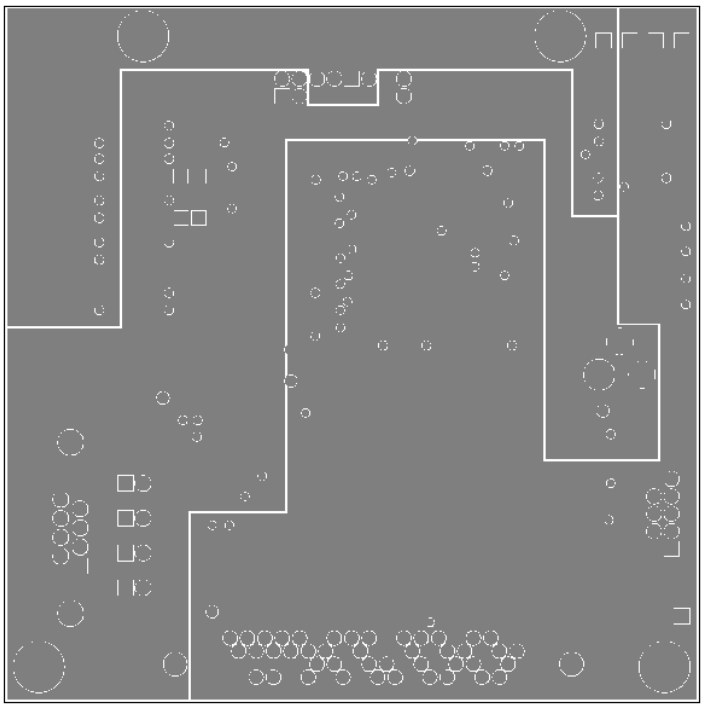


**Figure 4-24: Debug Board: Middle Layer 1, Ground Plane**

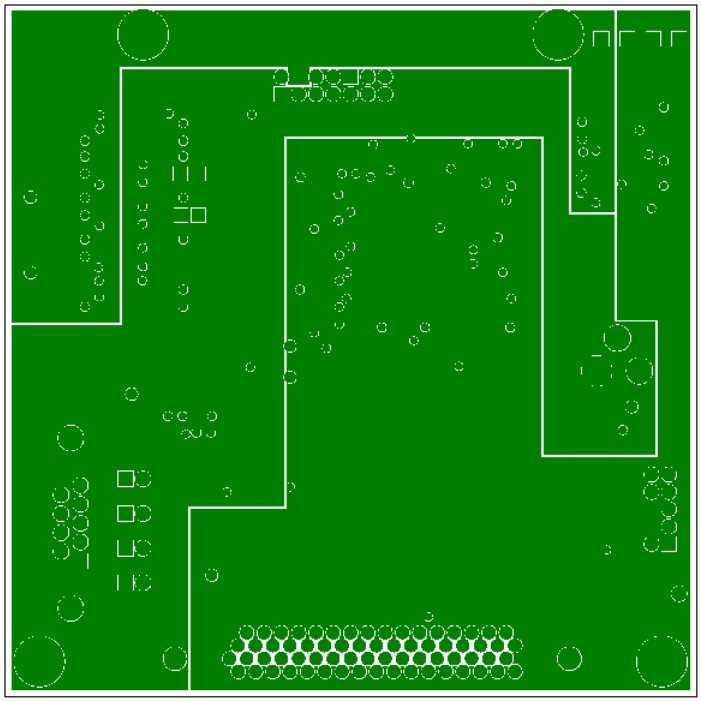


**Figure 4-25: Debug Board: Middle Layer 2, Supply Plane**

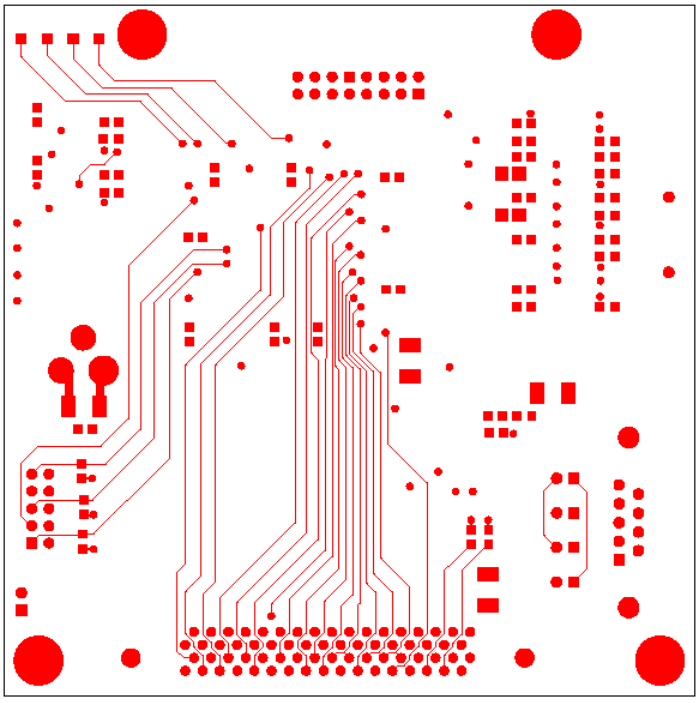


**Figure 4-26: Debug Board: Bottom Trace Layer**

## 4.13 TERIDIAN 71M6521 PIN-OUT INFORMATION

***Power/Ground/NC Pins*:**

| Name | Type | Description |
|---|---|---|
| GNDA | P | Analog ground: This pin should be connected directly to the ground plane. |
| GNDD | P | Digital ground: This pin should be connected directly to the ground plane. |
| V3P3SYS | P | System 3.3V supply. This pin should be connected to a 3.3V power supply. |
| V3P3A | P | Analog power supply: A 3.3V power supply should be connected to this pin. This power supply must be the same voltage as V3P3SYS,. |
| V3P3D | P | Auxiliary voltage output of the chip, controlled by the internal 3.3V selection switch. In mission mode, this pin is internally connected to V3P3SYS. In BROWNOUT mode, it is internally connected to VBAT. This pin is floating in LCD and sleep modes. |
| VBAT | P | Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS. |
| V2P5 | O | Output of the internal 2.5V regulator. A 0.1µF capacitor to GNDA should be connected to this pin. |

***Analog Pins:***

| Name | Type | Description |
|---|---|---|
| IA, IB | I | Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be connected to V3P3A.** |
| VA, VB | I | Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be connected to V3P3A or tied to the voltage sense input that is used.** |
| V1 | I | Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to an internal BIAS voltage (1.6V). If the input voltage is above the reference, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. A 0.1µF capacitor to GNDA should be connected to this pin. |
| VREF | O | Voltage Reference for the ADC. This pin is normally disabled by setting the *VREF_CAL* bit in the I/O RAM and can then be left unconnected. If enabled, a 0.1µF capacitor to GNDA should be connected. |
| XIN<br>XOUT | I | Crystal Inputs: A 32kHz crystal should be connected across these pins. Typically, a 27pF capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details. |

**Table 4-5: 71M6521 Pin Description 1/2**

***Digital Pins:***

| Name | Type | Description |
|---|---|---|
| COM3, COM2, COM1, COM0 | O | LCD Common Outputs: These four pins provide the select signals for the LCD display. |
| SEG0…SEG18 | O | Dedicated LCD Segment Outputs |
| SEG24/DIO4… SEG31/DIO11 | I/O | Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **If unused, these pins must be configured as outputs.** |
| SEG34/DIO14… SEG37/DIO17 | I/O | Multi-use pins, configurable as either LCD SEG driver or DIO. **If unused, these pins must be configured as outputs.** |
| SEG39/DIO19… SEG41/DIO21 | I/O | Multi-use pins, configurable as LCD driver or DIO (QFN 68 package only). **If unused, these pins must be configured as outputs.** |
| E_RXTX/SEG38, E_RST/SEG32, E_TCLK/SEG33 | I/O | Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E pulled low). |
| ICE_E | I | ICE enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG32, SEG33, and SEG38 respectively. For production units, this pin should be pulled to GND to disable the emulator port. This pin should be brought out to the programming interface in order to create a way for reprogramming parts that have the *SECURE* bit set. |
| CKTEST/SEG19 | O | Multi-use pin, configurable as either Clock PLL output or LCD segment driver. Can be enabled and disabled by *CKOUT_EN*. |
| TMUXOUT | O | Digital output test multiplexer. Controlled by *TMUX*[4:0]. |
| OPT_RX/DIO1 | I | Multi-use pin, configurable as Optical Receive Input or general DIO. When configured as OPT_RX, this pin receives a signal from an external photo-detector used in an IR serial interface. **If unused, this pin must be configured as an output or terminated to V3P3D or GNDD.** |
| OPT_TX/DIO2 | O | Multi-use pin, configurable as Optical LED Transmit Output, WPULSE, RPULSE, or general DIO. When configured as OPT_TX, this pin is capable of directly driving an LED for transmitting data in an IR serial interface. **If unused, this pin must be configured as an output or terminated to V3P3D or GNDD.** |
| DIO3 | I/O | DIO pin **(QFN 68 package only)** |
| RESET | I | This input pin resets the chip into a known state. For normal operation, this pin is connected to GNDD. To reset the chip, this pin should be pulled high. No external reset circuitry is necessary. |
| RX | I | UART input. **If unused, this pin must be terminated to V3P3D or GNDD.** |
| TX | O | UART output. |
| TEST | I | Enables Production Test. **Must be grounded in normal operation.** |
| PB | I | Push button input. A rising edge sets the *IE_PB* flag and causes the part to wake up if it is in SLEEP or LCD mode. PB does not have an internal pull-up or pull-down. **If unused, this pin must be terminated to GNDD.** |
| X4MHz | I | **This pin must be connected to GNDD.** |

**Table 4-6: 71M6521 Pin Description 2/2**

## PINOUT (QFN 68)

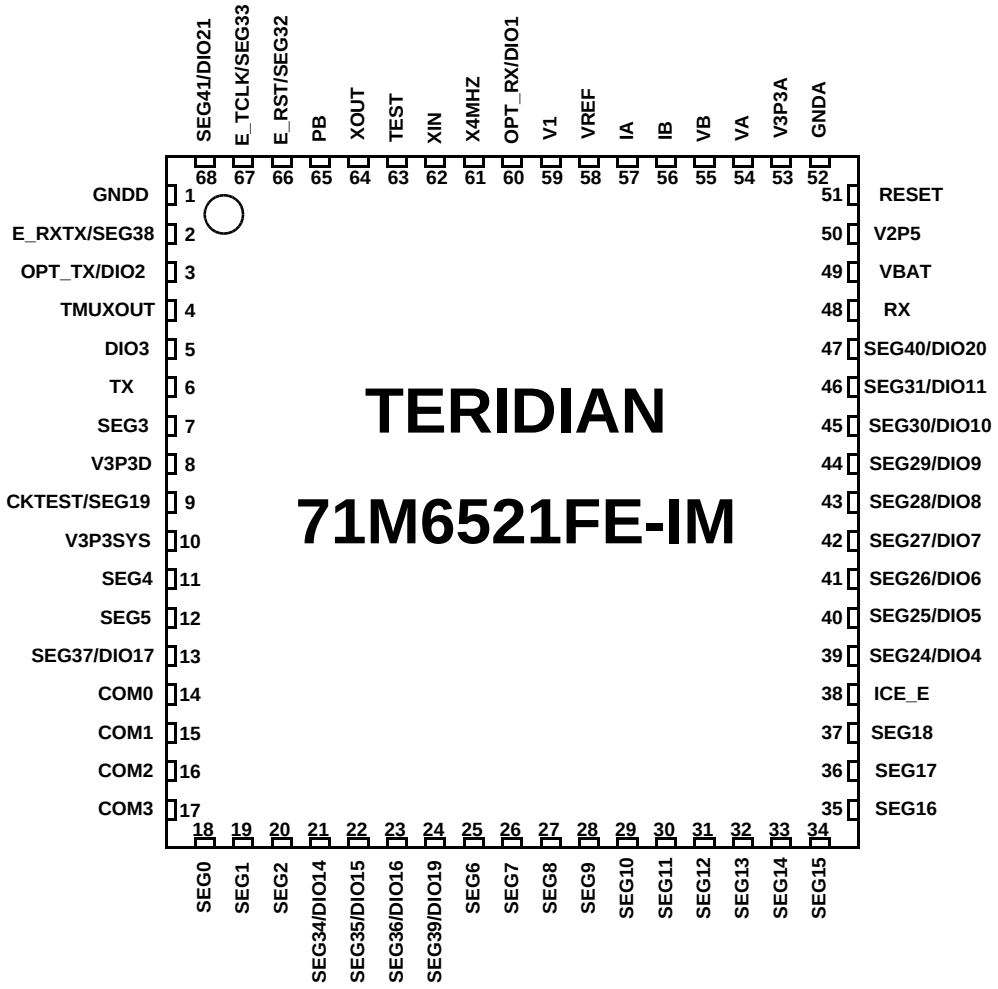



**Figure 4-27: TERIDIAN 71M6521 QFN68: Pinout (top view)**

**PINOUT (LQFP-64):**

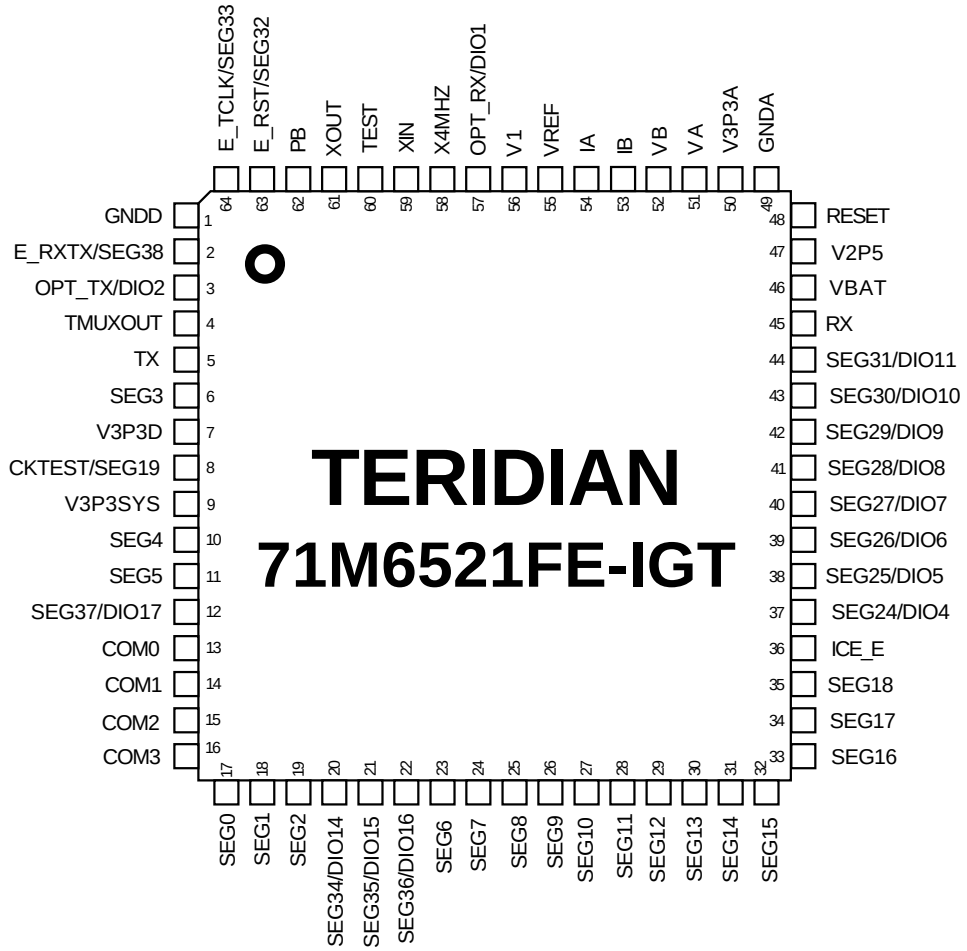



**Figure 4-28: TERIDIAN 71M6521 LQFP64: Pinout (top view)**

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### 4.13.1 MODIFICATION HISTORY

| Revision | Date | Change |
|---|---|---|
| 2-13 | 12-17-2007 | Updated schematics and BOM of Demo Board revision 6521T4A8 for improved EMI performance. Updated Teridian street address. Consolidated default kh (3.2) and WRATE settings for Demo Boards. |
| 2-14 | 01-10-2008 | Removed schematics, BOM and layout images for outdated D6521N12A3 Demo Boards. Updated figures showing calibration spreadsheets. Added Figure 1-6 showing 6521B Register Interpreter worksheet. Added Figure 3-2 and description of jumpers, headers, switches and connectors for D6521N12A4 Demo Board. |
| 2-15 | 01-31-2008 | Updated schematics and BOM for D6521T4A8. Updated pin description. |
| 2-16 | 07-24-2008 | Updated to include schematics, PCB layout, board description and BOM for D6521T4A10. Modified references to include 6521 B/BE, D/DE, and F/FE versions. |
| 2-17 | 02-10-2009 | Removed schematics, BOM and layout images for outdated D6521N12A4, D6521T4A5, and D6521T4A6 Demo Boards. Added Figure 3-1 and description of jumpers, headers, switches and connectors for D6521T4A7 Demo Board.<br>Added precautions for using batteries (chapter 2.3.8).<br>Added a list of Teridian Application Notes (chapter 2.5).<br>Added a note on the schematics and BOM of the D6521T4A10 board to remove C20.<br>Added note on availability of the CLI command "CLC" to switch to Intel hex format. |
| 2-18 | 04-15-2009 | Replaced `io_merge` command with `d_merge`. Replaced reference to FDBM flash download module with reference to TFP2 Flash Programmer.<br>Consolidated naming of ICs (71M6521BE, 71M6521DE, 71M6521FE) and removed references to discontinued versions (71M6521B, 71M6521D, 71M6521F).<br>Modified statements in 1.10.2 to reflect the fact that all Demo Kits are shipped noe exclusively with the 71M6521FE.<br>Corrected value of PPMC for 71M6521BE Demo Code. Added comments containing default values in MPU variable table for 71M6521DE/FE Demo Code.<br>Updated chapter 1.3 (Demo Kit Contents).<br>Updated default value and explanation of corresponding current value for `IThrshldA` in Table 1-13.<br>Added alternative method for determining *QUANT* in section 2.2.6. |



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